

# QPQ1905

## 2.4GHz Wi-Fi/IoT Narrowband BAW Filter

**High-performance, high power, Bulk Acoustic Wave (BAW) band-pass filter, high near-in rejection in the higher frequency channels.**

### Introduction

This purpose of this application note is to help customers translate the layout and design guidelines for the QPQ1905 Bulk Acoustic Wave (BAW) band-pass filter. The QPQ1905 is a high-performance, high power, Bulk Acoustic Wave (BAW) band-pass filter with extremely steep skirts, simultaneously exhibiting low loss in the Wi-Fi band (channels 1-2) and high near-in rejection in the 2.4GHz higher frequency channels. The filter module is specifically designed to enable unique use cases where sub-dividing usable channels within the available Wi-Fi spectrum becomes an advantage. This BAW filter is housed a 1.60mm x 2.00mm x 0.915 mm laminate package.

### Product Details

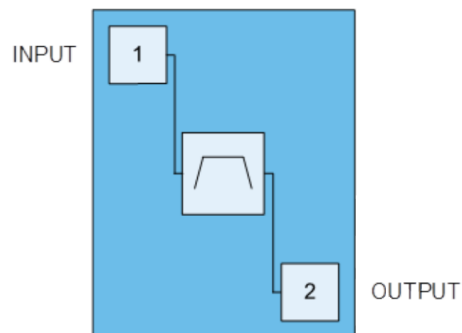


Figure 1. Functional Block Diagram & Pin-out Detail

Table 1. QPQ1905 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	INPUT	RF bi-directional port. Internally matched to 50 $\Omega$
2	OUTPUT	RF bi-directional port. Internally matched to 50 $\Omega$
Backside Paddle	-	Ground connection.

## Evaluation Board Information

The Qorvo QPQ1905 EVB is designed to provide performance representative of that obtainable in an actual application. The EVB is designed to operate with 50  $\Omega$  load impedances at all RF ports, which are provided with SMA connector interfaces.

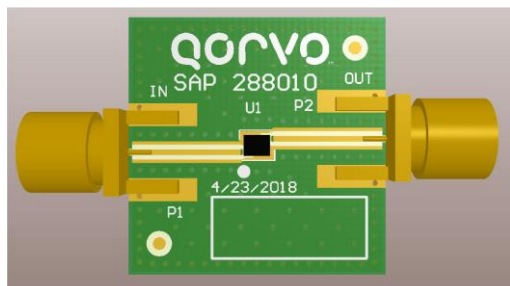


Figure 2a. QPQ1905 Evaluation Board Image

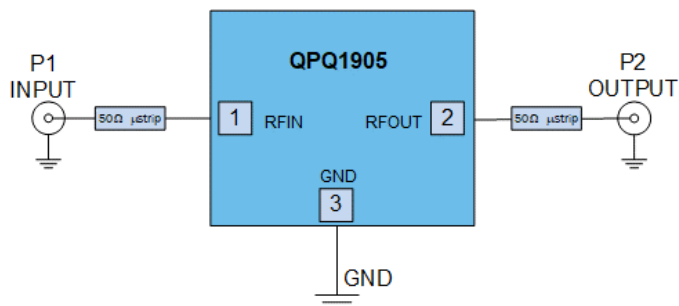


Figure 2b. QPQ1905 Evaluation Board Schematic

Table 2. QPQ1905-PCB Stack-up

LAYER	NAME	MATERIAL	THICKNESS	CONSTANT
1	Top Overlay	-	-	-
2	Top Solder	Solder Resist	0.80mil	3.5
3	Top Layer	Copper	1.40mil	-
4	Dielectric 1	Rogers R4003C	8.00mil	3.38
5	Layer 2	Copper	0.70mil	-
6	Dielectric 3	FR4	41.00mil	4.1
7	Layer 3	Copper	0.70mil	-
8	Dielectric 2	Rogers R4003C	8.00mil	3.38
9	Bottom Layer	Copper	1.40mil	-
10	Bottom Solder	Solder Resist	0.80mil	3.5
11	Bottom Overlay	-	-	-

Total Thickness: 62.8mil

Table 3. QPQ1905 Evaluation Board Bill of Materials

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURE	PART NUMBER
-	-	Printed Circuit Board	-	-
U1	-	QPQ1905 BAW Filter	Qorvo	QPQ1905

## System Architecture Application Circuit Recommendations

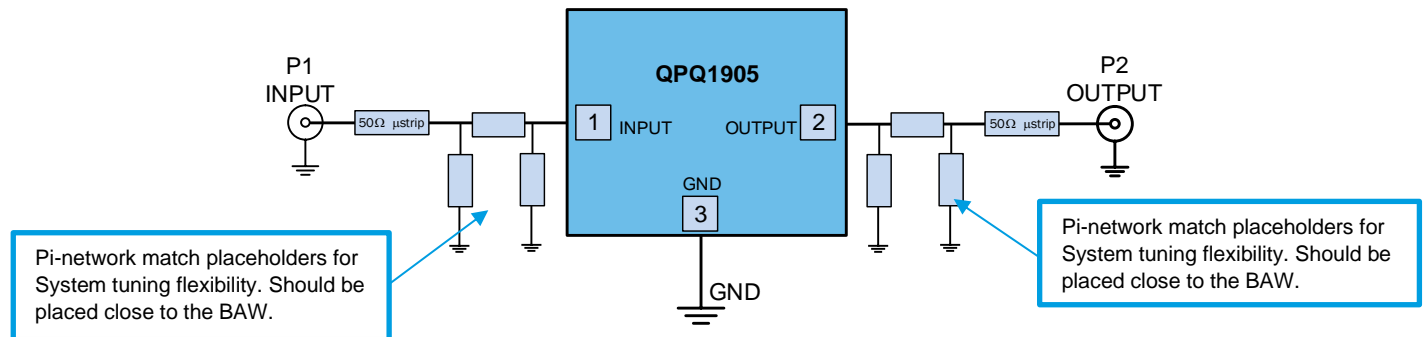


Figure 3. Recommended Application Circuit in a System.

1. The above schematic shows recommended Pi-network match placeholders for system tuning flexibility based on the QPQ1905 EVB. The customer should ensure that Pi-network matching is provided based on their PCB layout.
2. It is recommended to place a ground via next to each GND pin of the BAW and to add ground vias around RF traces. For example, each ground pin should have their own ground via.
3. We recommend following Qorvo evaluation board layout guidelines as close as possible. The QPQ1905 evaluation board uses 8 mil GND vias with 8 mil pads under the BAW. Gerber files are available upon request.

## PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any BAW filter, including the QPQ1905. In addition to providing connectivity between the BAW and external components, the PCB layout is a part of the overall circuit. The RF parasitic of the traces, along with coupling between traces, must be evaluated. The QPQ1905 Evaluation Board PCB layout guidelines provide a good starting point for designing the layout in the actual application.

### RF Traces

All PCB traces between the RF pins and matching networks (where applicable) should be 50  $\Omega$  controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on the top layer to minimize coupling with other RF, control input, and DC traces present on the PCB. If it is not possible for some reason to route RF traces on the top layer, we suggest that you make sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals from other components by adding solid ground planes (with vias) between them to minimize coupling and cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible.

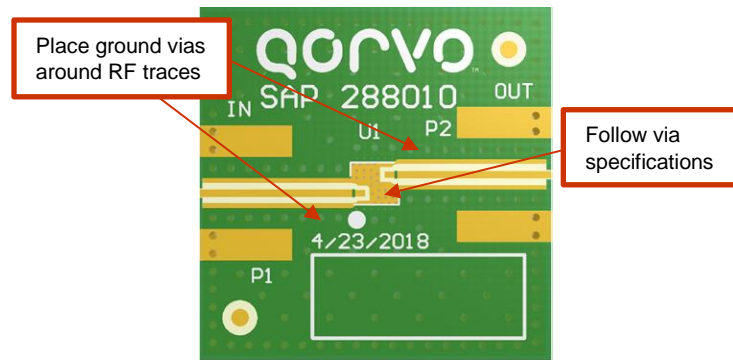


Figure 4a. Recommended PCB layout Considerations.

## Grounding Considerations

**Grounding of BAW GND pins** - The ground pins serve as the primary RF ground reference for the entire BAW. Connect the BAW filter ground pins directly to the main ground plane layer of the PCB. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines. **Reference Plane** - A larger number of via holes should be distributed over the entire area below/around the BAW to provide good RF ground reference ground plane, as shown in **Figure 4b** below. Alternately, it is recommended to place a ground via close and next to each GND pin of the BAW to avoid a ground loop. Each ground pin should have their own ground via. The QPQ1905 EVB uses GND vias with an 8mil diameter and 8mil hole size under the BAW.

**GND Vias for Thermal Considerations** – The BAW GND pins serve as the primary path for heat removal, additionally, the PCB ground vias will serve as a low resistance thermal path between the BAW and the PCB. Vias passing through multiple copper layers provide the best overall RF and thermal performance. The QPQ1905 ground pins have special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo evaluation board should be replicated. The Qorvo layout files in Gerber format can be provided upon request.

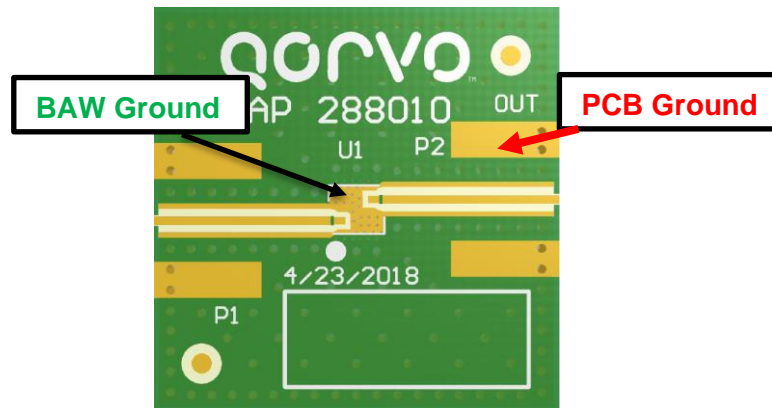


Figure 4b. Recommended Ground Via Placement.

## DC Layout Considerations

All DC traces routed near the BAW must be isolated with a GND in between the BAW and the DC trace. The GND should have vias on them which route from the top layer through to the bottom GND layer. It is recommended to avoid routing traces underneath the BAW.

## PCB Footprint Recommendations

See **Figures 5a and 5b** below for the recommended package outline drawing and solder mask patterns.

## PCB Footprint Recommendations

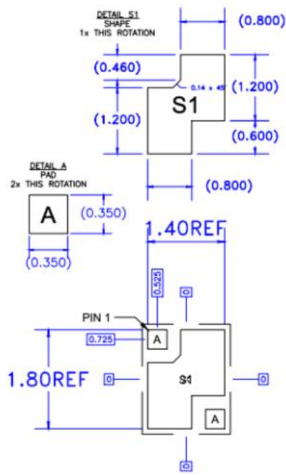


Figure 5a. PCB Footprint Recommended Landing Pattern

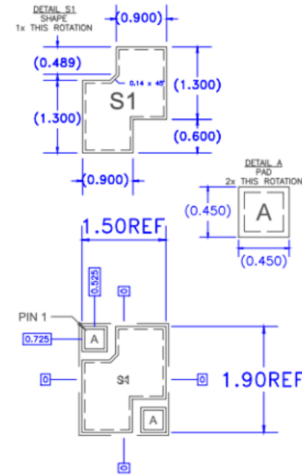


Figure 5b. PCB Footprint Recommended Solder Mask Pattern

## Package Information

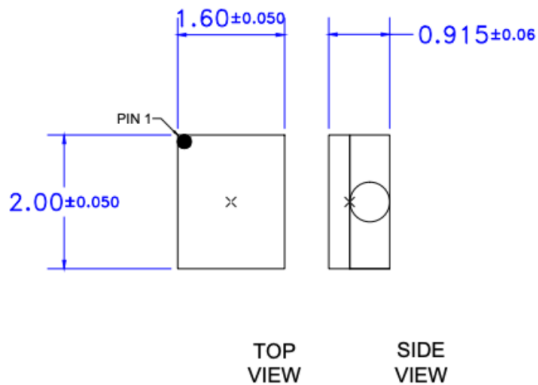


Figure 5c. Marking Diagram

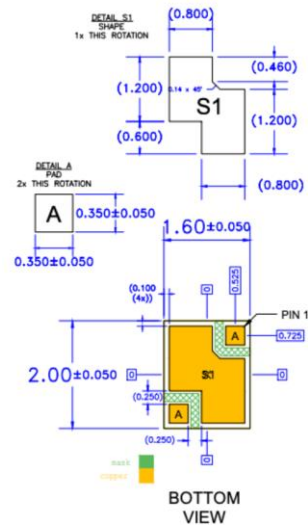


Figure 5d. QPQ1905 Package Outline Drawing

Dimensions: 1.60mm x 2.00mm x 0.915mm

### Notes:

1. All dimensions shown are typical in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo evaluation board for this product. Some modifications may be necessary to suit end user assembly materials and processes.

## Reflow Profile & Solder Paste

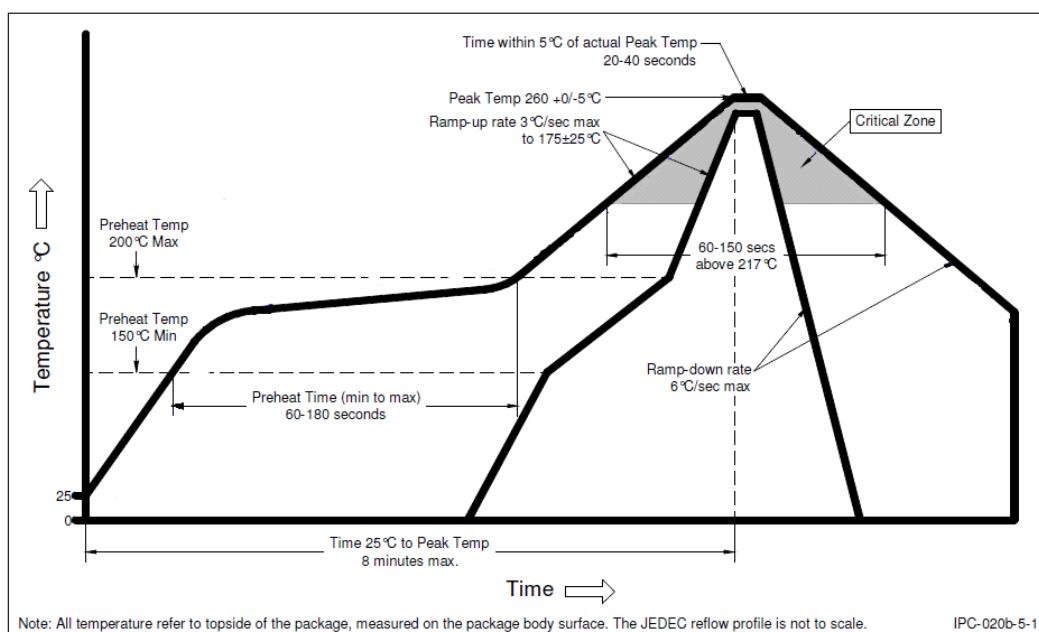


Figure 6a illustrates the recommended reflow profile for the QPQ1905

Table 4. Recommended Reflow Profile & Conditions

CONDITIONS	
Ramp-up rate	3 °C/second max.
Preheat temperature 175 (±25) °C	180 seconds max.
Temperature maintained above 217 °C	60 seconds to 150 seconds
Time within 5 °C of actual peak temperature	20 seconds to 40 seconds
Peak temperature range	260+0/-5 °C
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤ 3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed
Maximum reflow temperature	260 °C

Maximum reflow temperature is 260°C. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification except for the maximum reflow temperature of 260 °C.

Solder paste used for the Qorvo high temperature reflow qualification.

Table 5. Solder Paste Specifications.

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

## Support Data

For any further data on the QPQ1905, please request Qorvo point of contact such as marketing, sales or a representative in your region.

## Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** 1-844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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