Practical considerations when comparing SiC and GaN in power applications

Anup Bhalla, PhD.

VP Engineering
UnitedSiC, Inc.

Abstract

Silicon Carbide (SiC) and Gallium Nitride (GaN) semiconductor technologies are promising great things for the future. SiC devices in a cascode configuration enable existing systems to be easily upgraded to get the benefits of wide band-gap devices right now.

Wide band-gap devices – what they promise

Wide band-gap (WBG) semiconductor technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are the hot topics of the moment, promising anything from universal wireless charging to power converters shrunk to almost no size. However, the choice between the technologies and devices available is not always straightforward, and the markets they can penetrate are perhaps wider than you might think.

Let's take a step back and just outline what WBG devices are. Semiconductors have bound electrons that occupy distinct energy levels around an atomic nucleus – valence and conduction bands. Electrons can move up to the conduction band and be available for current flow, but require energy to do so. In WBG devices this energy requirement is much greater than with silicon (Si). For example, SiC requires 3.2 electron-volts (eV) compared with Si at 1.1eV. The increased energy required to move electrons in WBG devices into the conduction band translates to higher electric field breakdown performance compared with Si of the same scale. For the same reason, SiC can withstand higher temperatures (thermal energy) before failure and also, as a material, has a thermal conductivity about 3.5 times better than Si. In practice these attributes promise high-frequency, high-temperature operation at high voltage and power levels.

Devices initially available in SiC were simple diodes, but the material technology has advanced to enable fabrication of JFETs and MOSFETs. **Figure 1** shows a cell of a SiC JFET with a vertical trench construction giving very low ON-resistance, compared with a GaN High Electron Mobility Transistor (HEMT) cell with lateral construction.
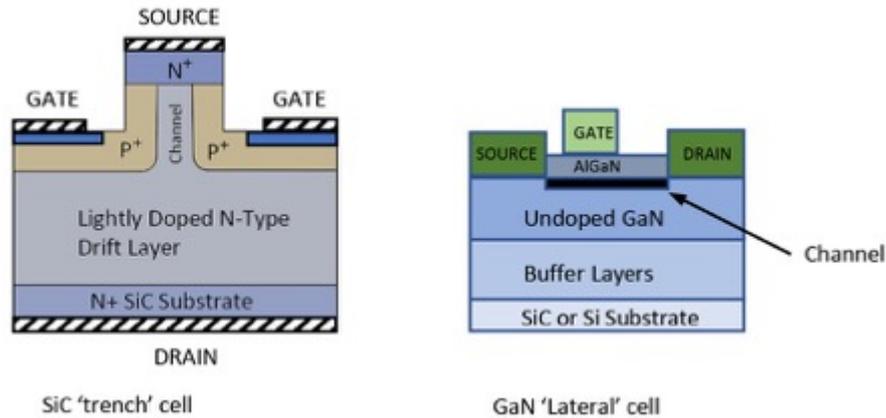
Figure 1.   SiC and GaN JFET cells – typical construction

### Finding the optimum solution for your application

Although enhancement-mode, normally OFF, Si- and now SiC-MOSFETs have been the component of choice for low- and medium-power switching applications, they do have some disadvantages:

- MOSFETs have an integral body diode that has a high forward voltage drop and relatively high recovery charge (Q_{rr}), which typically varies by a factor of three over-temperature. High Q_{rr} and high forward voltage drop correspond to high losses in circuits, which force or require the body diode to conduct such as choppers, hard-switched bridges with inductive loads and the currently popular bridgeless totem-pole arrangement for PFC stages. An extra parallel SiC Schottky diode can be added to bypass the body diode, but at significant cost and with limited benefit.
- With MOSFETs, the gate turn-on threshold is low, about 2.2V for SiC devices whose gate-source voltage has to be kept within quite tight limits for optimum and safe performance.
- Short-circuit saturation current varies with gate-source voltage and is poorly controlled, a major concern for system reliability.
- Input, output and Miller capacitances around MOSFETs are relatively high. This leads to significant gate-drive power requirements, losses as the capacitances are charged and discharged, and the danger of spurious device turn-on from current injected into the gate through the Miller capacitance.

JFETs can be considered, with no body diode, but are inconveniently normally ON with zero gate voltage and OFF with about -7V applied. Normally ON devices are useful in some applications such as circuit-breakers, but for switching applications normally OFF types are much preferred.

Cascode arrangements of switches

To avoid the problems of MOSFETs while still using WBG technology, manufacturers have turned the clock back to the vacuum-tube technology of the 1930s and revisited the cascode arrangement shown in **Figure 2**.
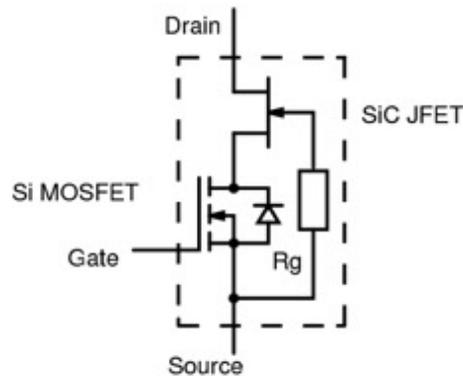
**Figure 2.   Cascode arrangement of Si MOSFET and SiC JFET**

Here, a low-voltage Si-MOSFET is connected with its drain to the source of a SiC trench JFET with the JFET gate sharing a common connection to the MOSFET source. When a positive voltage is applied to the Si-MOSFET gate, it turns ON, effectively shorting the JFET gate-to-source, turning it ON. When the Si-MOSFET gate is at zero volts, it is OFF, allowing its drain to rise in voltage. However, when this reaches about +6V, the JFET gate becomes 6V more negative than its source, turning it OFF. The MOSFET drain voltage will increase to 15-20V based on the voltage needed to fully pinch-off the JFET. Unlike other cascode implementations, the near zero C_{DS} of the JFET after pinch-off means that the capacitive divider with the Si-MOSFET favors ALL the voltage developing across the HV JFET. The Si-MOSFET can therefore be a low-voltage type with associated very low ON-resistance $R_{DS(on)}$ of a few milliohms. The overall ON-resistance is then dominated by the JFET channel.

We now have a normally OFF device like a MOSFET, but we have also solved the other MOSFET limitations as a bonus:

- A body diode has been introduced as part of the low-voltage Si-MOSFET but one with a very low Q_{rr} figure, smaller than that of a high-voltage SiC-MOSFET by a factor of two or more, and around twenty times less than a standard fast-recovery diode. In practical circuits that see the body diode conducting, an extra parallel diode is not necessary.
- The Si-MOSFET gate drive is not critical compared with a SiC-MOSFET and can withstand +/-25V maximum.
- The gate-source voltage of the Si-MOSFET in the cascode does not affect short-circuit saturation current after full enhancement at about +8V. The current is now controlled by a "pinch-off" effect in the vertical trench of

the JFET, which effectively limits current to a saturation level. Additionally, the heating effect produced by the current decreases the JFET channel conductivity, giving a self-limiting characteristic. The high allowed junction temperature also helps here.

- Because the Si-MOSFET in the cascode is low voltage and optimized for the application, its input capacitance C_{iss} is low and the cascode drain-gate Miller capacitance C_{rss} is virtually zero. See **Figure 3** for a UnitedSiC 1200V 60 milliohm device. This results in reduced gate-drive power and elimination of the danger of spurious turn-on due to drain positive-going dV/dt pushing spikes of current through the Miller capacitance into the gate-drive circuit.

- There is energy lost in switching, E_{oss}, associated with C_{oss}. In the 650V class of devices, a SiC cascode at around 6.5µJ has half the value or better than comparable Si- or SiC-MOSFETs.
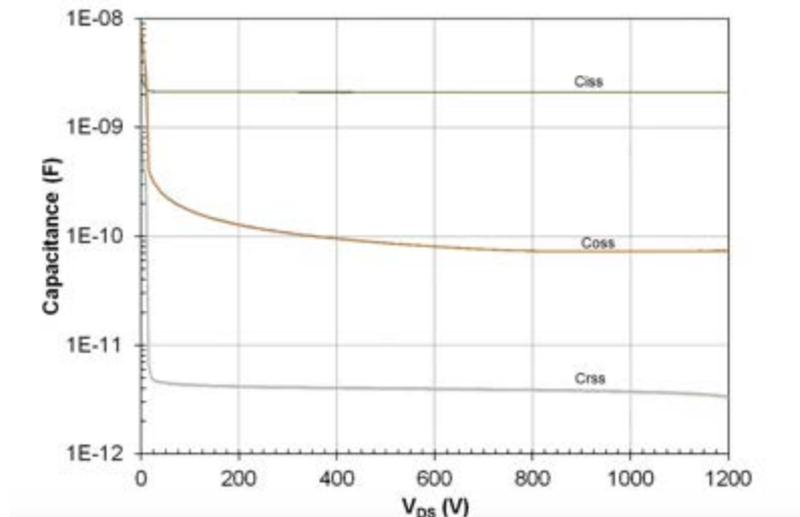
Figure 3.   Typical SiC cascode device capacitances

If the cascode has any caveat, it is the need to tame its speed! Practical designs will limit dV/dt and di/dt to manageable values to meet EMC standards and limit induced current spikes in associated circuitry and voltage spikes across the inductance of connections. When carefully configured, cascode arrangements can give effective control of dV/dt and di/dt with external gate resistors. **Figure 4** gives the values achieved with a gate resistor $R_{(on)}$ between 2.35 and 20.5 ohms for a UnitedSiC UJC1206K cascode device with a 600V inductive load. Bear in mind that every 1nH of inductance gives a 1V transient with a di/dt of 1000A/microsecond. If this transient appears in the gate-circuit loop it reduces turn-on or turn-off margin. Similarly, an easily achievable 50V/ns dV/dt would produce a 1A current spike into just 20pF of stray capacitance.
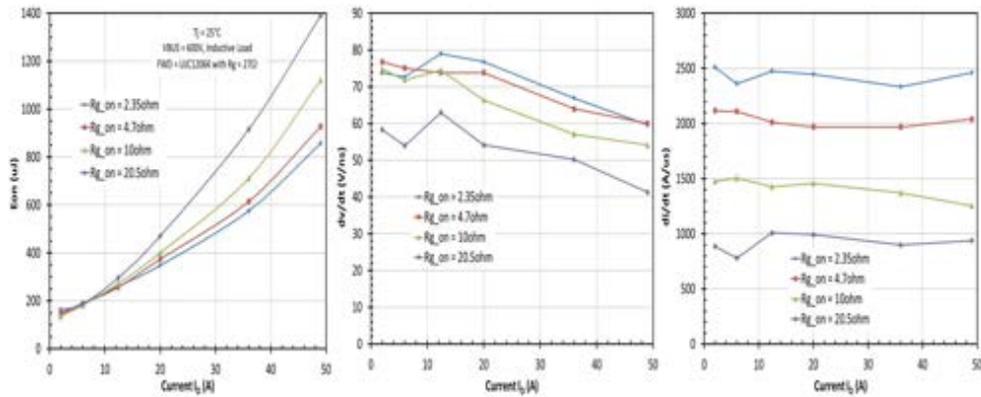
Figure 4.   Controlling dV/dt and di/dt with gate resistance

Figure 5 gives a summary of the relative characteristics of the WBG technologies with respect to each other and traditional Si superjunction MOSFETs.

| Technology	SiC Cascode 650V-45mΩ (UJC6505K)	Commercial SiC MOSFET	Commercial GaN HEMT	Commercial Si Superjunction
R_{DSA}	0.75 mΩ-cm²	2-3 mΩ-cm²	3-7 mΩ-cm²	10 mΩ-cm²
Normalized Die Area	1	2.6X	4X	13X
E_{OSS}	7.5 μJ	32 μJ	12 μJ	14 μJ
Avalanche Capability	YES	YES	NO	YES
Short Circuit	YES	YES	NO	YES

Figure 5.   Indication of relative die sizes for different technologies

Cascodes "drop in" to existing slots

The headline advantages of WBG devices are often seen as speed and high-temperature operation with multi-megahertz and >200°C junction temperatures being quoted, promising dramatic reductions in size and cost with increased efficiency. This is surely possible with a ground-up redesign with new magnetics, resonant topologies and RF-style layouts. Perhaps the best example is Google's and the IEEE's "Little Box Challenge" to design a 95% efficient converter with

50W/cu-in power density, ten times smaller than the state-of-the-art versions at the time. The winner achieved better than 145W/cu-in using WBG technology.

However, there is a vast market for upgrading existing equipment where total redesign is neither feasible nor economical. Most WBG switch solutions are a poor match for designed-in components such as IGBTs or Si-MOSFETs; the gate-drive systems for these components are incompatible with the precise gate-drive voltages needed for say, SiC-MOSFET or GaN HEMT devices. However, cascode SiC JFETs can drop right in. They are available in the traditional TO-247 and TO-220 case styles and can accept a wide range of gate-drive voltages, encompassing every other device standard (**Figure 6**). Some cascodes also include a gate-clamping diode to protect from overvoltage and ESD. Gates of IGBTs and Si-MOSFETs in existing systems are often directly driven through a transformer with inexact voltages, varying with duty cycle. Again, the wide tolerance of the gate voltage drive to SiC cascodes makes substitution easy.
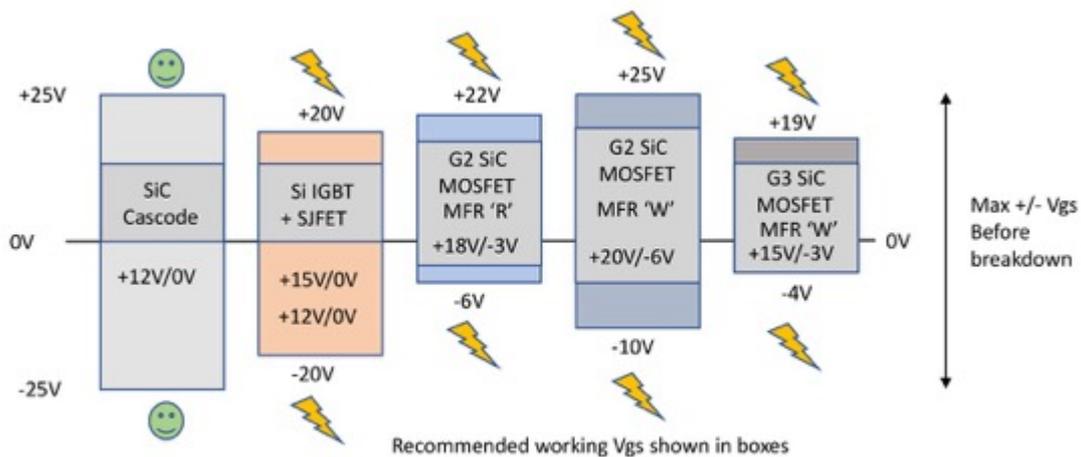
Figure 6.   **SiC cascodes encompass other allowable gate-drive voltage ranges**

The cascode can be slowed down with a choice of gate resistors to match the existing design while dramatically reducing energy loss in the body diode, compared with Si-MOSFETs and IGBTS with an external fast-recovery diode.

System stability and potential speed are improved, with the Miller effect practically absent, and gate-drive power is much reduced. As an example, if a SiC cascode from UnitedSiC-type UJC1210K 800V/20A is compared with an IGBT-type IRG7PH35UD 600V/25A, the total gate charge $Q_{G(total)}$ of the cascode is 47.5nC and that of the IGBT 85nC. This may not seem to be a huge difference, but the cascode can be switched with 0V/12V on its gate while the IGBT may need -9V/+15V. Gate-drive power requirement P_G is given by:

$$P_G = Q_{G(total)} \cdot F \cdot V_{SW}$$

where F is the operating frequency and V_{SW} is the total gate voltage swing, which for the IGBT is twice the cascode value. Total power required is therefore about a quarter with the cascode. Note that the power is constant at any duty cycle as long as the gate is fully charged and discharged each switching period.

SiC cascodes can therefore be dropped into many applications using IGBTs, Si-MOSFETs or even SiC-MOSFETs with little more than a change in series gate resistor value to optimize switching speed. A typical gate-drive circuit for SiC cascodes is given in **Figure 7**. Note that unusually, $R_{(on)}$ is typically lower than $R_{(off)}$, which should have a minimum value of about 10 ohms to avoid internal oscillation in the cascode. The series ferrite bead is optional for damping.
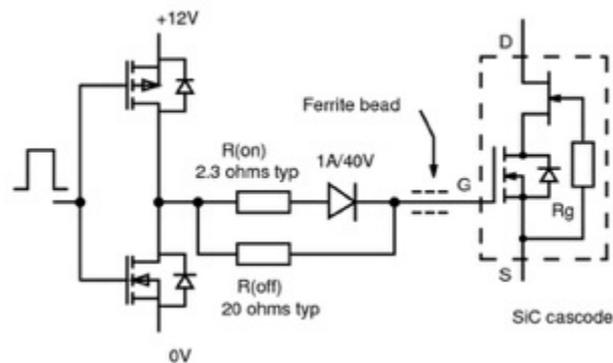
Figure 7.   Typical SiC-cascode gate-drive circuit

SiC vs GaN

Coming later than SiC, GaN has had slow adoption due to cost, yield and reliability concerns. It is certainly theoretically capable of higher switching speed than SiC or Si, with its much higher electron mobility, but with a thermal conductivity lower than SiC by a factor of three, its power density potential is limited. Currently SiC devices are common at around 650V through 1.2kV rating and higher, while GaN is limited to around 650V, where it struggles to compete with the current lower cost and proven robustness of the more mature SiC offering at the same voltage. GaN suppliers are hoping that the lower voltage/power market including data centers, EV/HEV and photovoltaics will open up as the hoped-for cost savings materialize. However SiC cascodes also address these market areas, especially in applications for bi-directional DC-DC converters and totem-pole PFC (see below). Data from IHS [1] shows the relative split in usage remaining similar up to the mid-2020s, with the combined WBG market reaching $3.5B, of which GaN is still only about $500M.

SiC is well established in the supply chain now, with parts available in the catalogs of high-service distributors.

SiC trench cascodes have a natural advantage over GaN and indeed Si-MOSFETs and SiC-MOSFETs in that their figure of merit R_{DSA} is much better (**Figure 8**). R_{DSA} is a measure of what combination of ON-resistance is achieved in a particular die area, and if you compare the same power levels across the devices, SiC cascodes for example are 5–10 times better than GaN. In other words, the die size can be 5–10 times smaller, giving lower capacitances and more die per wafer with the associated cost savings. There is less area for heat transfer but SiC has a thermal conductivity three times better than GaN, and anyway tolerates junction temperatures up to 250°C with little variation in characteristics.

Device	SiC Cascode UJC06505K	SiC MOSFET SCT3120KL	E-mode GaN GS66508B	Si Superjunction IPP65R045C7
R_{DSA} mohm-cm^2	0.75	3.5	6.6	10
Rds*Eoss mohm-uJ	255	600	350	462
Vth (V)	5	4.5	1.3	3.5
Avalanche	Yes	Yes	No	Yes
Gate voltage rating (V)	+/-25	+22/-4	+/-10	+/-20
Diode behavior	Excellent	Excellent	Excellent	Poor

Figure 8.   Comparative figures of merit

Perhaps a factor that gives SiC an edge in industrial systems, even if GaN voltage ratings improve to compete, is the ability of SiC to withstand voltage avalanche conditions, as can happen with inductive loads. Manufacturers have extensive data showing SiC reliability overvoltage overstress, whereas GaN makes no claims except to say maximum voltage should not be exceeded otherwise damage will occur.

A more tangible difference between the devices is the packaging available; SiC parts are commonly available in TO-247 and T0-220 styles, allowing them to drop in as replacements for MOSFETs and IGBTs in existing designs, giving immediate advantages. Various standard surface mount options are under development. However, GaN device manufacturers have recognized that leaded packages with their inherent speed-limiting connection inductances would be a barrier to getting the best potential performance from their parts. They have therefore mostly opted for surface-mount, single-source, chip-scale packaging, which limits their adoption to new designs. Here, the system design can be matched to the

GaN device properties to give smaller passive components, particularly magnetics and capacitors.

Where we are today

SiC cascodes are commonly available with 650V and 1200V ratings at currents up to around 85A with ON-resistances of around 30 milliohms. "Super cascodes" are also available – series-connected JFETs with greater than 3.5kV rating. SiC-MOSFETs up to 1700V at around 70A and 45 milliohms are available, but their internal body diode is relatively slow, unlike with cascodes, and often has to be bypassed with a costly, fast SiC external diode when the application requires it, for example in hard-switched bridge circuits.

GaN devices top out at 650V with about 60A and 25 milliohms rating, equivalent to many SiC parts but theoretically capable of faster switching. Interestingly, available GaN devices at 100V rating are no better than traditional Si-MOSFETs for ON-resistance and therefore rely on their speed advantage to counter the significant cost added over commodity MOSFETs at this level.

For the future, the IHS data clearly shows a significant increase in WBG device design-ins, although IGBT and traditional MOSFET sales will also increase in a growing market. The debate is how the different WBG devices might dominate particular market segments. **Figure 9** is one view of the possible future split in power and operating frequency for power devices, although the GaN presence again depends on prospective cost reductions.
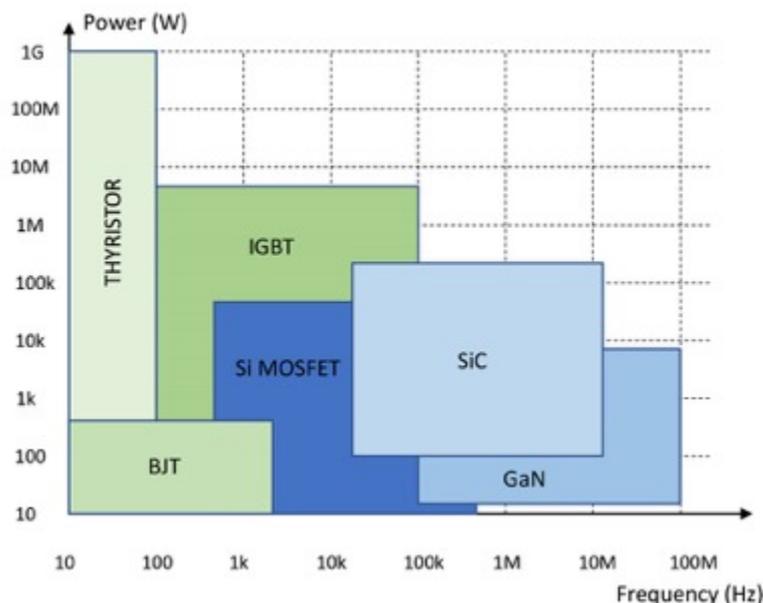
Figure 9.   A possible future scenario
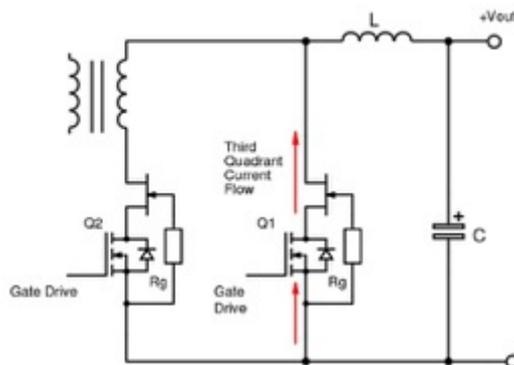
The applications

The high temperature capability of WBG devices with potentially fast switching and low losses makes them ideal for military and industrial applications where performance is key. Bridge circuits are an obvious candidate used at high power for inverters, welding, class D audio amplifiers, motor drives and more. A particular application where major benefits are seen is the bridgeless totem-pole PFC circuit. (**Figure 10**). Here, previous circuits using Si technology have been limited by the slow performance of body diodes in the MOSFETs typically used. A parallel SiC diode helps, but defeats the object of reducing component count. This forces "critical conduction" mode to be used, which sets switching current to zero at the end of each conduction period. However, this variable-frequency mode produces high peak currents and high EMI. Using cascode SiC JFETs, "continuous conduction" mode can be used, increasing efficiency, reducing inductor size and easing filtering and EMI problems with fixed operating frequency. An example circuit using UnitedSiC UJC06505K devices at 1.5kW and 230VAC-line showed an impressive efficiency of 99.4% [2].
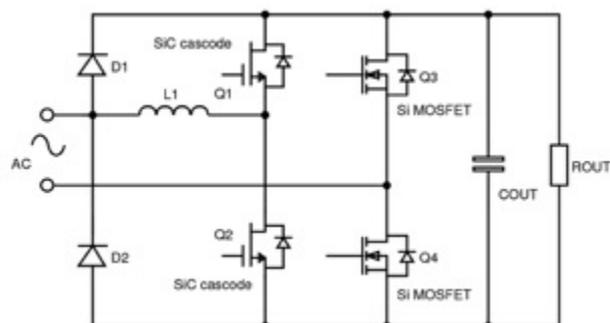
Figure 10.   SiC devices in a bridgeless totem-pole PFC stage

Achieving high efficiency in converter primary switches must be matched with similar improvements in rectification for DC outputs. Again, SiC cascodes fit here as they can be configured for "synchronous rectification" (**Figure 11**). In so-called third-quadrant operation current flows from source to drain of one or other of the cascodes through the output inductor to load during the "forward" and "flywheel" periods of forward or buck-derived converters. Current flow through the body diode sets the JFET gate-source voltage to approximately +0.7V, turning it naturally hard ON. If the cascode gate is set high, the internal Si-MOSFET channel conducts and the total ON-resistance becomes the $R_{DS(on)}$ of the cascode,

giving low conduction losses. Q1 forms the flywheel rectifier and Q2 the forward rectifier.

Figure 11.   SiC cascodes in synchronous rectification

Robustness concerns

In high-power applications, robustness with transient short-circuits and overvoltages is a major concern. A typical cascode SiC JFET has excellent characteristics in this respect. The pinch-off effect has already been mentioned, limiting saturation current with its negative temperature coefficient.

For overvoltages, the SiC JFET gate-drain diode conducts, causing current flow in the built-in gate resistor and turning the JFET channel ON to clamp the overvoltage. Again, the inherent high temperature rating of the SiC die gives a good margin of safety for significant avalanche energy levels even in the relatively small die sizes encountered. As an additional confidence measure, all parts are subjected to 100% avalanche at final test [3].

References

1. https://technology.ihs.com/521146/sic-gan-power-semiconductors-2016
2. http://unitedsic.com/wp-content/uploads/2016/11/Totem-Pole-PFC-AppNotes.pdf
3. http://unitedsic.com/wp-content/uploads/2016/02/bp_2015_05-Robustness-of-SiC-JFETs.pdf

For more information, visit: http://www.unitedsic.com