Circuit protection with SiC FETs in dual-gate configuration

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ABSTRACT

Interest in solid-state circuit breakers and solid-state power controllers has grown rapidly in recent years[1]. SiC JFETs have long been considered ideal devices for this application[2], given their ability to have low on-state resistance at high voltage ratings, without compromising their ability to limit current when needed. In this white paper, we examine the use of normally-off SiC FETs in a dual-gate configuration to simplify the development of high current DC and AC circuit breakers.

WHITE PAPER

A great deal of research has been conducted into the benefits of solid-state circuit breakers, which fall broadly into the classes of hybrid breakers and completely solid-state breakers with no mechanical parts. This article focuses on solid-state circuit breakers. Table 1 presents an overview of the relative advantages and disadvantages of solid-state circuit breakers when compared to established electromechanical breakers and relays. The key benefit of solid-state breakers is known to be their ability to interrupt current on a nano/microsecond scale, rather than the milli-second scale needed with mechanical breakers. This becomes increasingly valuable when interrupting power sources with very low internal impedance, for e.g., EV batteries. They can also be used to interrupt DC circuits, without the need for elaborate arc prevention measures. The absence of moving parts and degradation of contacts allows many more cycles of fault prevention without the need for replacement in the field. However, solid-state circuit breakers do have higher resistance than mechanical contacts, making their cost/A significantly higher. As the voltage rating of the semiconductors increase, the resistance increases as the V^2 or $V^{2.5}$ for the same area of material used (for basic unipolar devices). This directly impacts the cost as the voltage class of the breaker increases.

Feature	Solid state (Si, SJ, SiC, IGBT, IGCT)	Electromechanical
Full controllability	★★★★★	★★★
High speed	★★★★★	★★
Conduction loss	★★	★★★★★
No arcing	★★★★★	★★
Use cycles: no maintenance	★★★★★	★★
Cost per amp	★★	★★★★★
Voltage rating vs. on Rds(on)	★★★	★★★★★

Table 1: Comparing features of solid-state breakers and electromechanical breakers

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Why SiC for circuit protection

The main function of a solid-state protection circuit is to carry current in the on-state with minimal resistive loss, and to be able to interrupt this current when commanded to do so by the system controller. At low voltages <600 V, silicon MOSFETs offer low resistance, and are a cost-effective option for building circuit breakers, relays and E-fuses, and are already used as such in 48V battery systems. Once the needed voltage exceeds 600 V, the resistance of even advanced silicon technologies like superjunction (SJ) MOSFETs becomes too high. IGBTs, while able to provide very low differential resistance, have a knee in their conduction characteristics, making the power loss during conduction excessive, which in turn leads to the need for more heat removal. At voltages >3000 V, IGCTs have been used to implement breakers.

Figure 1 shows the specific on-resistance of silicon SJ MOSFETs, GaN FETs, SiC MOSFETs, and SiC-JFET based SiC FETs. It should be clear that in a wide voltage class from 600 to 2000 V, SiC FETs offer the lowest resistance per unit area. This allows the development of the lowest conduction loss, most compact and cost-effective solid-state breakers. They can be very useful in applications where there are constraints in heat removal. All SiC devices are also able to tolerate high instantaneous temperature rise (e.g., during short circuit events), which can be useful in handling 4X as much energy per unit area as a silicon device. This is because the wide bandgap results in a much higher temperature needed to thermally generate sufficient carriers to degrade the voltage blocking capability of the switch. The 3X higher thermal conductivity of 4H-SiC allows effective heat spreading compared to GaN or Si based options, allowing operation at higher current densities.

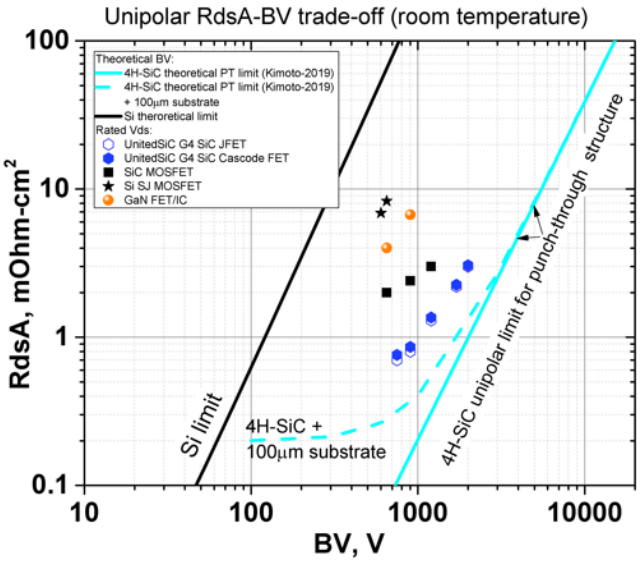

Figure 1: Comparing specific-on resistance vs voltage for various semiconductors

Major applications for SiC-based circuit protection

Given the generally higher cost of solid-state circuit protection, it is likely to be used where the speed, controllability, reliability, and weight reduction features are more important than the cost premium. This is typical of a new technology, and with the reduction in cost that invariably occurs as technology (especially SiC) matures and scales, the application space expands.

Given the rapid growth of DC sources (solar, EV batteries, energy storage etc.) and DC loads, one area where SiC based breakers needing 750 V – 1200 V FETs being examined are DC breakers. For applications in EVs, ships, aircraft, where very low conduction losses are needed, and arc-flash poses a safety concern, solid-state breakers are a good solution. The ability of the solid-state solution to rapidly interrupt short circuit events before currents can rise to >5 kA or 10 kA is valuable. Faster co-ordination is possible between the main breaker and downstream breakers in the protection hierarchy.

High power AC breakers can also benefit from the use of solid-state solutions, largely because the on-resistance now possible with 1200 V SiC FETs rivals a mechanical contact, and the overall solution makes field maintenance much easier. Improved capabilities stemming from the fast current interrupt and inrush current limiting directly by the solid-state switch add further value.

AC breakers in the residential space can utilize the un-paralleled low conduction losses of SiC devices, to implement smart solutions for energy management in emerging environments with solar panels, energy storage, and EVs on top of traditional loads. Minimal heat generation allows for cost effective breaker panels, not requiring any fans for cooling.

In addition to solid-state breakers, the same devices have been used to construct solid state power controllers, which regulate the managed flow of power between multiple generation sources and loads on ships and aircraft. Inrush currents are managed effectively, as are fault currents.

Solid-state breakers can play a role in railway traction, in better managing faster fault response between the catenary and system power electronics. This can help reduce the size of the downstream power electronics, and its weight and cost. The system reliability and longevity benefit.

In a range of emerging applications, SiC JFETs are employed as bi-directional current limiting switches, self-powered breakers, and super-cascode HV breakers[4,5,6,7].

When it comes to functional safety, in applications where it is beneficial for the transistor to stay on even if gate power is lost, the normally-on SiC JFET is a useful device. Consider a full-bridge rectifier that uses normally-off devices on the high side, and normally-on JFETs on the low side. Such a bridge still presents as normally-off to the input side, but since the low side JFETs can short the output when both are on, they serve as a shunt when control power is lost. The same methodology can improve the design of motor drive inverters, where simply using normally-on devices as low side FETs can simplify managing functional safety.

In all the aforementioned areas, the ability of the solid-state solution to monitor its health and allow easily scheduled maintenance rather than repair after failure is a significant benefit, and the dual-gate SiC FET will be shown to provide the best option in this regard.

JFET, SiC FET and dual-gate SiC FET structures

Figure 2 compares the basic structure of the SiC MOSFET and SiC JFET. The lower on-resistance per unit area for SiC JFET shown in Figure 1 stems from the absence of the low mobility channel, and the absence of the need to protect the gate oxide from a high field with additional shielding that adds to on-resistance. The JFET however, is a normally-on device, and to form a normally-off option, a low voltage Silicon MOSFET can be connected in series with the SiC JFET in a cascode configuration, as shown in figure 2, which can add 5 – 15% to the $R_{DS(on)}$. The series connected device can be configured either as a basic cascode, referred to as a SiC FET, or a dual-gate device where both the gates of the LVMOS and SiC JFET are externally accessible.

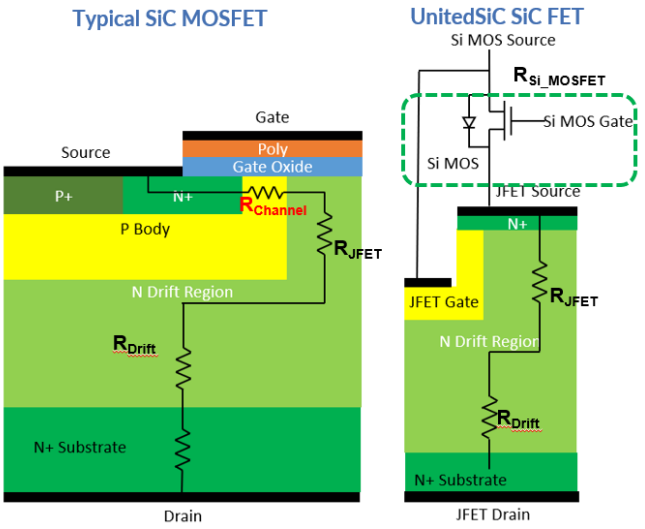

Figure 2: Resistance difference between SiC MOSFETs and SiC FETs resulting from the low channel resistance in JFETs

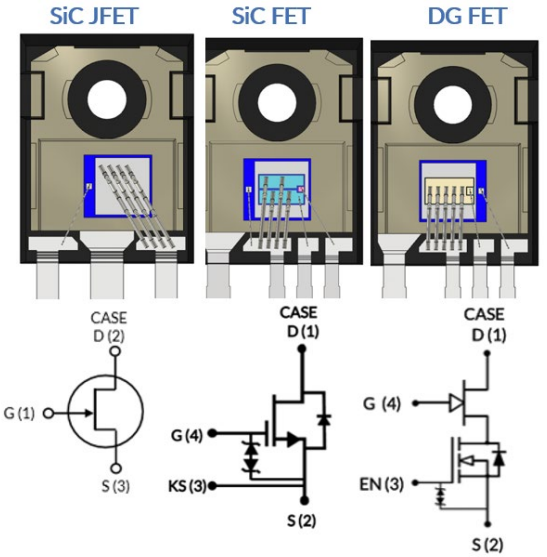

Figure 3: Structures of SiC JFET based devices

In figure 3, the leftmost image shows a SiC JFET packaged in a TO-247 package like a traditional MOSFET. The center image shows how the SiC FET cascode structure is formed by stacking the low voltage MOSFET on the source pad of the high voltage SiC JFET die. The gate of the SiC JFET is connected to the LV MOSFET source within the package, completing the cascode connection. This device can be used like a normally-off MOSFET. The rightmost image shows how both the MOSFET and JFET gates can be brought out for user control in the same TO-247-4L package. This is referred to as a dual-gate FET (DG FET). In the example shown, the 1200 V JFET has a resistance of 7 mΩ at V_{GS} = 2 V, and 8 mΩ at V_{GS} = 0 V. In the SiC FET, the JFET operates with V_{GS} close to 0 V in the on-state. The resistance is 9 mΩ, with 1 mΩ added by the LV MOSFET. In the rightmost dual-gate device, in the on-state, the MOSFET is on, and since the JFET can be operated with the gate at 2 to 2.5 V, its resistance drops to 7 mΩ, and the composite device resistance drops to 8 mΩ. This on-state behaviour is shown in figure 4.

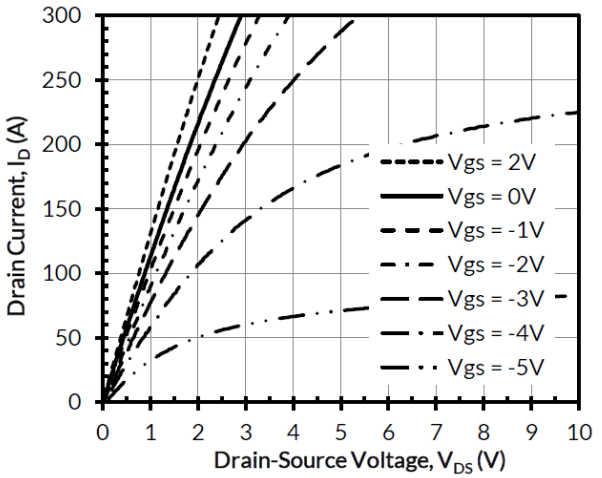

Figure 4: Lower resistance with V_{GS} = 2 V vs. V_{GS} = 0 V, can be exploited in the 1200 V dual-gate FET

Figure 5 shows the behaviour of the V_{GS} of the JFET as a function of temperature at 1 mA, which amounts to sensing the knee voltage of the gate-source SiC PN junction. This voltage can be sensed by the gate drive circuit while the device is on, to determine the T_J directly. This method of sensing T_J is far more accurate than sensing $V_{DS(on)} = (I_D \cdot R_{DS(on)})$. The low current knee voltage varies very little between devices, since it is not influenced by many of the process factors that cause $R_{DS(on)}$ to vary. It is also superior to integrating temperature sense diodes in the SiC chip, in speed and accuracy. Finally, sensing temperature using an NTC in a power module and/or the T_J of a control IC does not offer anywhere near the needed response speed or accuracy of this JFET V_{GS} sense method.

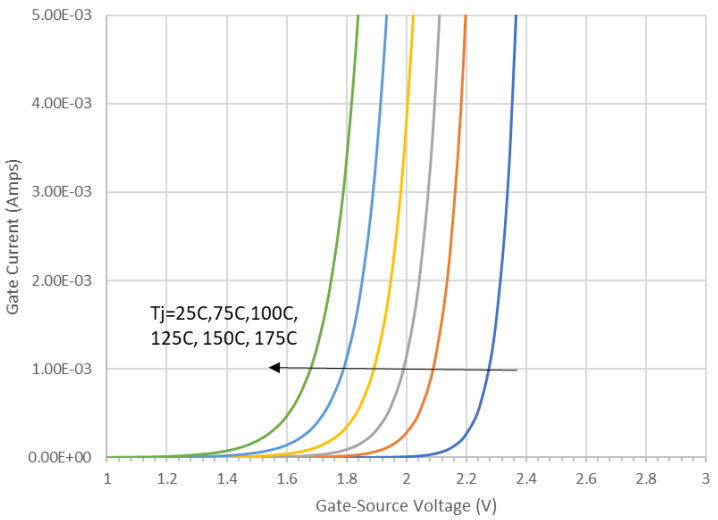

Figure 5: Using the on-state V_{GS} of the SiC JFET to montior its junction temperature

Changes in the JFET T_J during known operating conditions can be compared to a reference to check aging of the device during normal operation. An excessive increase in T_J can flag imminent end of life and allow replacement before catastrophic failure. Since the T_J response speed is accurate on a microsecond scale, temperature rise in the chips can also be monitored during transient events, such as when the breaker is activated, to allow shutdown before the switch is damaged.

In a simple 4 terminal DG FET, the on-state drop in the low voltage FET adds to the V_{GS} measured externally and must be corrected for to extract the junction temperature. In packages with higher pin counts, the JFET source potential can be directly accessed to improve precision of the extracted T_J. Alternatively, the DG FET can be implemented as two discretes, with an ultra-low $R_{DS(on)}$ logic level SMT discrete FET, and this provides direct access to the JFET gate and source.

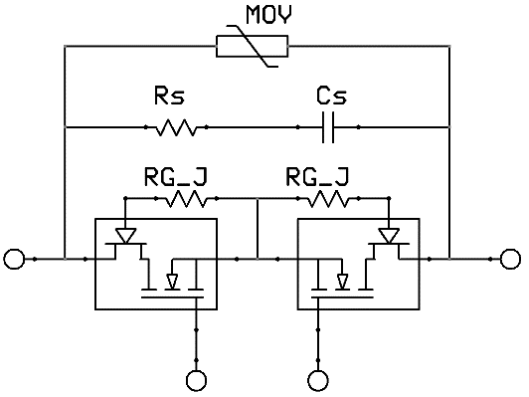

Figure 6: Circuit architecture of a solid-state circuit breaker (power elements)

Solid-state circuit breaker

A common circuit implementation of a solid-state circuit breaker is shown in figure 6. Two switches are connected in a common source configuration, to provide bidirectional voltage blocking and current flow. RC snubbers (Rs, Cs) are used across individual FETs or the FET pair. A transient voltage suppression device (MOV, TVS) is placed across the transistors to absorb inductive energy from the line and load inductance when the current is cut off. This architecture can be used to cover a wide range of applications. For example, in E-mobility applications, this circuit can be used to replace the DC disconnect switch. Since all the battery power is routed through the solid-state switches, sub-mΩ resistances are needed for breakers rated at 500 - 1500 A, 1200 V. This requires the use of many devices in parallel, and the task is simplified by using ultra-low $R_{DS(on)}$ devices.

Figure 7 shows an experimental setup used to demonstrate the ability to parallel the dual-gate SiC FETs and interrupt large fault currents. Three TO247-4L devices, each 9 mΩ, 1200 V are paralleled, for a switch resistance of 3 mΩ.

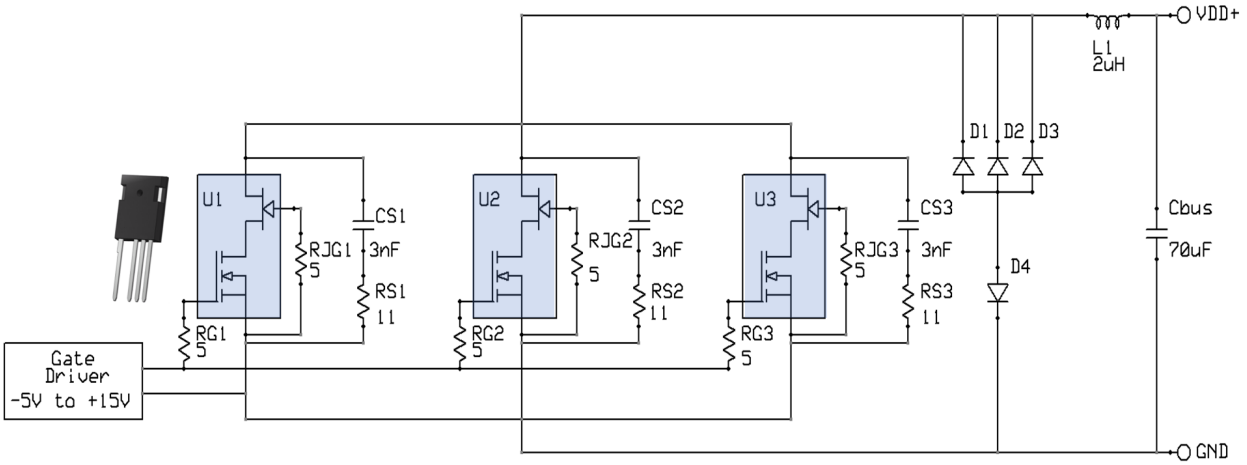

Figure 7: Schematic of a solid-state circuit breaker test circuit where the switch is formed by paralleling three dual-gate SiC FETs. The SiC schottky diodes D1-D4 are used as the TVS (instead of a MOV) to protect the switch during turn-off transient.

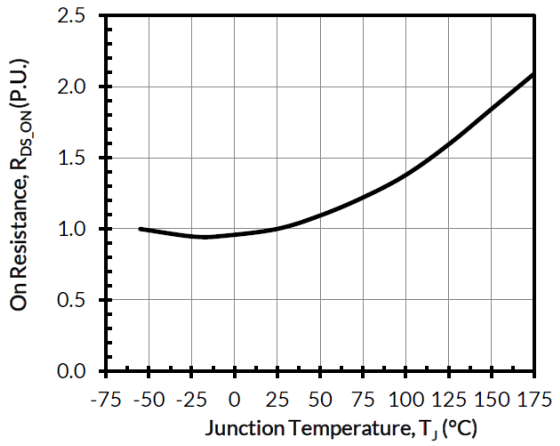

Figure 8: Temperature dependence of $R_{DS(on)}$ in the 1200 V dual-gate device

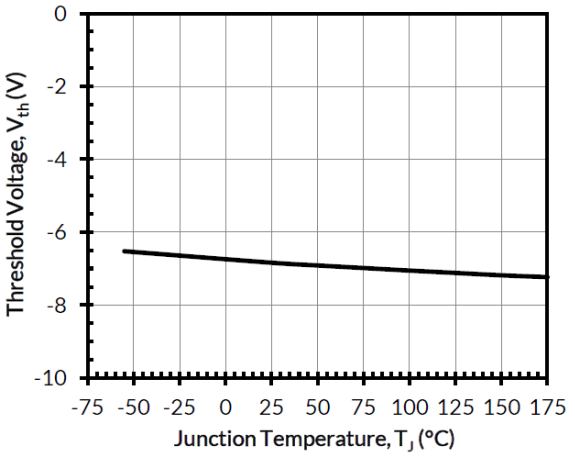

Figure 9: Temperature dependence of V_{th} in the 1200 V dual-gate device

The positive temperature coefficient of the device on-resistance, shown in figure 8, ensures good current sharing when the devices are on. The devices are operated with a standard MOSFET like gate drive -5 to 15 V in this test, but a unipolar gate drive 0 to 12 V may also be used. A 5 Ω resistor is provided at each of the MOSFET and JFET gates to assist parallel operation during switching. The 5 Ω JFET R_G slows down the switch turn-off. Since this resistance is much larger than the intrinsic gate resistance of the JFET, it helps to set the turn-off speed for the cascode and keep the switching behavior matched for the three paralleled devices. An individual RC snubber is placed across each device since this configuration minimizes the stray inductance that would otherwise exist between the snubber and the switches. The mild variation of JFET V_{th} with temperature (figure 9), is also important for ensuring excellent current sharing during the switching transient.

Figure 10 shows the measured turn-off behavior for the 3 paralleled FETs. The bus voltage is 400 V, the TVS clamp is created using 200 A, 650 V SiC Schottky diodes that can absorb the avalanche energy of the 2 µH inductance used to simulate the line inductance. At 1000 A, this energy is 1 J, so three such diodes are used in parallel to provide adequate margin. The gate pulse V_{GS} is used to ramp the current to 1150 A in 10 µs, and then turned off. Since current in the 2 µH inductor persists, the device voltage flies up at a rate determined by the switching speed (set by R_G of the JFET in this case), and the snubbers used. Once it reaches the clamp voltage set by the TVS diode breakdown, the current transfers to the TVS diodes. With this arrangement, the three TO-247 devices can smoothly turn off 1150 A as shown in figure 10. Note that the current in the SiC FETs is interrupted in <500 ns and transferred to the avalanching TVS array. The 5 µs duration for the current to return to zero is set by the peak current, and the downward slope is set by $BV_{(TVS)}/L1$. The short voltage spike in the V_{DS} waveform is a result of the relatively fast di/dt of the switch turn-off and the stray inductance between the devices and TVS diodes. This can be further moderated by slowing turn-off speed and/or adjusting the RC snubber.

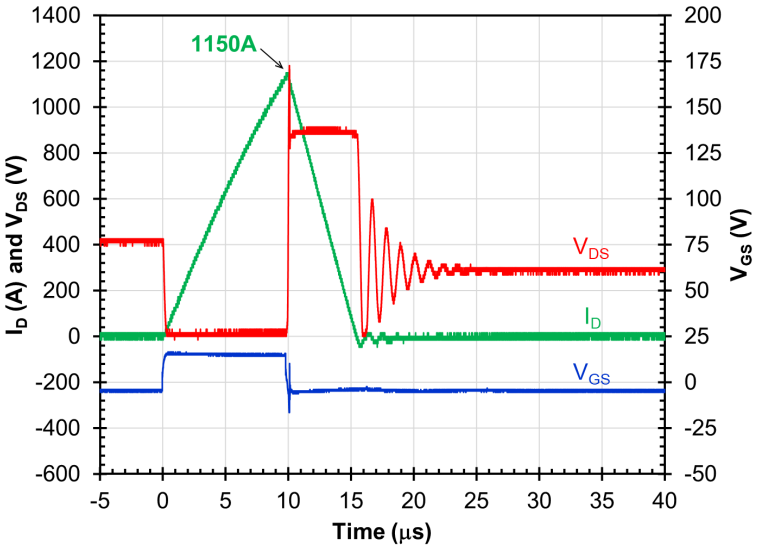

Figure 10: Measured turn-off transient waveforms at 1150 A of three paralleled 1200 V dual-gate devices in the test circuit as shown in Figure 7. The TVS clamp voltage is about 900 V.

Figure 11 extends the study of the suitability of dual-gate devices to a 2 mΩ, 1200 V module in a SOT-227 footprint, within which six such devices are used in parallel. A single 22 Ω resistor is used to slow the cascode switching, and the device is provided with an 11 Ω, 20 nF snubber. To facilitate higher current testing, the line inductor is reduced to 0.4 µH, and five paralleled 200 A, 650 V diodes are used as the TVS. Figure 12 shows the resulting waveforms from the test, when the module is used to interrupt a 1950 A peak current. The voltage spike in the V_{DS} waveform was eliminated by adjusting the JFET turn-off with the 22 Ω resistor and using a larger RC snubber.

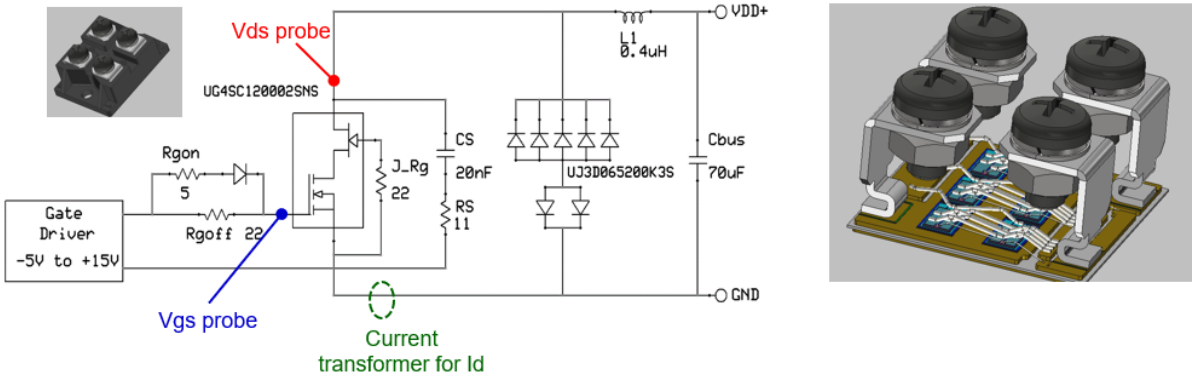

Figure 11: Schematic of a solid-state circuit breaker test circuit where the switch is formed using a dual-gate module in SOT-227 footprint with six 9 mΩ, 1200 V devices in parallel. Including package parastics, this forms a 2.2 mΩ, 1200 V device rated at >300 A.

Commercial aspects

A complete implementation of a solid-state circuit breaker would, of course, use two such switches connected in common-source configuration. And for higher currents, modules with more paralleled devices are being developed. While these examples show the use of the dual-gate device in cascode from, driven by standard silicon MOSFET/IGBT gate drivers, the more sophisticated implementation would drive the gate of the SiC JFET directly, by using the low voltage MOSFET as an enable switch. This would enable the lowest conduction loss for the SIC JFETs and as well as the junction temperature sense capability. Current sensing LV MOSFETs stacked atop the JFETs can eliminate the need for expensive external current sense methods.

SiC transistors can handle a great deal of avalanche energy, up to 4X that of a given area of silicon. However, as the line inductance and currents scale up, it becomes prohibitive to absorb all the avalanche stress in the SiC devices, which leads to the use of paralleled MOV devices. The cost of a solid-state breaker solution will therefore depend on the cost of the SiC switches and MOV used. MOVs are far more resistive in their clamping characteristics, so peak voltages will be much higher than with the SiC TVS diodes used in these demonstrations. The MOV sized to keep the peak voltage below the rated breakdown for the SiC devices will necessarily be larger if the voltage rating of the SiC components is reduced. In the examples shown in this paper, with a bus voltage in the 400 – 600 V range, a MOV that keeps the peak voltage below 1200 V for the worst-case turn-off current allows the use of 1200 V SiC devices. In theory, a lower cost MOV that allows peak voltages of 1500 – 1700 V would require the use of 1700 V devices, and that could drive up the cost of the SiC solution by nearly 2X. In other words, there is a direct trade-off between SiC cost and the MOV cost and size, scaling up with the worst-case energy the breaker must absorb. Final volume and weight considerations limit the breaker size in some applications, leading to the need for high voltage rated, more expensive SiC breakers.

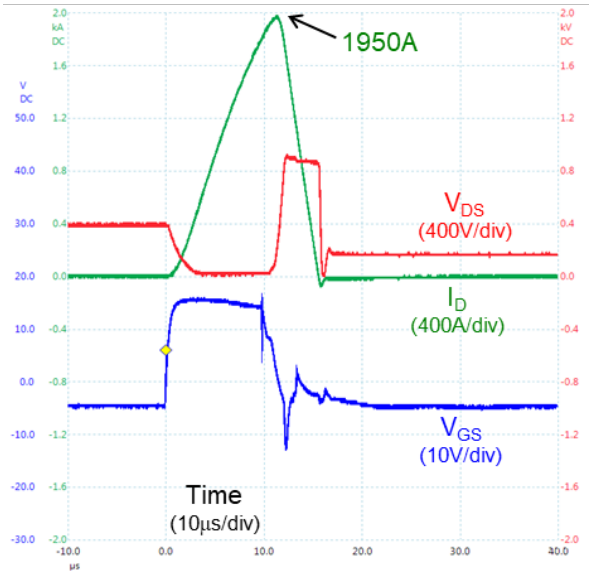

Figure 12: Measured turn-off transient waveforms at 1950 A of a 1200 V dual-gate module in the test circuit as shown in Figure 11. The TVS clamp voltage is about 900 V.

The cost of SiC devices is being rapidly reduced as adoption has increased, and market projections are largely focused on the possible growth of the EV segment for SiC devices. Volume-driven efficiencies are expected to halve SiC wafer costs in the next few years. Technology enhancements projected for SiC JFET technology will bring steady reductions in $R_{DS}A$, and drive costs to new lows in conjunction with volume efficiencies. These factors are shown in figure 13, alongside the projected SiC revenue growth (source: IHS Markit). Most current projections do not factor in the possible impact of large-scale adoption of solid-state breakers, presumably due to the cost differential with respect to electromechanical options. The use of solid-state breakers in EVs alone could double the projected market size, if indeed all the battery power is routed through solid-state circuit breakers. Extending this logic to other application spaces discussed in Section 3, if even a fraction of the generated and used DC power is routed through solid-state breakers and controllers, the market potential can be several times what is envisaged in figure 13.

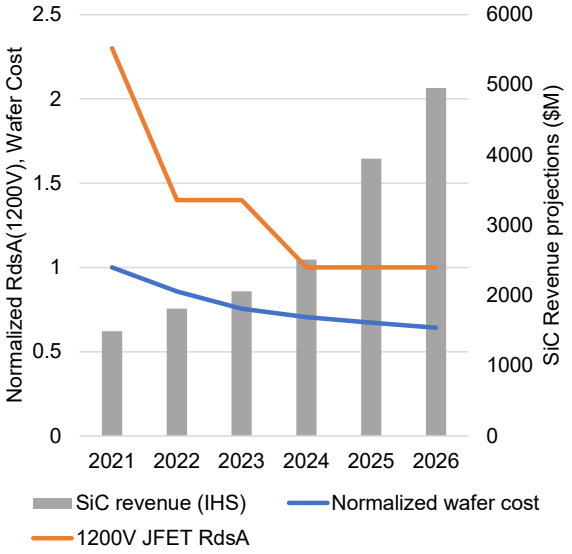

Figure 13: Projected SiC revenue growth, and evolution of SiC wafer costs and technology improvements ($R_{DS}A$ reduction). Solid-state breakers could well double the SiC market in the second half of the decade.

Conclusion

Solid-state breakers using semiconductors in the 600 – 1200 V class may be approaching a tipping point in their adoption. SiC devices are especially well suited in this voltage class, given the low $R_{DS}A$ they can provide, and SiC JFET based solutions have been shown to excel in this regard. The growth of the overall SiC market in EVs and other applications is creating a beneficial cycle driving down costs. Technology development is reducing $R_{DS}A$ rapidly for SiC FETs, and this trend is set to continue in the next few years, leading to 2X – 3X further reductions in $R_{DS}A$. These self-reinforcing trends will drive improved cost-performance and the consequent uptake of solid-state circuit breakers. Understanding and exploiting all the system level advantages of solid-state breakers, as well the ability of these devices to provide metrology to help monitor their degradation, coupled with the trends now apparent in Industry 4.0, indicates that a major transformation in solid-state circuit protection can soon come to pass.

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