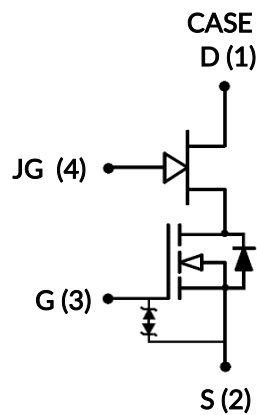
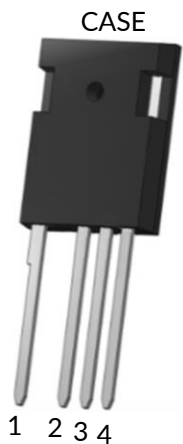


DATASHEET

UG4SC075009K4S



750V-8.4mΩ Combo-FET

(SiC JFET w/ Si MOSFET)

Rev. B, May 2024

Description

Qorvo's UG4SC075009K4S "Combo-FET" integrates both a 750V SiC JFET and a Low Voltage Si MOSFET into a single TO-247-4L package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

Features

- Single digit $R_{DS(on)}$
- Normally-off capability
- Improved speed control
- Improved parallel device operation (3+ FETs)
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- Short circuit rated

Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High power switch mode converters (>25kW)

Part Number	Package	Marking
UG4C075009K4S	TO-247-4L	UG4SC075009K4S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750V	V
JFET Gate (JG) to source voltage	V_{JGS}	DC	-30 to +3	V
		AC ¹	-30 to +30	V
MOSFET Gate (G) to source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ²	I_D	$T_C < 61^\circ\text{C}$	106	A
		$T_C = 100^\circ\text{C}$	86	A
Pulsed drain current ³	I_{DM}	$T_C = 25^\circ\text{C}$	344	A
Single pulsed avalanche energy ⁴	E_{AS}	L=15mH, $I_{AS} = 5.2\text{A}$	202	mJ
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	375	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering,	T_L		250	$^\circ\text{C}$

1. +30V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.

2. Limited by bondwires

3. Pulse width t_p limited by $T_{J,max}$

4. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.31	0.40	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ and $V_{JGS} = 0\text{V}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=V_{JGS}=0\text{V}$, $I_D=1\text{mA}$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750\text{V}$, $V_{GS}=0\text{V}$, $V_{JGS}=0\text{V}$, $T_J=25^\circ\text{C}$		4	84	μA
		$V_{DS}=750\text{V}$, $V_{GS}=0\text{V}$, $V_{JGS}=0\text{V}$, $T_J=175^\circ\text{C}$		35		
Total JFET gate leakage current	I_{JGSS}	$V_{JGS}=-20\text{V}$, $V_{GS}=+12\text{V}$		0.1	65	μA
Total MOSFET gate leakage current	I_{GSS}	$V_{GS}=-20\text{V} / +20\text{V}$		2	20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12\text{V}$ $I_D=70\text{A}$	$V_{JGS}=2\text{V}$ $T_J=25^\circ\text{C}$	8.4		$\text{m}\Omega$
			$T_J=25^\circ\text{C}$	9	11.5	
			$T_J=125^\circ\text{C}$	14.8		
			$T_J=175^\circ\text{C}$	19.4		
JFET gate threshold voltage	$V_{JG(th)}$	$V_{DS}=5\text{V}$, $V_{GS}=12\text{V}$, $I_D=110\text{mA}$	-11.3	-9.3	-6.7	V
MOSFET gate threshold voltage	$V_{G(th)}$	$V_{DS}=5\text{V}$, $V_{JGS}=0\text{V}$, $I_D=10\text{mA}$	3.5	4.5	5.5	V
JFET gate resistance	R_{JG}	$f=1\text{MHz}$, open drain		0.8		Ω
MOSFET gate resistance	R_G	$f=1\text{MHz}$, open drain		2.3		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C < 61^\circ\text{C}$			106	A
Diode pulse current ²	$I_{S,pulse}$	$T_C = 25^\circ\text{C}$			344	A
Forward voltage	V_{FSD}	$V_{GS}=0\text{V}$, $V_{JGS}=0\text{V}$, $I_S=35\text{A}$, $T_J=25^\circ\text{C}$		1.10	1.24	V
		$V_{GS}=0\text{V}$, $V_{JGS}=0\text{V}$, $I_S=35\text{A}$, $T_J=175^\circ\text{C}$		1.14		
Reverse recovery charge	Q_{rr}	$V_{DS}=400\text{V}$, $I_S=70\text{A}$, $V_{GS}=V_{JGS}=0\text{V}$, $R_{JG}=0.7\Omega$		368		nC
Reverse recovery time	t_{rr}	$di/dt=4400\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$		31		ns
Reverse recovery charge	Q_{rr}	$V_{DS}=400\text{V}$, $I_S=70\text{A}$, $V_{GS}=V_{JGS}=0\text{V}$, $R_{JG}=0.7\Omega$		433		nC
Reverse recovery time	t_{rr}	$di/dt=4400\text{A}/\mu\text{s}$, $T_J=150^\circ\text{C}$		35		ns

Typical Performance - Dynamic with MOSFET gate as control terminal and $V_{GS}=0V$

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
MOSFET input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V,$ $V_{JGS}=0V, f=100kHz$		3340		pF
Output capacitance	C_{oss}			230		
Reverse transfer capacitance	C_{rss}			1.4		
Effective output capacitance, energy	$C_{oss(er)}$	$V_{DS}=0V$ to $400V,$ $V_{GS}=0V, V_{JGS}=0V$		286		pF
Effective output capacitance, time related	$C_{oss(tr)}$			605		pF
C_{OSS} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V,$ $V_{JGS}=0V$		23		μJ
Total Gate charge	Q_G	$V_{DS}=400V, I_D=70A,$ $V_{JGS}=0V,$ $V_{GS} = 0V$ to $15V$		75		nC
Gate-drain charge	Q_{GD}			13		
Gate-source charge	Q_{GS}			22		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6		26		ns
Rise time	t_r	$V_{DS}=400V, I_D=70A,$ $V_{GS}=0V$ to $+15V,$		21		
Turn-off delay time	$t_{d(off)}$	$R_{G_ON}=1\Omega, R_{G_OFF}=10\Omega,$		112		
Fall time	t_f	$R_{JG_ON}=0.7\Omega, R_{JG_OFF}=4.7\Omega,$		42.5		
Turn-on energy	E_{ON}	Inductive Load,		1135		μJ
Turn-off energy	E_{OFF}	FWD: same device with V_{GS} $= 0V, R_G = 10\Omega, V_{JGS}=0V,$		1013		
Total switching energy	E_{TOTAL}	$R_{JG}=0.7\Omega, T_J=25^\circ C$		2148		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6		24		ns
Rise time	t_r	$V_{DS}=400V, I_D=70A,$ $V_{GS}=0V$ to $+15V,$		25		
Turn-off delay time	$t_{d(off)}$	$R_{G_ON}=1\Omega, R_{G_OFF}=10\Omega,$		114		
Fall time	t_f	$R_{JG_ON}=0.7\Omega, R_{JG_OFF}=4.7\Omega,$		40		
Turn-on energy	E_{ON}	Inductive Load,		1170		μJ
Turn-off energy	E_{OFF}	FWD: same device with V_{GS} $= 0V, R_G = 10\Omega, V_{JGS}=0V,$		953		
Total switching energy	E_{TOTAL}	$R_{JG}=0.7\Omega, T_J=150^\circ C$		2123		

5. Measured with the half-bridge mode switching test circuit in Figure 23.

6. Devices are driven with the ClampDRIVE method as described in the section "Recommended Gate Drive Approach: ClampDRIVE method".

Typical Performance - Dynamic with JFET gate as control terminal and $V_{GS}=+12V$

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
JFET input capacitance	C_{Jiss}	$V_{DS}=400V$, $V_{JGS}=-20V$, $f=100kHz$		1965		pF
JFET output capacitance	C_{Joss}			226		
JFET reverse transfer capacitance	C_{Jrss}			222		
JFET total gate charge	Q_{JG}	$V_{DS}=400V$, $I_D=70A$, $V_{JGS} = -18V$ to $0V$		304		nC
JFET gate-drain charge	Q_{JGD}			159		
JFET gate-source charge	Q_{JGS}			50		

Typical Performance Diagrams - MOSFET gate as control terminal and $V_{JGS}=0V$

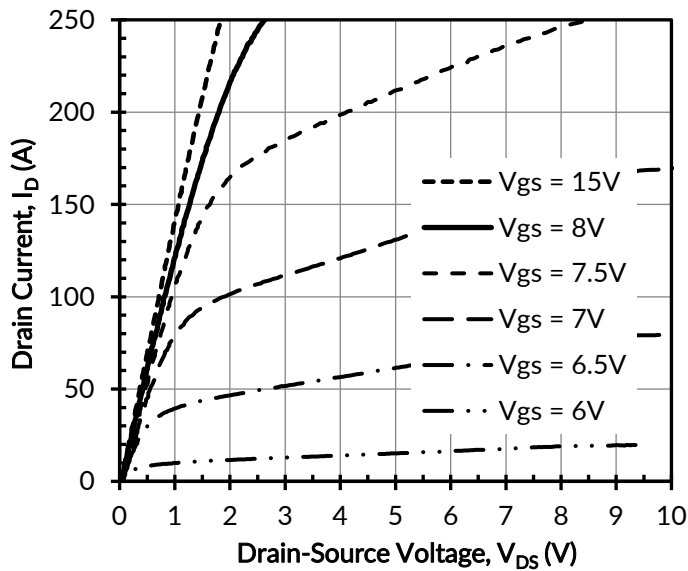


Figure 1. Typical output characteristics at $T_j = -55^\circ C$, $t_p < 250\mu s$

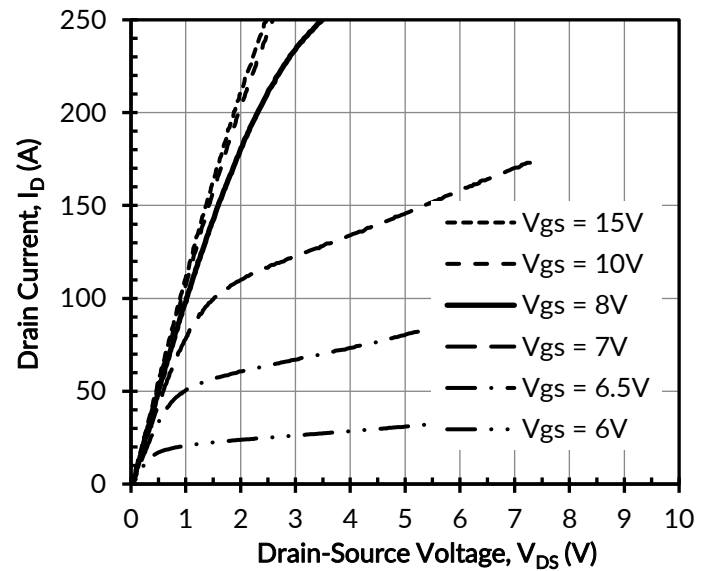


Figure 2. Typical output characteristics at $T_j = 25^\circ C$, $t_p < 250\mu s$

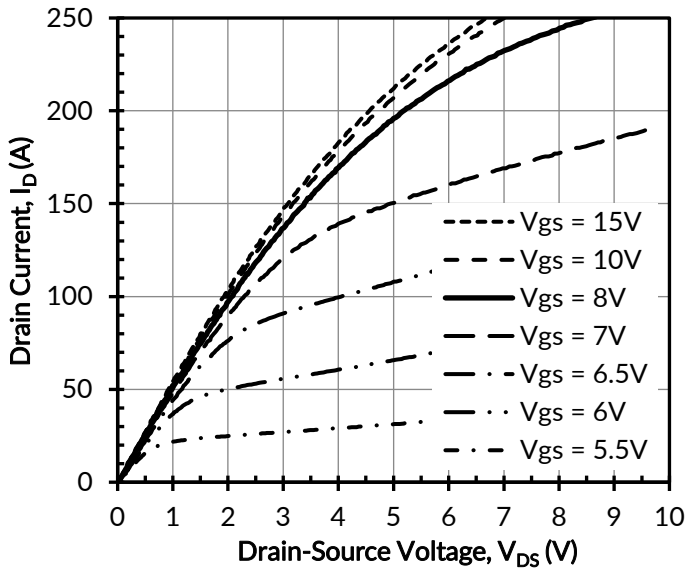


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$ and $t_p < 250\mu\text{s}$

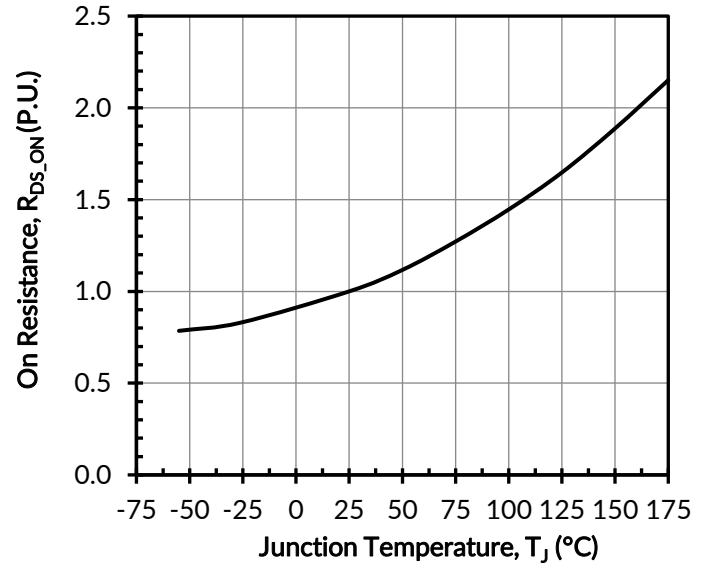


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 70\text{A}$

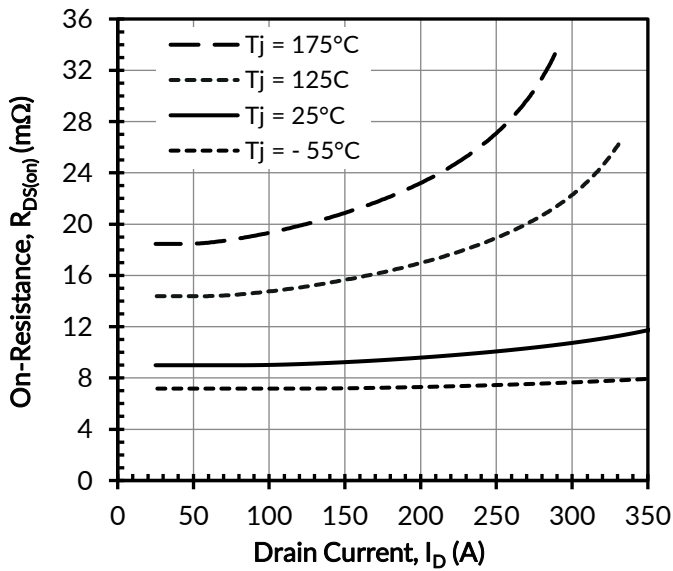


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12\text{V}$

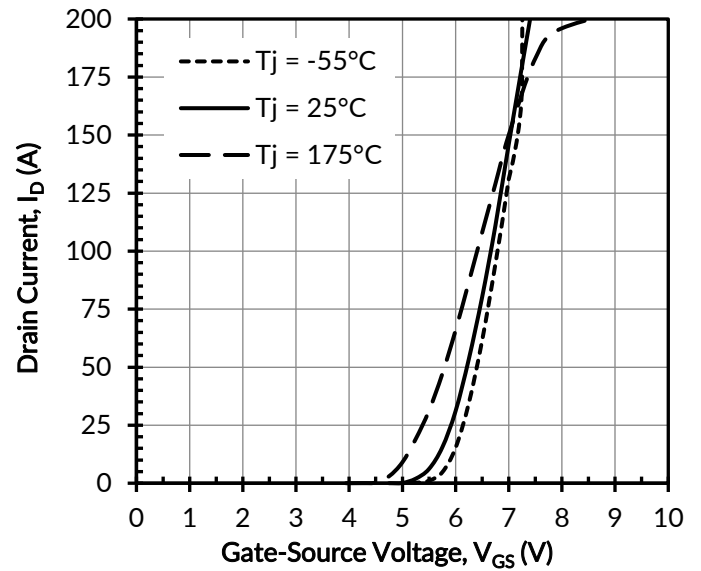


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

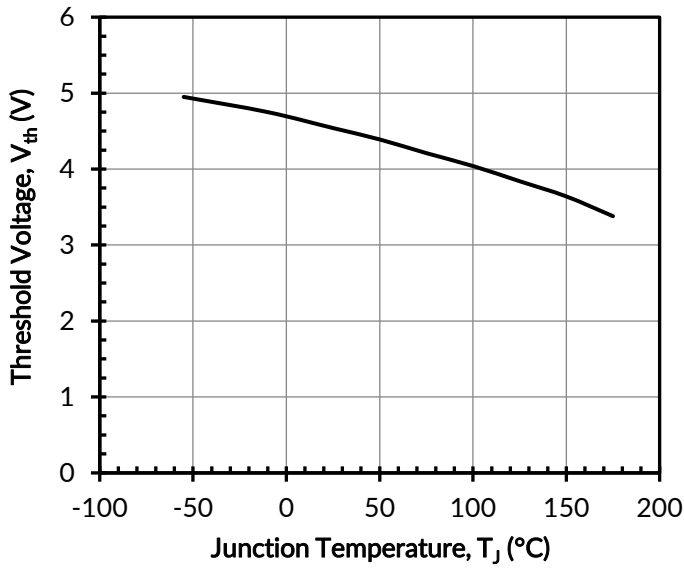


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

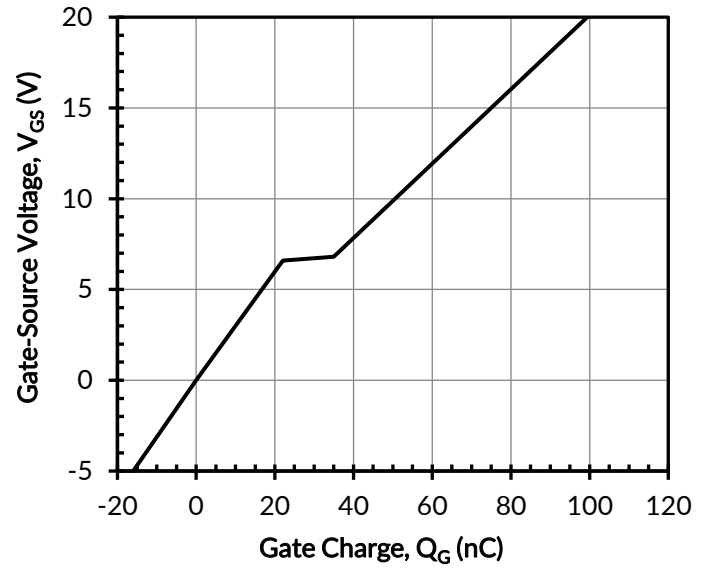


Figure 8. Typical gate charge at $V_{DS}=400V$ and $I_D = 70A$

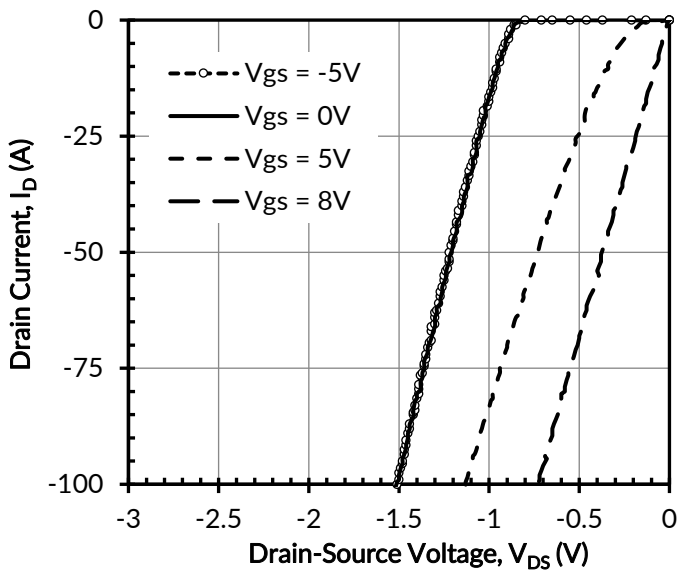


Figure 9. 3rd quadrant characteristics at $T_J = -55^{\circ}C$

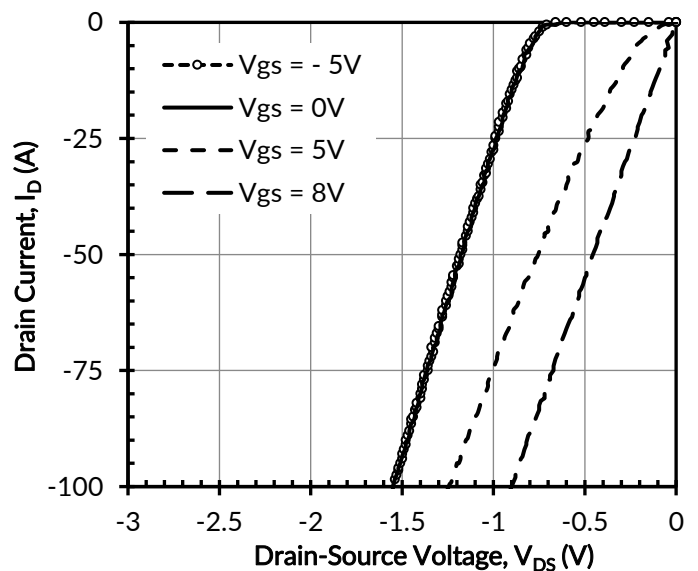


Figure 10. 3rd quadrant characteristics at $T_J = 25^{\circ}C$

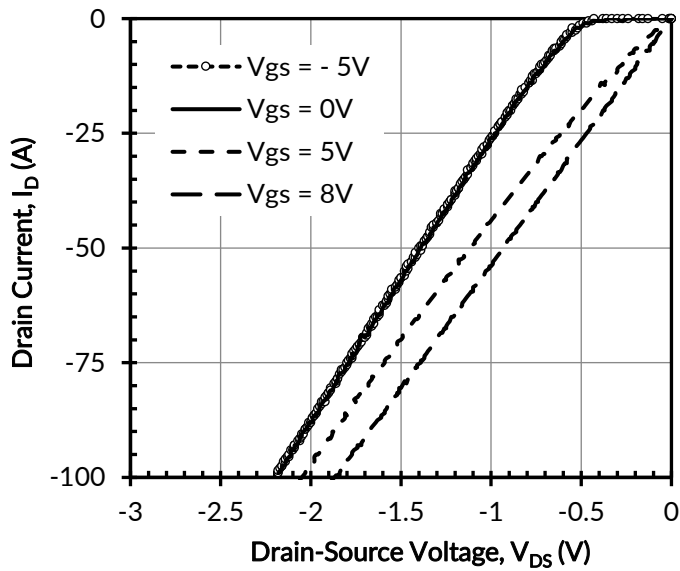


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

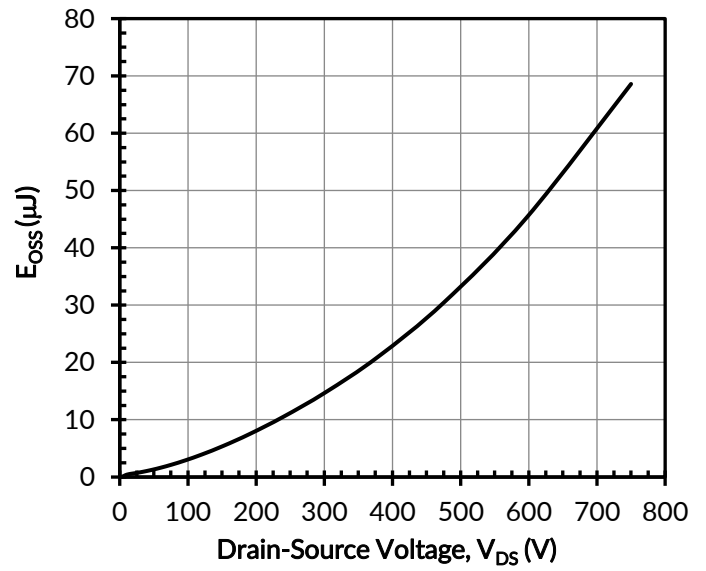


Figure 12. Typical stored energy in C_{oss} at $V_{GS} = 0\text{V}$

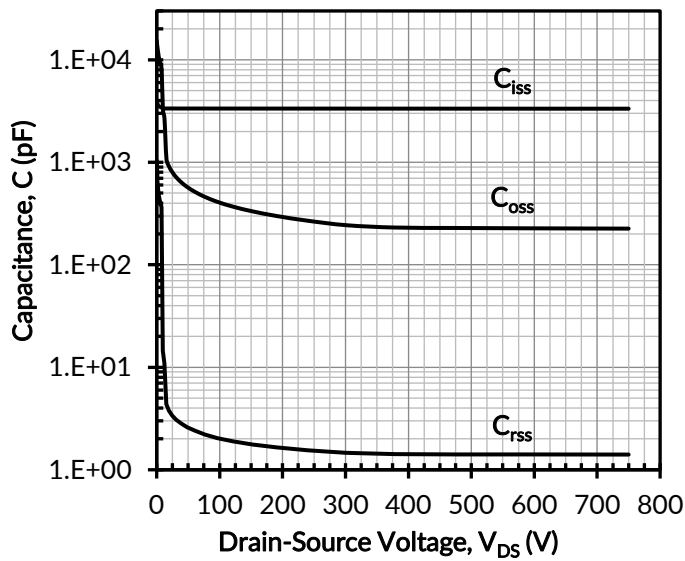


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

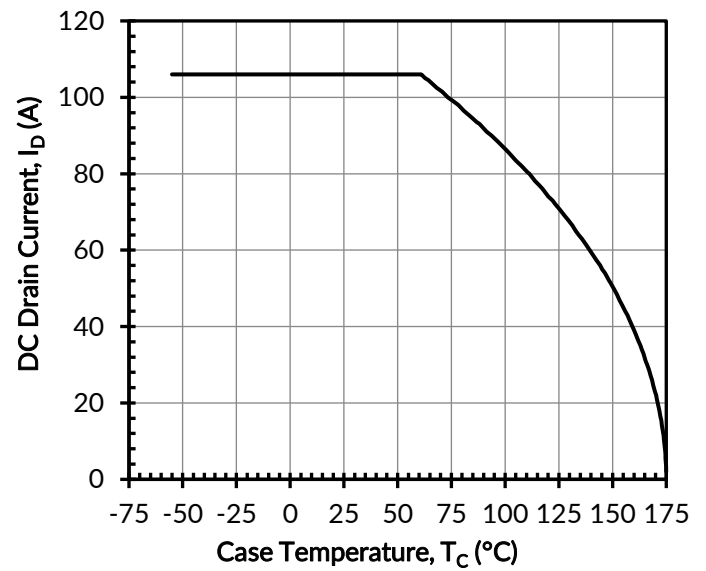


Figure 14. DC drain current derating

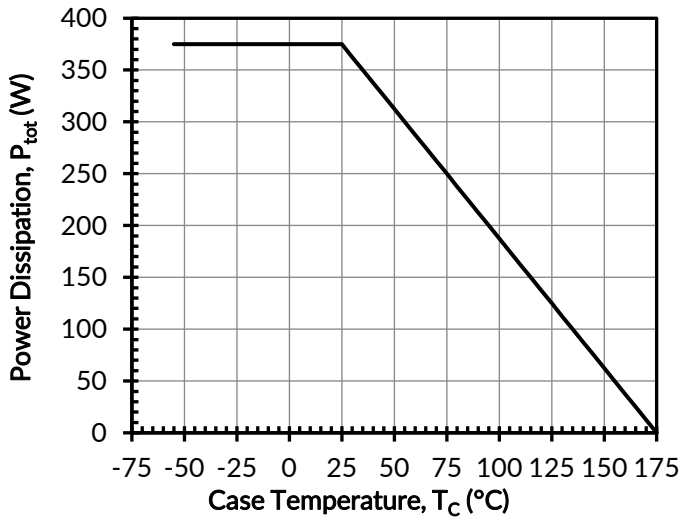


Figure 15. Total power dissipation

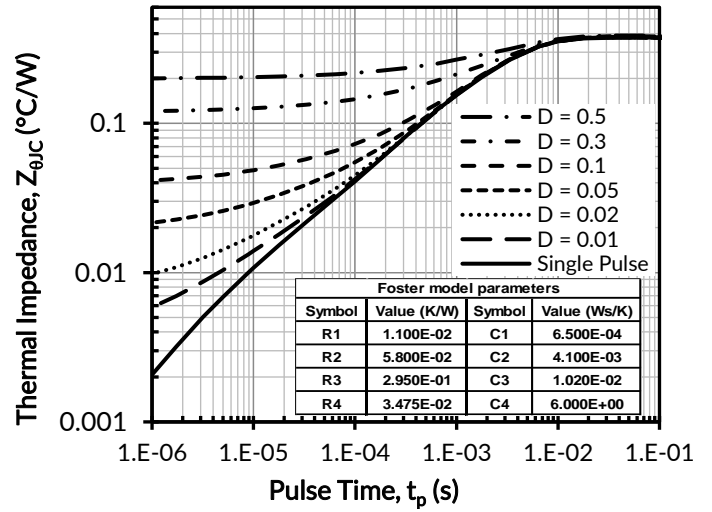


Figure 16. Maximum transient thermal impedance

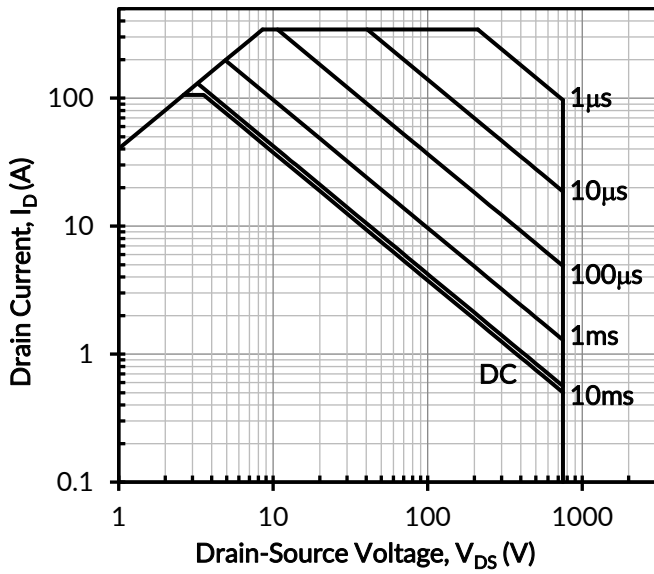


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

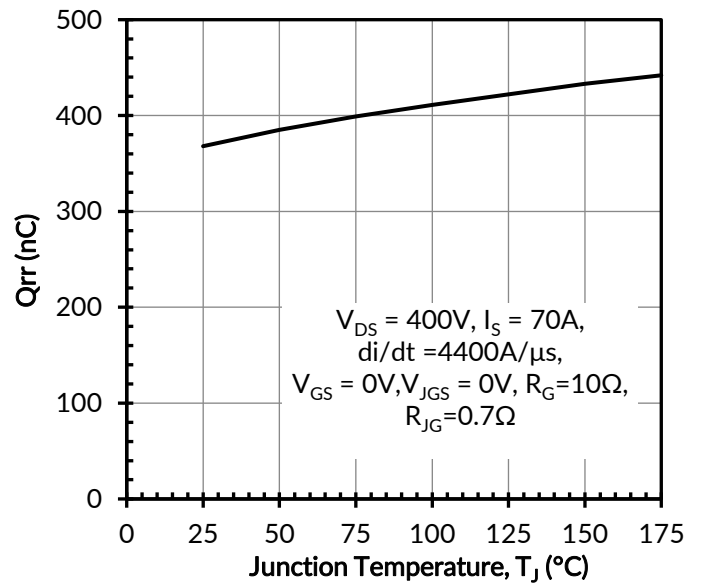


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

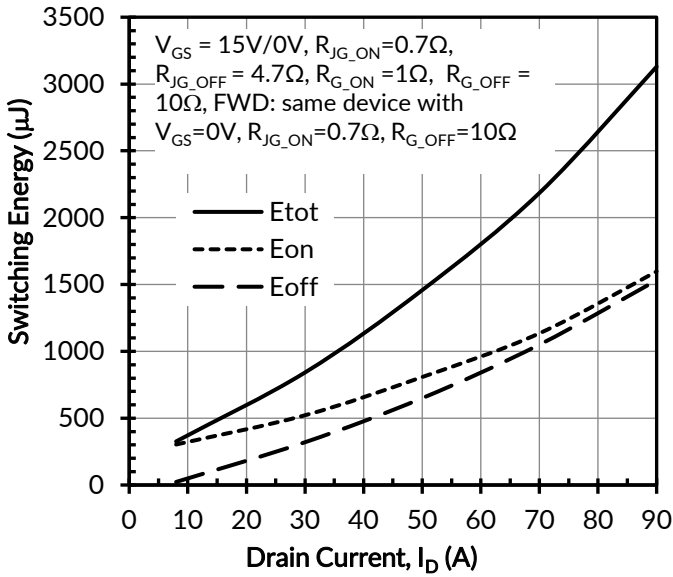


Figure 19. Clamped inductive switching energy vs. drain current at $V_{\text{DS}} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

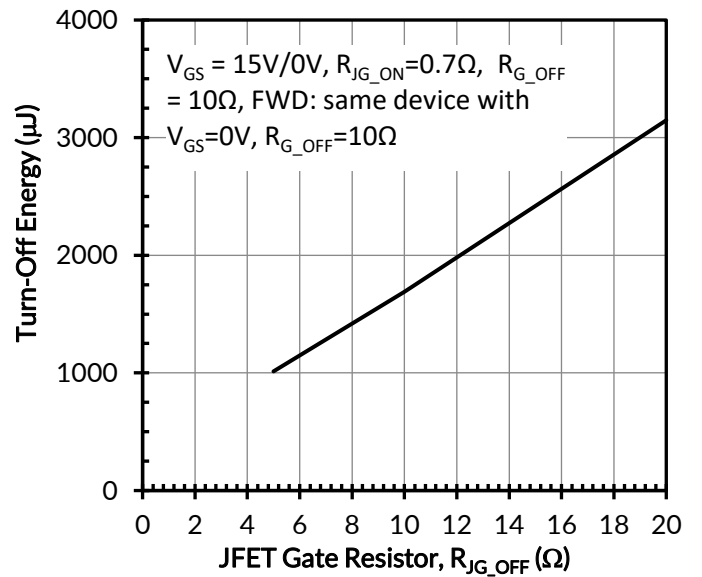


Figure 20. Clamped inductive switching energies vs. JFET gate resistor $R_{\text{JG_OFF}}$ at $V_{\text{DS}} = 400\text{V}$, $I_D = 70\text{A}$, and $T_J = 25^\circ\text{C}$

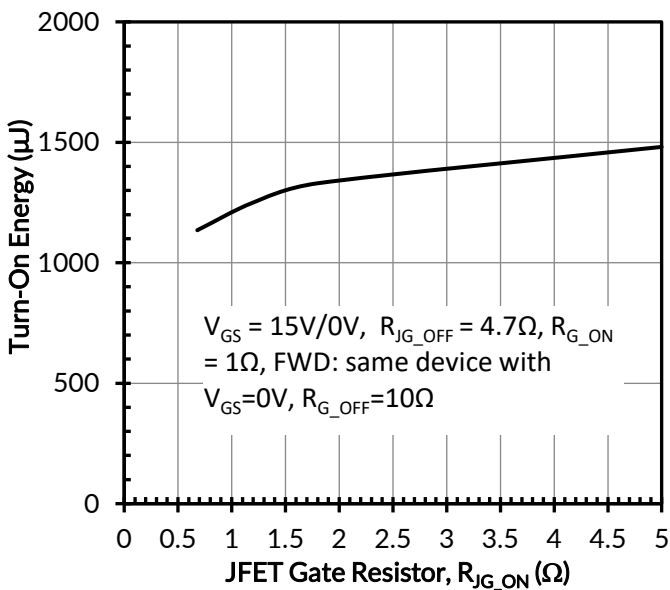


Figure 21. Clamped inductive switching energies vs. JFET gate resistor $R_{\text{JG_ON}}$ at $V_{\text{DS}} = 400\text{V}$, $I_D = 70\text{A}$, and $T_J = 25^\circ\text{C}$

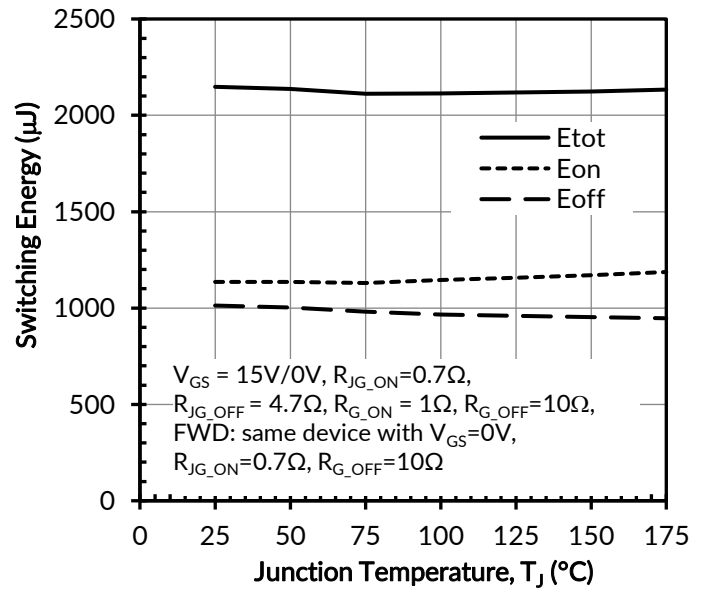


Figure 22. Clamped inductive switching energy vs. junction temperature at $V_{\text{DS}} = 400\text{V}$ and $I_D = 70\text{A}$

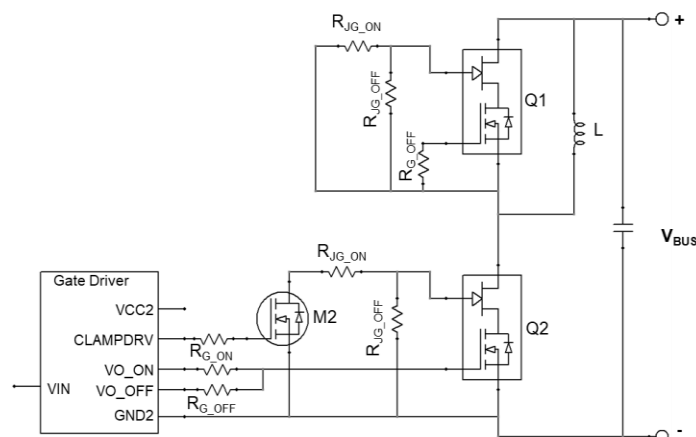


Figure 23. Schematic of the half-bridge mode switching test circuit with ClampDRIVE method.

Typical Performance Diagrams - JFET gate as control terminal and $V_{GS}=+12V$

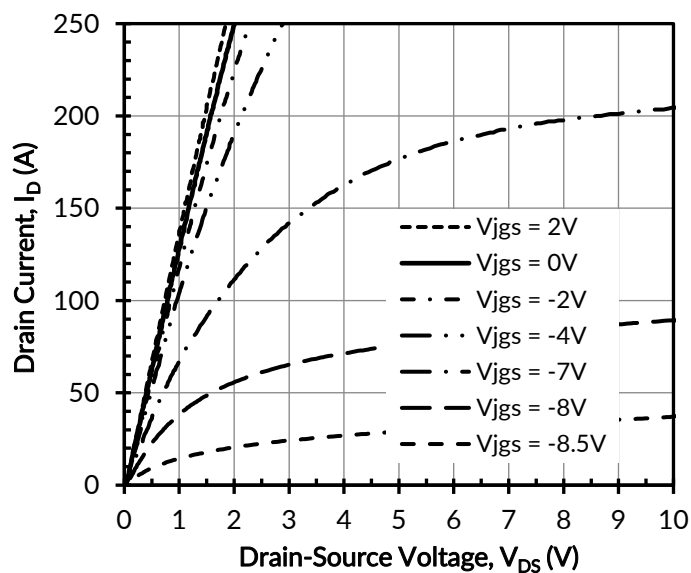


Figure 24. Typical output characteristics with JFET gate as control at $T_J = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

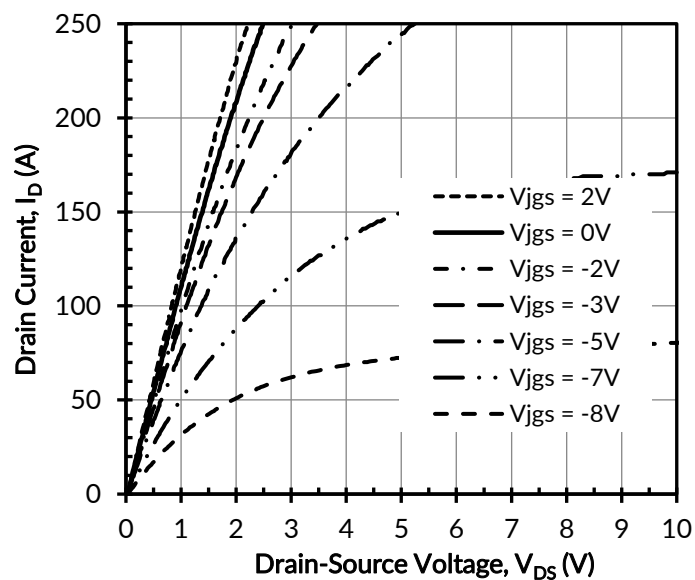


Figure 25. Typical output characteristics with JFET gate as control at $T_J = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

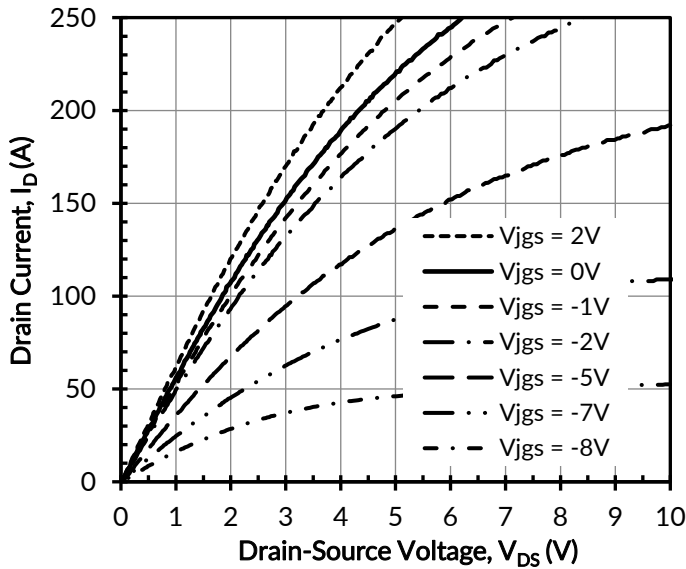


Figure 26. Typical output characteristics with JFET gate as control at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

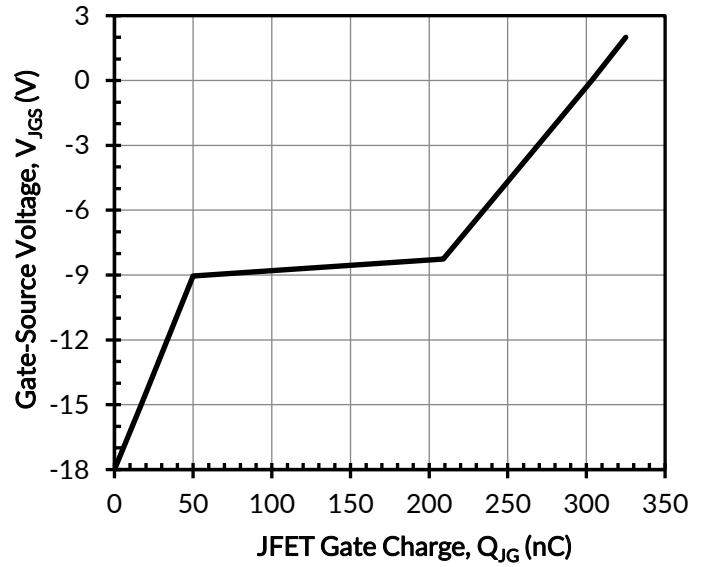


Figure 27. Typical JFET gate charge at $V_{DS} = 400\text{V}$ and $I_D = 70\text{A}$

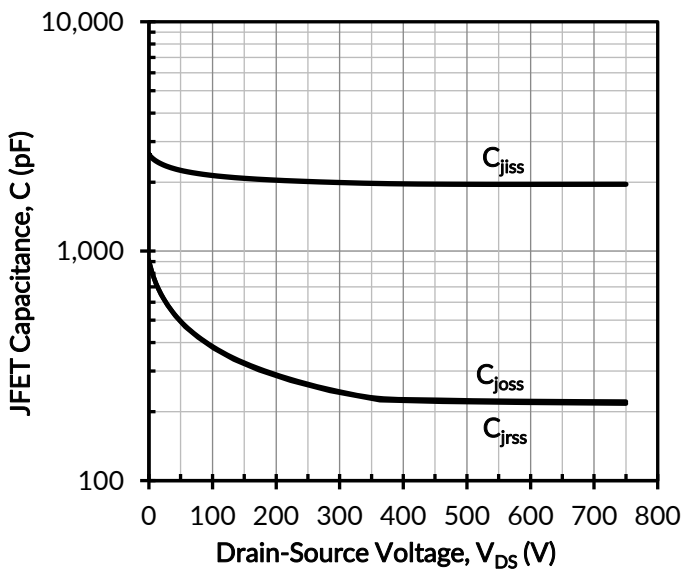


Figure 28. Typical JFET capacitances at $f = 100\text{kHz}$ and $V_{JGS} = -20\text{V}$

Recommended Gate Drive Approach: ClampDRIVE method

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behavior of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring well controlled switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value R_{JG} such that, in the off-state, R_{JG} is small enough not to cause a reverse recovery issue, and during turn-off transient, R_{JG} is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure A. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is R_{JG_OFF} . During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is R_{JG_OFF} during the turn-off process, and R_{JG_OFF} can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of R_{JG_OFF} and R_{JG_ON} . R_{JG_ON} can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and R_{JG_ON} into the JFET gate, so, the turn-on process is also determined by R_{JG_ON} .

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors R_{JG_ON} and R_{JG_OFF} .

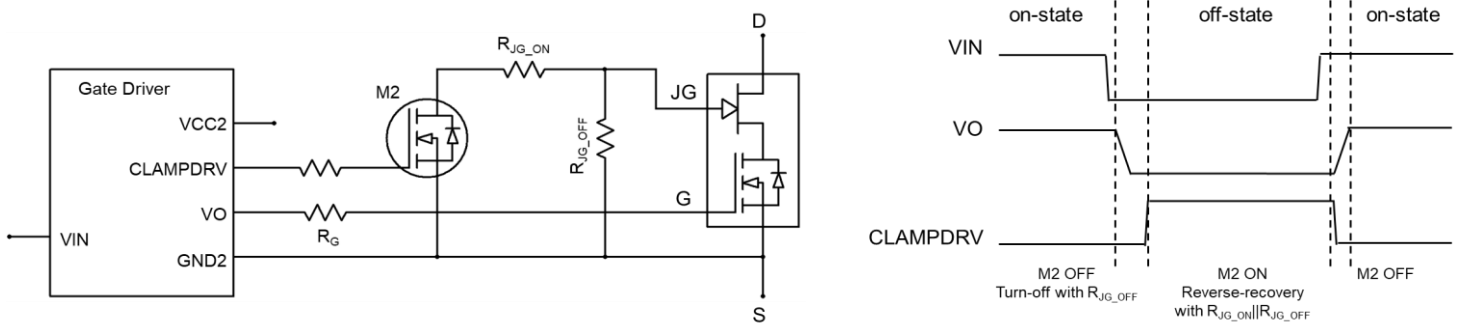


Figure A. Circuit schematic and timing diagram of the ClampDRIVE method

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