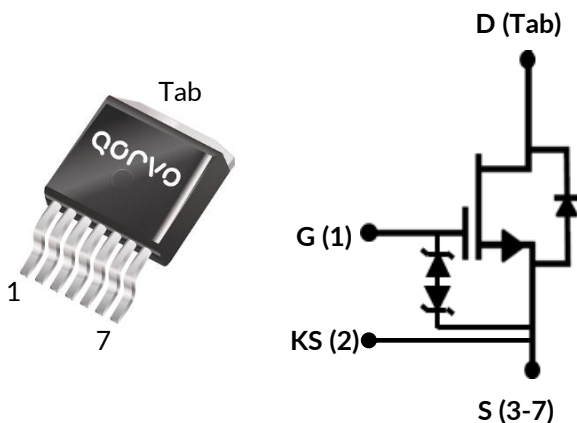


DATASHEET

UF4C120053B7S



1200V-53mΩ SiC FET

Rev A, October 2023

Description

The UF4C120053B7S is a 1200V, 53mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs.

Available in the space-saving D²PAK-7L package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: 53mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 98nC
- Low body diode V_{FSD} : 1.28V
- Low gate charge: Q_G = 37.8nC
- Threshold voltage $V_{G(th)}$: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- D²PAK-7L package for faster switching, clean gate waveforms

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Induction heating

Part Number	Package	Marking
UF4C120053B7S	D²PAK-7L	UF4C120053B7S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC ($f > 1\text{Hz}$)	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	34	V
		$T_C = 100^\circ\text{C}$	24.6	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	100	A
Single pulsed avalanche energy ³	E_{AS}	$L=15\text{mH}$, $I_{AS}=2.7\text{A}$	54.6	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 800\text{V}$	150	V/ns
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	250	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering Temperature	T_{solder}	reflow MSL 1	245	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.46	0.60	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	1200			V
Total drain leakage current	I_{DSS}	$V_{DS}=1200V, V_{GS}=0V, T_J=25^\circ\text{C}$		0.2	50	μA
		$V_{DS}=1200V, V_{GS}=0V, T_J=175^\circ\text{C}$		15		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		6	20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=20A, T_J=25^\circ\text{C}$		53	67	$m\Omega$
		$V_{GS}=12V, I_D=20A, T_J=125^\circ\text{C}$		112		
		$V_{GS}=12V, I_D=20A, T_J=175^\circ\text{C}$		159		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	4.8	6	V
Gate resistance	R_G	$f=1MHz, \text{open drain}$		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			34	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			100	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_S=10A, T_J=25^\circ\text{C}$		1.28	1.65	V
		$V_{GS}=0V, I_S=10A, T_J=175^\circ\text{C}$		1.96		
Reverse recovery charge	Q_{rr}	$V_{DS}=800V, I_S=25A, V_{GS}=-5V, R_G=20\Omega, di/dt=1600A/\mu s, T_J=25^\circ\text{C}$		98		nC
Reverse recovery time	t_{rr}	$T_J=25^\circ\text{C}$		15.2		ns
Reverse recovery charge	Q_{rr}	$V_{DS}=800V, I_S=25A, V_{GS}=-5V, R_G=20\Omega, di/dt=1600A/\mu s, T_J=150^\circ\text{C}$		105		nC
Reverse recovery time	t_{rr}	$T_J=150^\circ\text{C}$		19.6		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=800V, V_{GS}=0V$ $f=100kHz$		1370		pF
Output capacitance	C_{oss}			43.5		
Reverse transfer capacitance	C_{rss}			2.2		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to $800V$, $V_{GS}=0V$		54		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to $800V$, $V_{GS}=0V$		100		pF
C_{OSS} stored energy	E_{oss}	$V_{DS}=800V, V_{GS}=0V$		17.3		μJ
Total gate charge	Q_G	$V_{DS}=800V, I_D=25A$, $V_{GS}=0V$ to $15V$		37.8		nC
Gate-drain charge	Q_{GD}			9.5		
Gate-source charge	Q_{GS}			10		
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, $V_{DS}=800V, I_D=25A$, Gate Driver = $-5V$ to $+15V$, $R_{G_ON}=1\Omega, R_{G_OFF}=20\Omega$, inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 20\Omega$, Snubber: $R_s=20\Omega$, $C_s=100pF$ $T_J=25^\circ C$		20		ns
Rise time	t_r			32		
Turn-off delay time	$t_{d(off)}$			57		
Fall time	t_f			12		
Turn-on energy	E_{ON}			570		μJ
Turn-off energy	E_{OFF}			57		
Total switching energy	E_{TOTAL}			627		
Snubber R_s energy during turn-on	E_{RS_ON}			5		
Snubber R_s energy during turn-off	E_{RS_OFF}			11		
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, $V_{DS}=800V, I_D=25A$, Gate Driver = $-5V$ to $+15V$, $R_{G_ON}=1\Omega, R_{G_OFF}=20\Omega$, inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 20\Omega$, Snubber: $R_s=20\Omega$, $C_s=100pF$ $T_J=150^\circ C$		24		ns
Rise time	t_r			33		
Turn-off delay time	$t_{d(off)}$			63		
Fall time	t_f			13		
Turn-on energy including R_s energy	E_{ON}			660		μJ
Turn-off energy including R_s energy	E_{OFF}			75		
Total switching energy	E_{TOTAL}			735		
Snubber R_s energy during turn-on	E_{RS_ON}			5		
Snubber R_s energy during turn-off	E_{RS_OFF}			12		

4. Measured with the switching test circuit in Figure 26.

5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance Diagrams

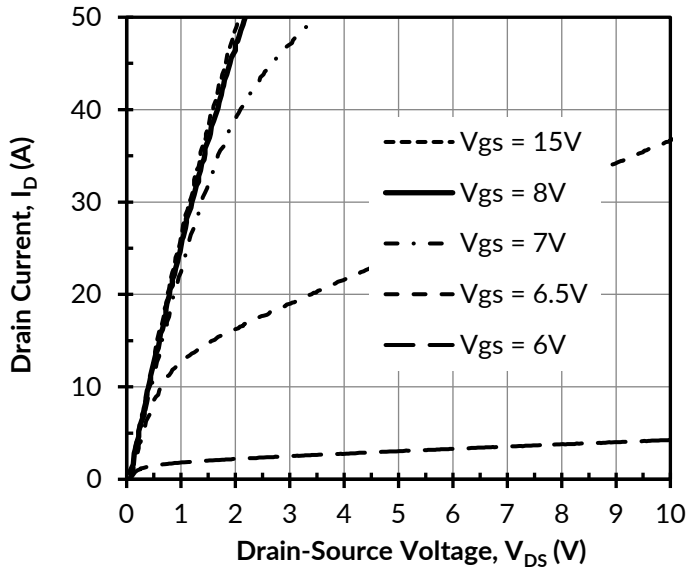


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

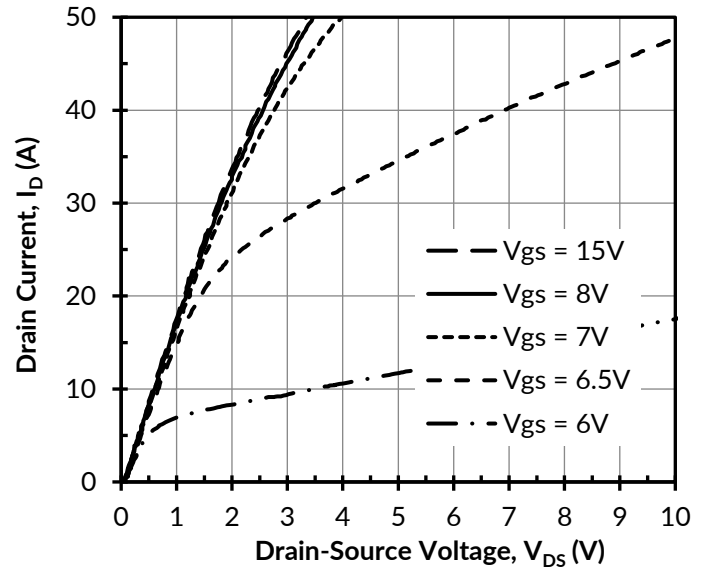


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

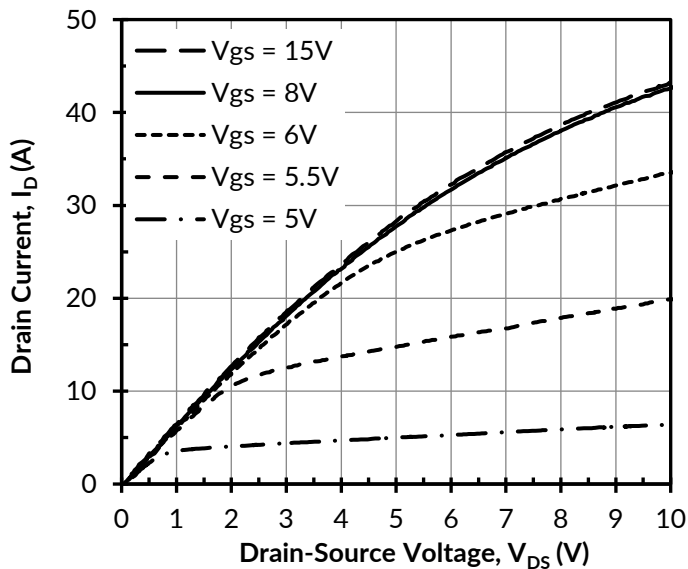


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

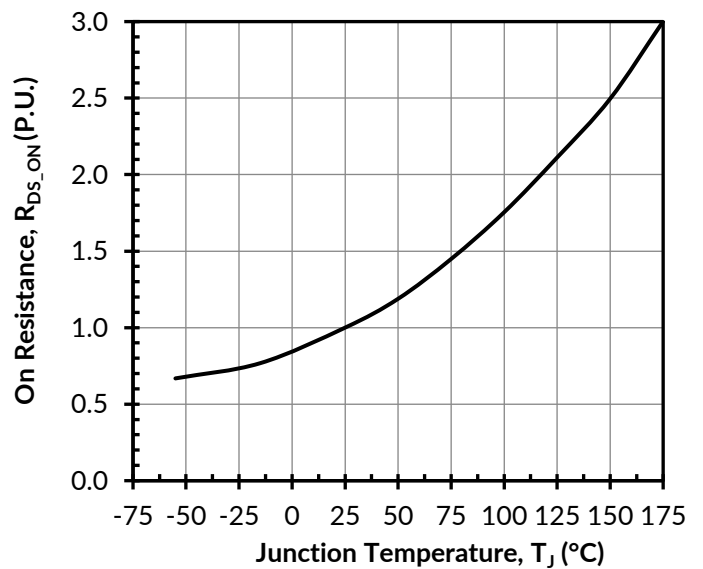


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 25\text{A}$

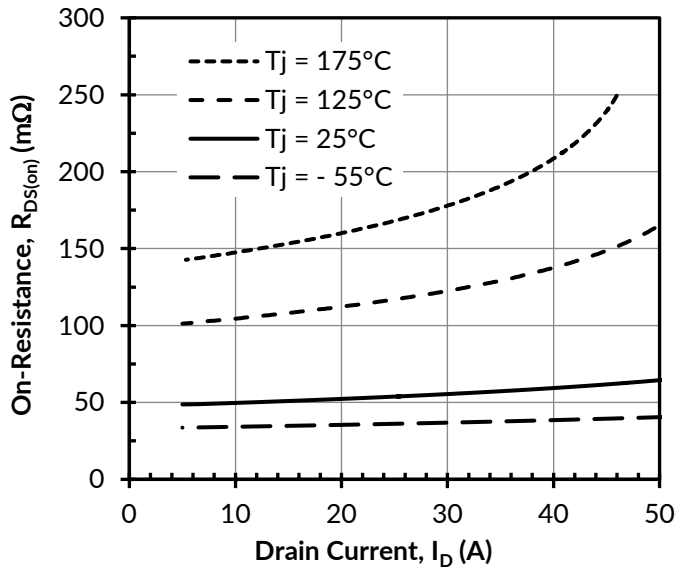


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

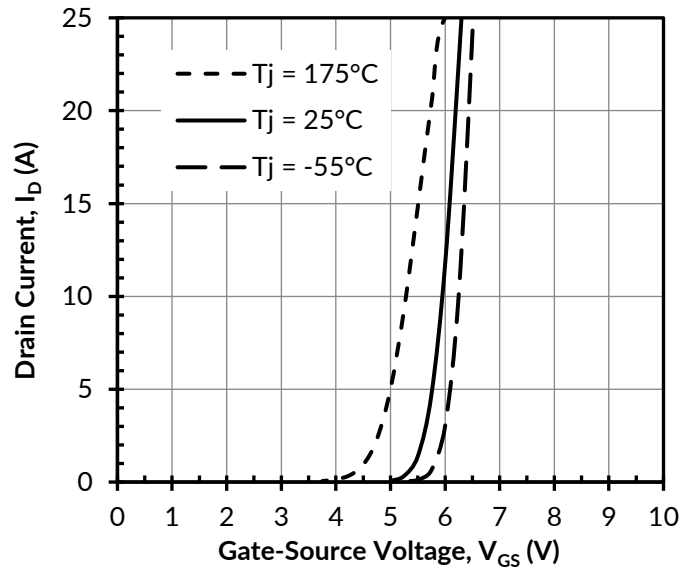


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

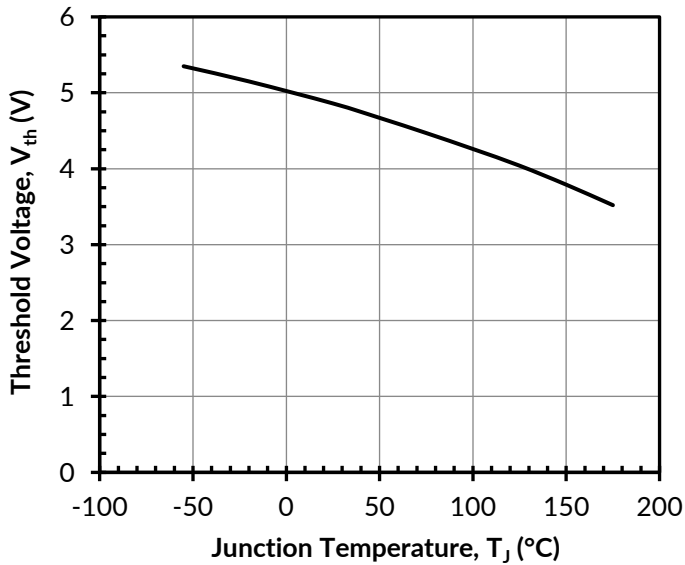


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

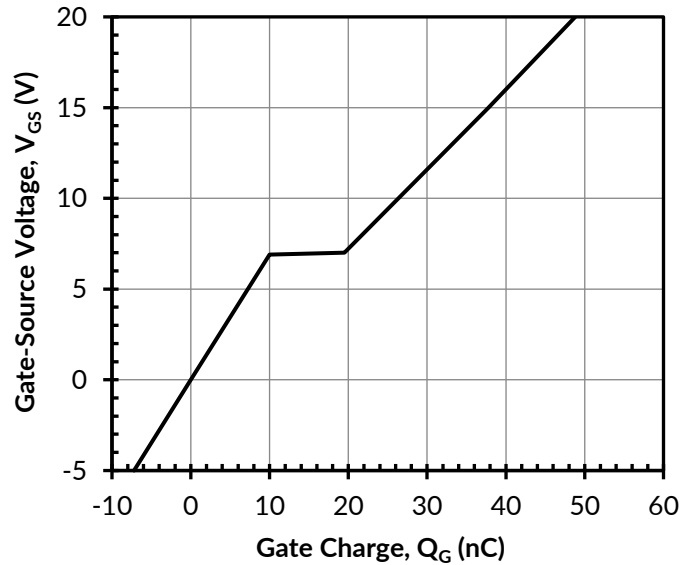


Figure 8. Typical gate charge at $V_{DS} = 800V$ and $I_D = 25A$

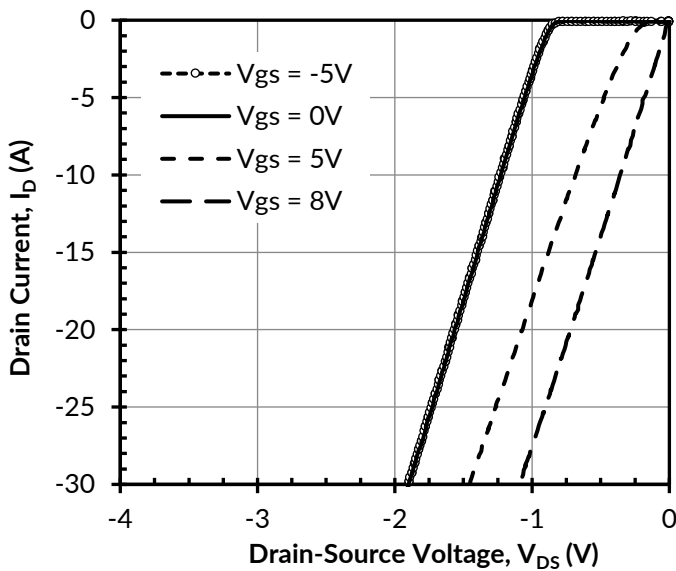


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

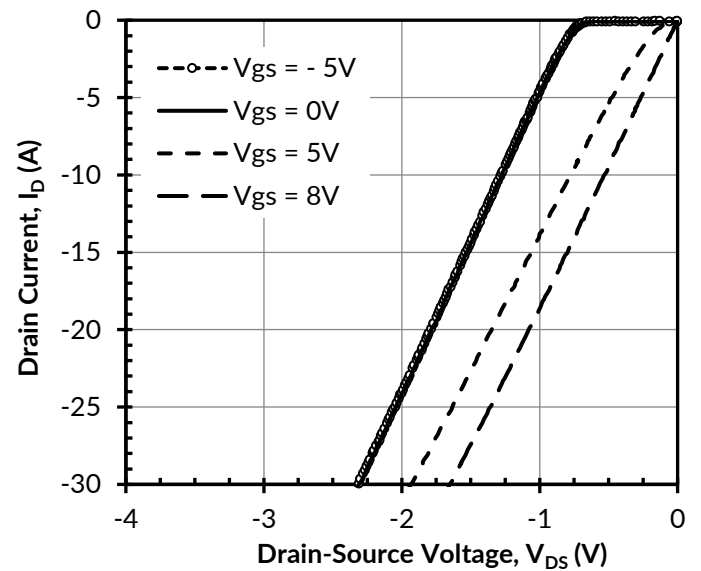


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

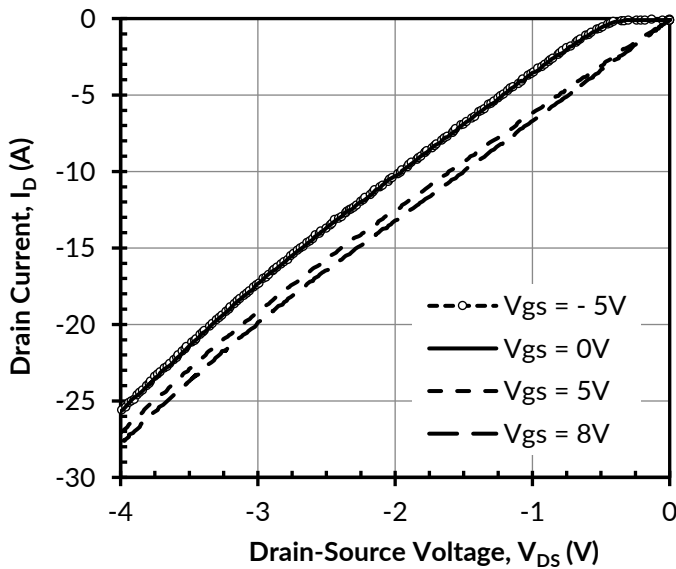


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

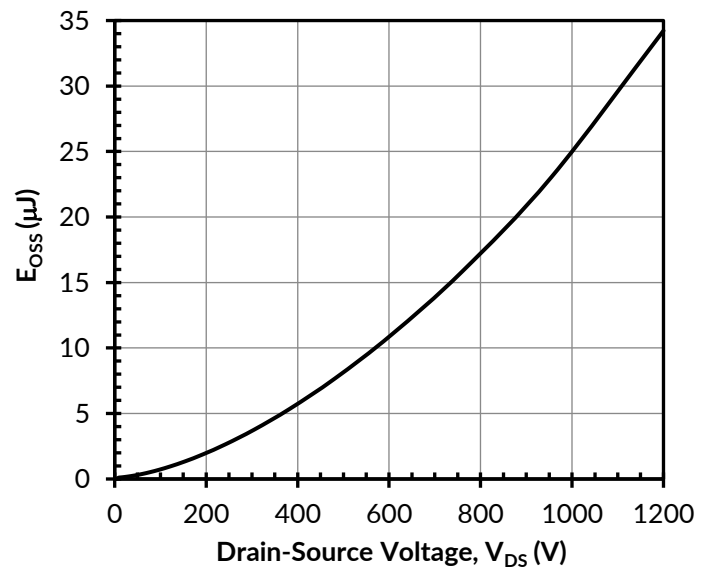


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

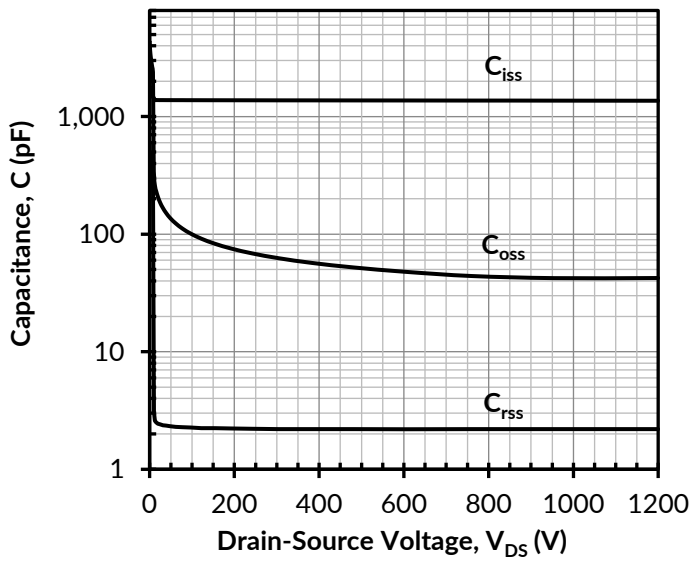


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

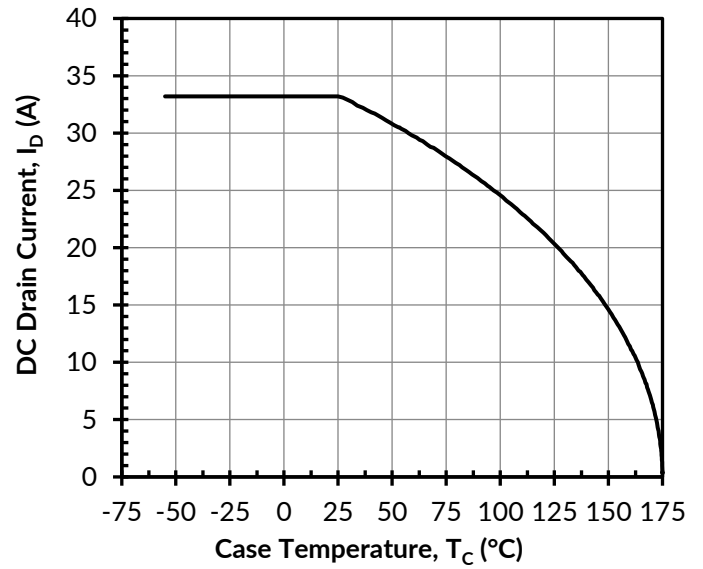


Figure 14. DC drain current derating

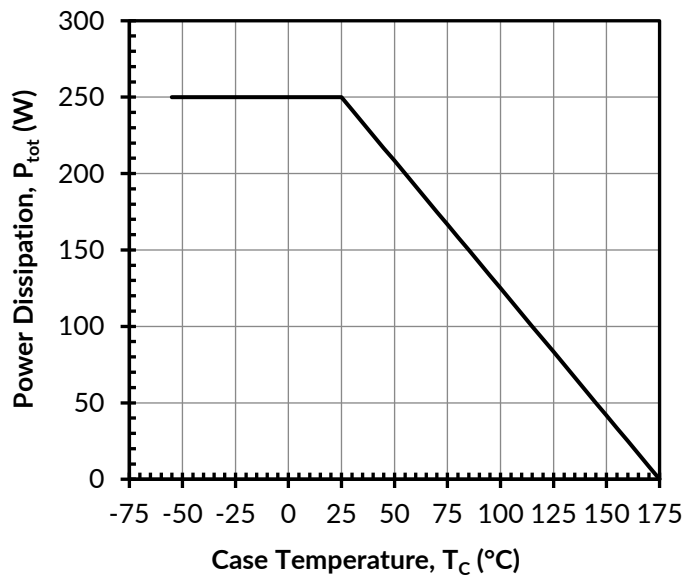


Figure 15. Total power dissipation

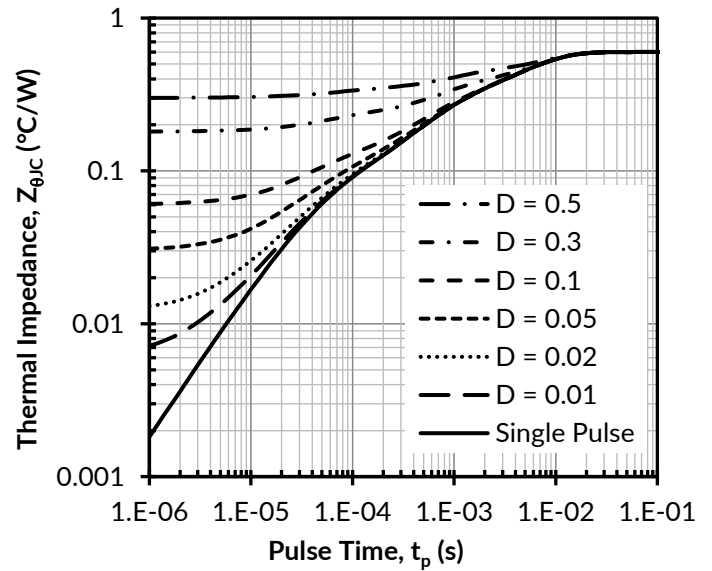


Figure 16. Maximum transient thermal impedance

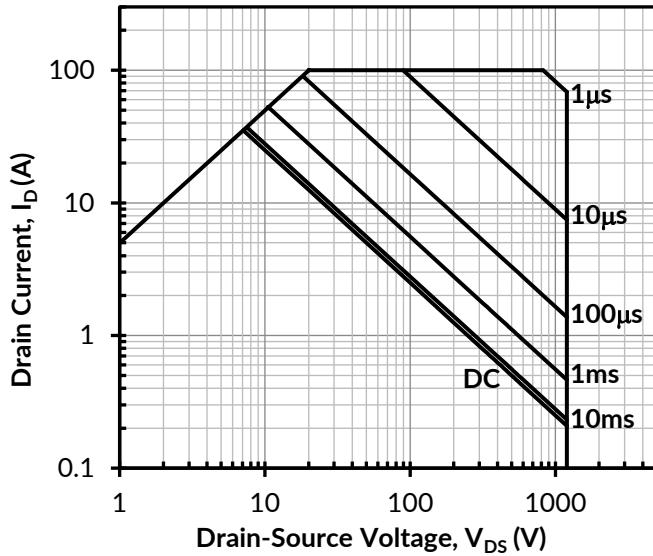


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

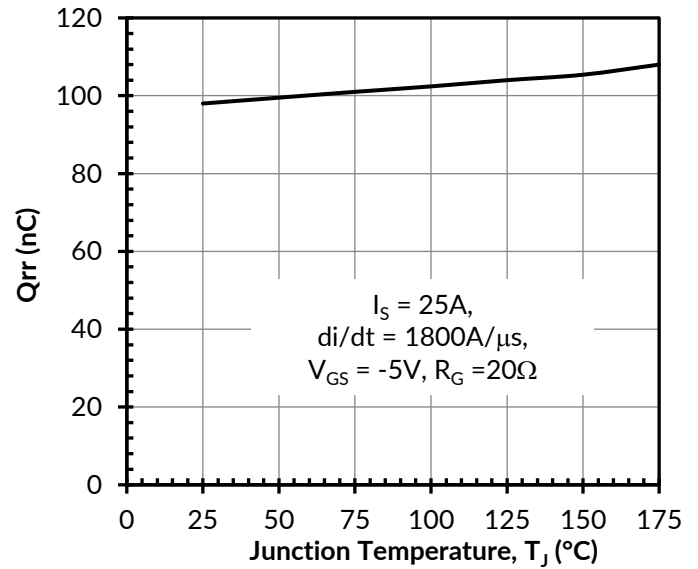


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature at $V_{DS} = 800\text{V}$

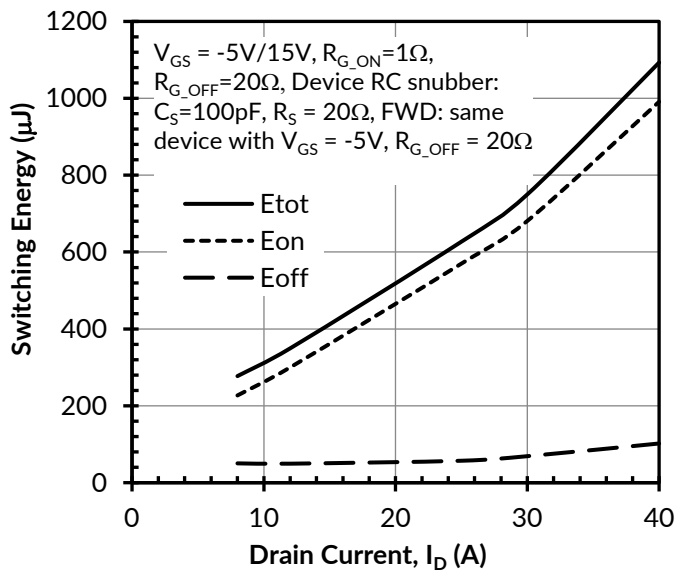


Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 800\text{V}$ and $T_J = 25^\circ\text{C}$

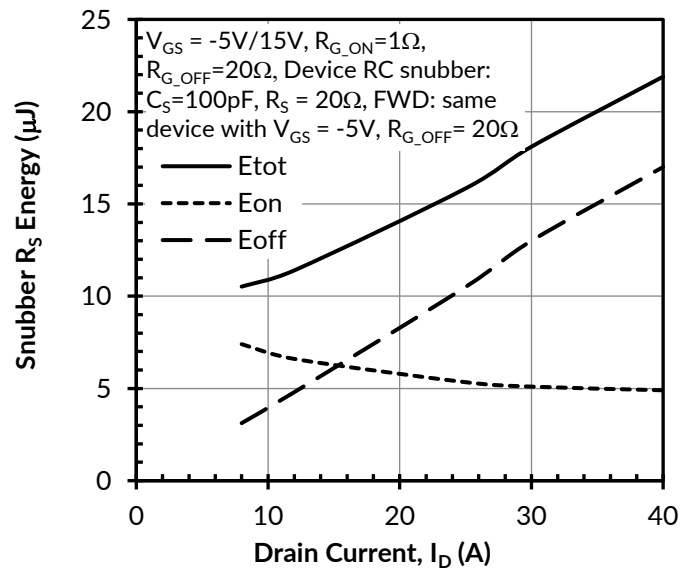


Figure 20. RC snubber energy loss vs. $R_{G,EXT}$ at $V_{DS} = 800\text{V}$, $I_D = 25\text{A}$, and $T_J = 25^\circ\text{C}$

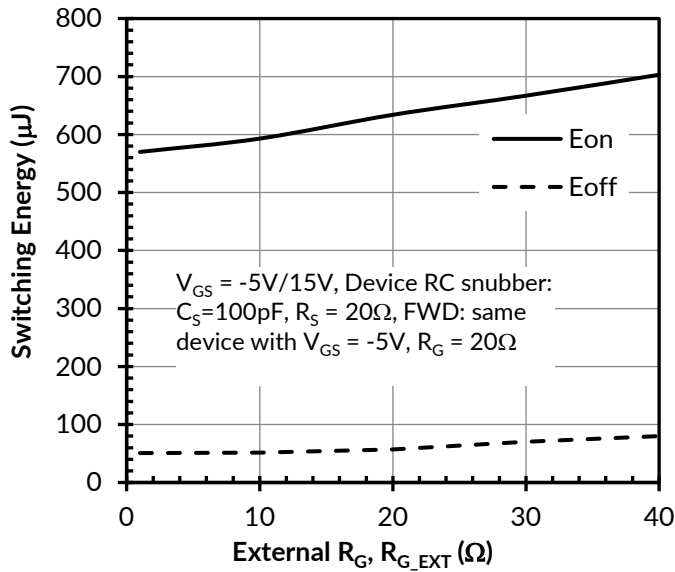


Figure 21. Clamped inductive switching energies vs. R_{G_EXT} at $V_{DS} = 800V$, $I_D = 25A$, and $T_J = 25^\circ\text{C}$

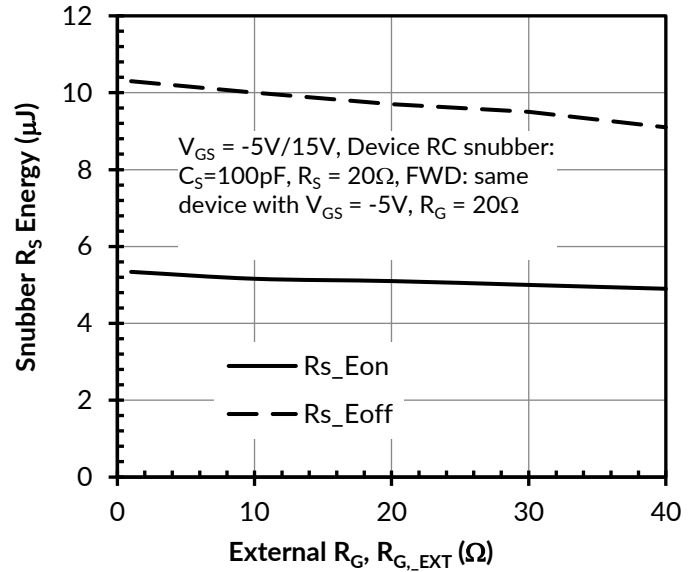


Figure 22. RC snubber energy loss vs. R_{G_EXT} at $V_{DS} = 800V$, $I_D = 25A$, and $T_J = 25^\circ\text{C}$

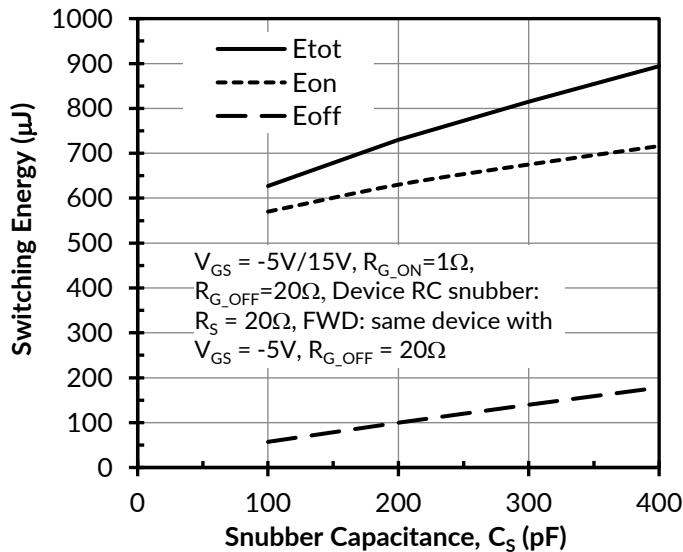


Figure 23. Clamped inductive switching energies vs. snubber capacitance C_S at $V_{DS} = 800V$, $I_D = 25A$, and $T_J = 25^\circ\text{C}$

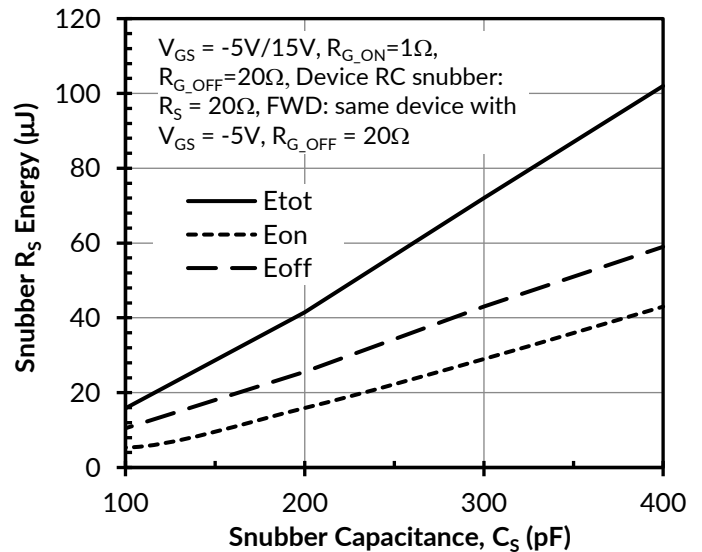


Figure 24. RC snubber energy losses vs. snubber capacitance C_S at $V_{DS} = 800V$, $I_D = 25A$, and $T_J = 25^\circ\text{C}$

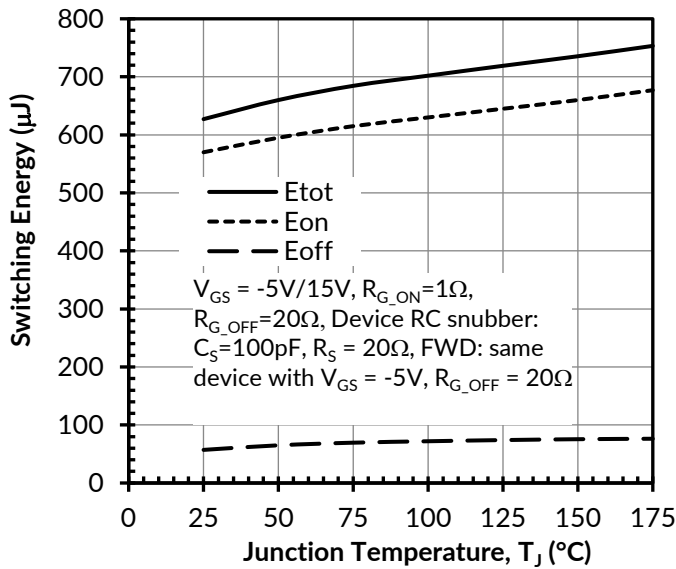


Figure 25. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 800V$ and $I_D = 25A$

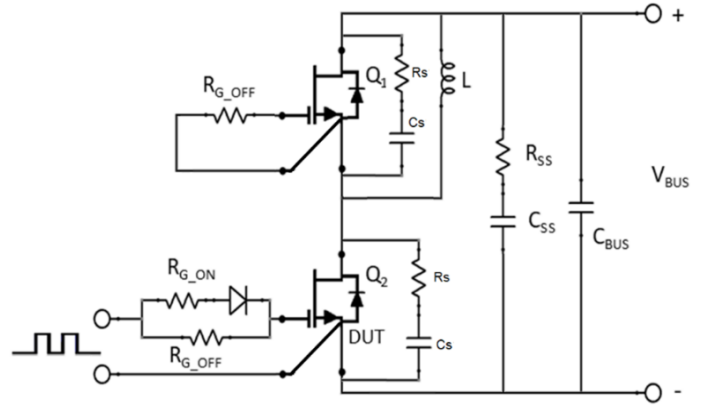


Figure 26. Schematic of the half-bridge mode switching test circuit with device RC snubbers ($R_S = 20\Omega$, $C_S = 100pF$) and a bus RC snubber ($R_{SS} = 2.5\Omega$, $C_{SS} = 100nF$).

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see <https://www.qorvo.com/design-hub>.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the Qorvo website at <https://www.qorvo.com/design-hub>.

Important notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.