

SiC FET & Module User Guide

Scope

This SiC FET & Module user guide presents practical solutions and guidelines for fast switching SiC devices. The solution is verified by experimental double pulse tests (DPT) results. The snubber loss is precisely measured to assist users in computing the power rating of the snubber resistor and is much lower than traditional estimation using CV^2 . The beneficial impact of the snubber is analyzed for both hard-switching and soft-switching applications in application note “[Switching Fast SiC FETs with a Snubber](#)”. Please review our webinar for more details on snubber benefits and snubber loss analysis: [Minimizing EMI and switching loss for fast SiC FETs](#).

Referenced Documents

- [1] Qorvo SiC power solution central hub: <https://www.qorvo.com/innovation/power-solutions/sic-power>
- [2] More design tips: <https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips>
- [3] SMT assembly guide: [Qorvo Surface Mount Technology Devices](#)
- [4] [Origins of SiC FETs and Their Evolution Towards the Perfect Switch](#)
- [5] [Circuit Protection with SiC FETs in Dual-Gate Configuration](#)
- [6] X. Li, A. Bhalla and P. Losee, "ClampDRIVE: An Improved Technique for SiC Cascode FET Switching Behavior Control," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 181-186, doi: 10.1109/APEC43580.2023.10131568.
- [7] Web based loss calculator: <https://www.qorvo.com/design-hub/design-tools/interactive/fet-jet-calculator>
- [8] Citation: J. Betten, "Power Tips: Calculate an R-C snubber in seven steps", https://e2e.ti.com/blogs_/b/powerhouse/posts/calculate-an-r-c-snubber-in-seven-steps
- [9] Snubber benefits and loss estimation: <https://www.qorvo.com/design-hub/videos/minimizing-emi-and-switching-loss-for-sic-fets>
- [10] Paralleling SiC FETs – Best Practices: <https://www.qorvo.com/products/d/da009247>

Contents

Product family introduction

- Qorvo Gen3 vs Gen4
- UJ, UF, UG, C/SC, E1B module

Snubbers achieve high efficiency and smooth waveforms

- Example waveforms
- Snubber configuration
- Avoid long lead

Recommendation table for all part number

Snubber design guides

Product family introduction

SiC power semiconductor can greatly improve power density, efficiency, and cost-effectiveness for overall system design compared to Si devices. The core advantages of SiC are high voltage blocking capability, low conduction loss, low switching loss, and high thermal conductivity. All these advantages combined enable power density enhancement from two factors. First, to increase power density the loss of a system must be reduced to handle the increased concentration of heat. The low conduction loss and low switching loss of SiC FET help to achieve this goal. Second, lower switching loss allows higher switching frequency which enables smaller size of passive components such as capacitors and inductors for a system with a given power level. Thanks to all these advantages, SiC power devices have been accelerating efficiency and performance improvements in many industrial and automotive applications such as server power supplies, energy storage systems, EV motor drives and charging equipment, etc.

Qorvo Gen3 vs Gen4

Qorvo SiC FET is a cascode structure device consists of a high-voltage SiC JFET and a low-voltage Si MOSFET (LVMOS). Qorvo SiC JFET has many advantages such as super low $R_{DS(on)}$, super low output capacitance, etc. A cascode structure is needed to make SiC FET a normally-off device. Gen3 products use planar technology. Gen4 products use trench technology which pushes performance to the next level.

Please see this link for more information on Gen4 products: [GEN 4 SiC FETs](#).

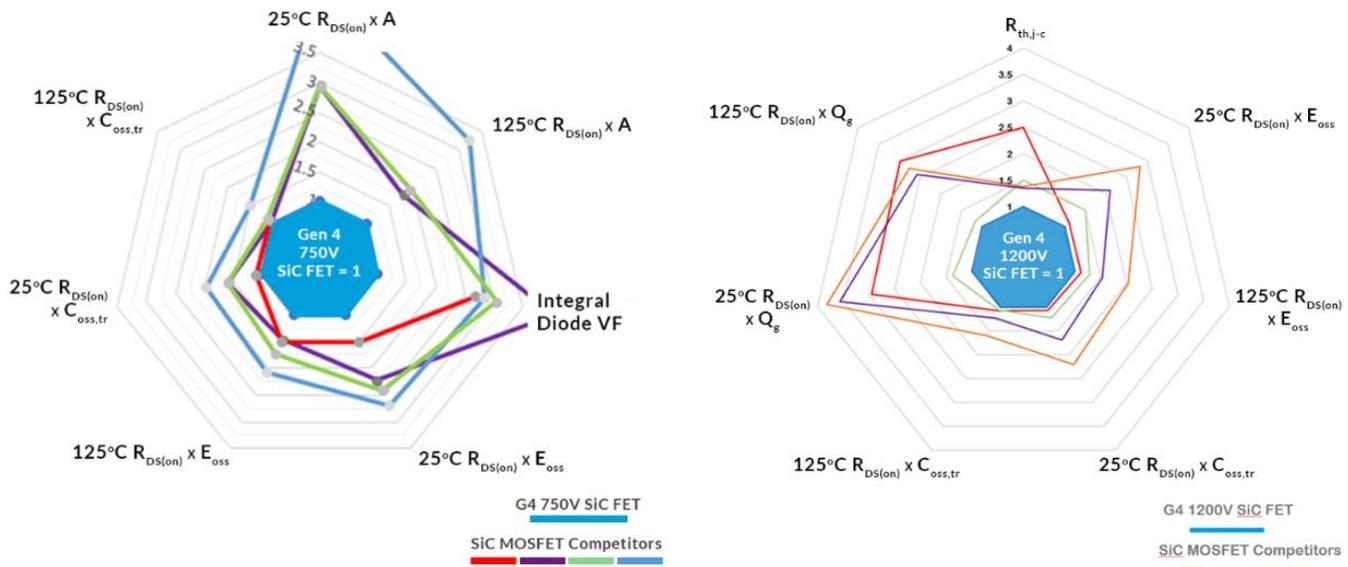


Figure 1. Figures of merit parameters normalized to Gen 4 SiC FETs. 750V is on the left. 1200V is on the right.

Gen 4 750V key features	Gen 4 1200V key features
750V VDS rating vs 650V VDS rating from other vendors	1200V VDS rating
Low $R_{DS(on)}$ from 5.4 m Ω to 60 m Ω	Low $R_{DS(on)}$ from 23 m Ω to 70 m Ω
Best-in-class figure of merit	Best-in-class figure of merit
Flexible gate drive voltage from 12 V to 18V with 5 V threshold	Flexible gate drive voltage from 12 V to 18V with 5 V threshold
Wide package options: TO-247-3L/4L, TOLL, D2PAK-7L	Wide package options: TO-247-3L/4L, TOLL, D2PAK-7L
Especially advantageous for ZVS soft-switching applications	Especially advantageous for ZVS soft-switching applications
5 μs short-circuit withstand time for 6m Ω device	

UJ, UF, UG, C/SC, E1B module

UJ series UJ series has slower switching speed which is good for replacing existing non-kelvin package designs like TO247-3L, D2PAK3L, etc.

UF series UF series has faster switching speed which is good for high switching frequency, high efficiency, and high-power density applications. It is recommended to use kelvin package designs like TO247-4L, D2PAK7L, MO-229 (TOLL), etc. to fully exploit the fast-switching speed of UF series. Device snubber is strongly recommended for UF series non-kelvin packages, TO247-3L, D2PAK3L, etc.

UG series has two gate pins (one for SiC JFET, one for Si MOSFET). The SiC JFET gate pin allows very wide controllability of switching speed. UG series target applications with very high currents and relatively slow dv/dt ($<20V/ns$) like circuit protection, etc. UG series are easy to parallel even in discrete packages. For more details, please see [6].

C/SC means side-by-side cascode or stacked cascode. Letter “C” means that the cascode structure has a Si low voltage MOSFET and SiC high voltage JFET packaged side-by-side. Letter “SC” means that the cascode structure has a Si low voltage MOSFET die attached on top of the SiC high voltage JFET die, thus called stacked die. Stacked die has 2X power cycling lifetime comparing to SiC MOSFET.

E1B modules provide Qorvo SiC benefits (low $R_{DS(on)}$, low switching loss, low thermal resistance junction to case, etc.) in an industry standard module package. E1B package is pin compatible to many vendors. Qorvo’s first 1200 V E1B modules are extremely efficient for ZVS (zero-voltage switching) soft-switching applications like phase-shifted full-bridge, LLC, etc. Please refer to E1B module [mounting guidelines](#) and [technical overview](#) documents for detailed information.

Snubbers achieve high efficiency and smooth waveforms

Qorvo strongly recommends using snubbers (device snubber and bus snubber) with low R_g to control switching speed of SiC FETs.

- First, using bus snubber (decoupling cap) can greatly reduce power commutation loop stray inductance. This means less voltage overshoot peak (drain-to-source) and ringing duration at a faster switching speed, thus balancing high efficiency and EMI.
- Second, using device drain-to-source snubber capacitor enables significant reduction in turn-off switching loss for inductive load hard turn-off switching, especially for ZVS soft-switching where drain-to-source snubber capacitor energy is recycled for turn-on.
- Third, Qorvo SiC FETs have very small gate-to-drain stray capacitance (C_{gd}) which is preferable for fast switching and improved immunity to false-trigger by fast dv/dt . However, it also makes external gate drive R_g less effective in switching speed control.
- Fourth, using snubber reduces delay time as lower R_g values can be used to achieve same overshoot with faster dv/dt speed.

For more details on snubber benefits please refer to [2].

Example waveforms with / without snubber

Figure 2. shows the improvement of V_{DS} and V_{GS} waveform of the fast switching SiC device (UF3C120040K3S, TO247-3L) at inductive load hard turn-off with and without the drain-to-source RC snubber. The V_{DS} spike and ringing duration is greatly reduced.

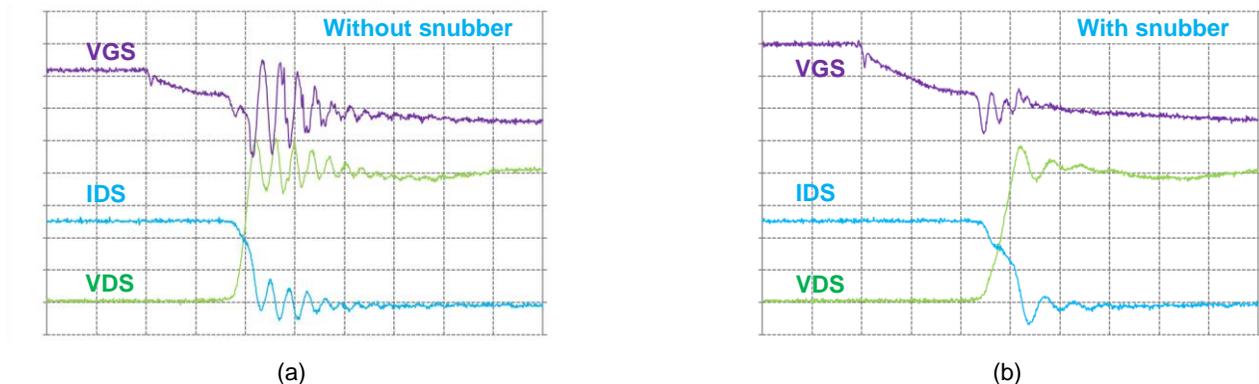


Figure 2. UF3C120040K3S turn-off waveforms without drain-to-source snubber (a), with drain-to-source snubber (b), at V_{DS} 800V, I_D 50A, V_{GS} -5V, R_{goff} 33 Ω . Drain current (IDS) (20A/div), V_{GS} (10V/div), V_{DS} (200V/div), time scale 40ns/div.

Snubber configuration

A typical RC snubber configuration in a half-bridge is shown in **Figure 3**. for hard-switching and ZVS soft-switching applications.

Bus snubber consists of decoupling capacitor (C_d) and resistor (R_d) between the fast-switching half-bridge and DC LINK bulk capacitor.

Device snubber consists of high voltage small footprint capacitor (C_s) and resistor (R_s) across device drain and source terminals.

Load inductor (L) represents inductive load. The DC LINK capacitor has high capacitance to maintain DC bus voltage while providing energy to the load inductor L . C_d is the power loop decoupling capacitor, usually a ceramic capacitor. It is located very close to the half-bridge to minimize power loop stray inductance for switching transients. CT is a current transformer for current measurement.

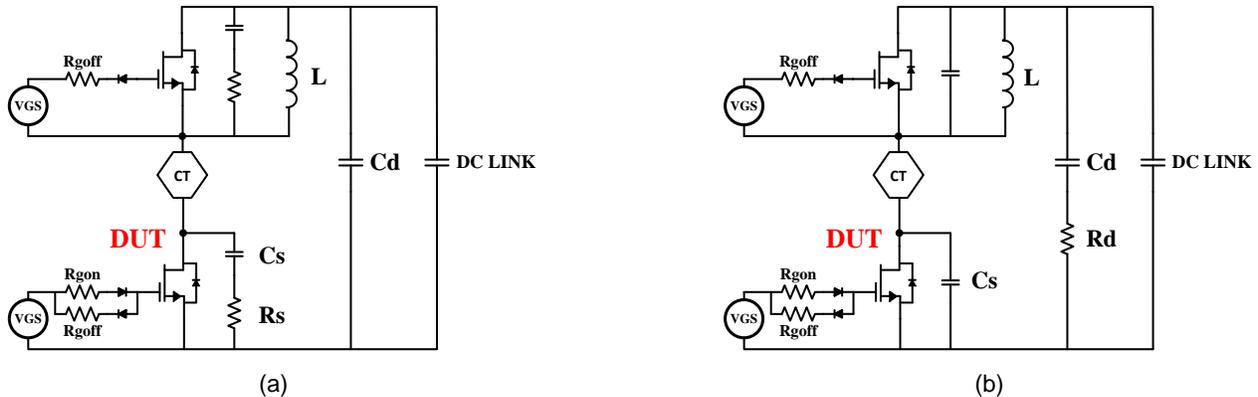


Figure 3. DPT schematic with RC snubbers on both switches for hard-switching (a) and ZVS soft-switching (b).

For hard-switching the device snubber resistor R_s is placed near device drain-to-source to provide best damping effects.

For ZVS soft-switching the device snubber has no resistor R_s in series to avoid R_s energy loss at ZVS turn-on during each soft-switching cycle. Instead, the damping effect is realized by bus snubber resistor R_d which is also series connected in the power loop.

R_s and R_d does generate heat. Although R_s experience loss due to charging and discharging of C_s at every switching cycle, R_s loss is much lower than CV^2 estimation as explained in this [webinar](#) [9]. With sufficient R_d value to provide strong damping effect the R_d loss is dominated by stray inductance energy ($0.5LI^2$) between C_d and DC LINK bulk capacitor. Therefore, R_d loss is layout dependent.

In practice, C_s is key to ensure VDS spike and switching dv/dt are under control at high switching current. For the balance between damping of VDS ringing and snubber resistor loss (R_d and R_s) it is better evaluated by experiment. We strongly recommend designers to measure snubber resistor loss (R_s and R_s) and temperature during the design stage.

To ease thermal dissipation, two SMD resistors can be used in parallel. Also, wide PCB traces or planes are recommended for snubber R_s and R_d terminals for better heat dissipation. In half-bridge, for example, the low side device R_s has access to large GND plane for thermal dissipation while the high side device R_s has access to large DC+ plane for thermal dissipation.

Avoid long-lead

Long device leads introduce more power loop stray inductance creating more ringing and voltage spikes on device GS and DS terminals. This effect is more prominent for UF series with non-kelvin packages (with common source inductance). If long lead is required due to mechanical limits, more device snubber capacitance and higher R_g is required to slow down switching speed to control the ringing and voltage spikes. Therefore, long lead has a significant negative impact on efficiency and waveform.



Figure 4. Long lead (left) vs. short lead (right). Short lead is recommended whenever possible.

Snubber design guides

This SiC FET & module user guide presents practical solutions and guidelines for using RC snubbers with fast switching SiC devices. The solution is verified by experimental double pulse tests (DPT) results. The snubber loss is precisely measured to assist users in computing the power rating of the snubber resistor. The beneficial impact of the snubber is analyzed for both hard switching and soft switching applications. More details can be found in application note entitled "[Switching fast SiC FETs with a snubber](#)".

7 steps to calculate an RC snubber	
Step 1	Measure the VDS turn-off oscillation frequency (f_0). See Figure 1.
Step 2	Add a capacitor (C_1) to device drain-to-source and measure the new shifted oscillation frequency (f_1). Recommendation for a starting value of C_1 is 1-3 times of device energy related output capacitance, $C_{oss(er)}$, at a specified bus voltage. In an example of UF3C120040K4S, the SiC MOSFET $C_{oss(er)}$ at 800V bus is 112pF. C_1 of 300pF is used to have sufficient frequency shift. See Figure 6.
Step 3	Calculate the frequency ratio: $m = f_0/f_1$
Step 4	Calculate the circuit parasitic capacitance: $C_0 = C_1/(m^2 - 1)$
Step 5	Calculate the power loop parasitic inductance: $L = 1/[(2\pi f_0)^2 * C_0]$
Step 6	Calculate the starting snubber capacitor value: $C_1 = 2 * C_0$
Step 7	Calculate the starting snubber resistor value: $R = \sqrt{L/(C_0 + C_1)}$

Figure 5. Device snubber (drain-to-source) design 7 steps [8].

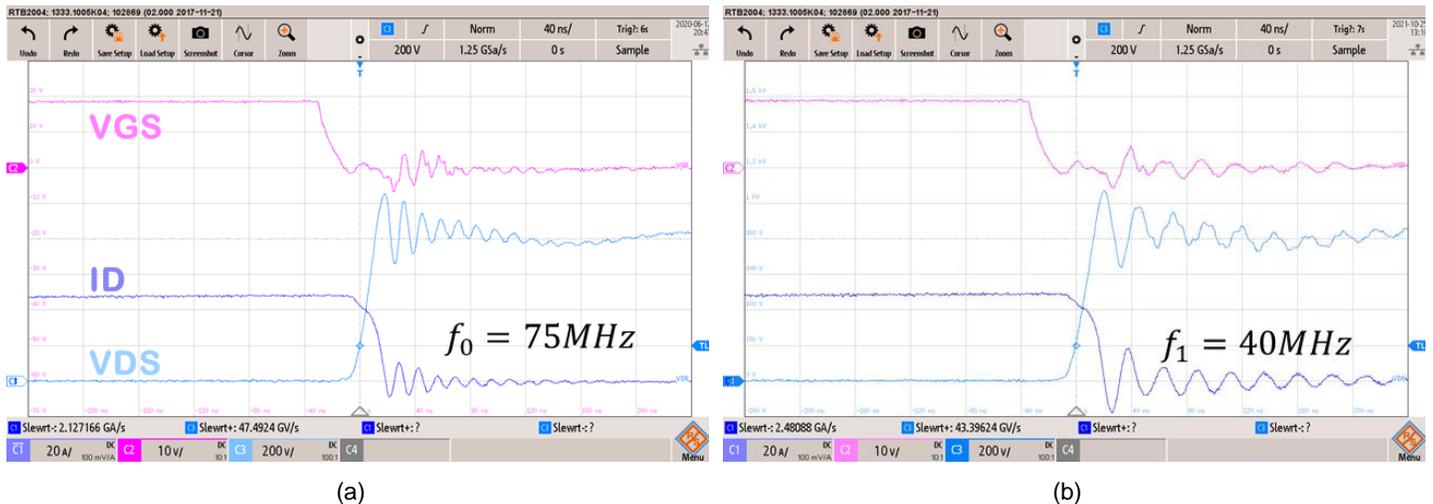


Figure 6. Device snubber (drain-to-source) design step 1 (left) and step 2 (right).

Guidelines for single-gate FETs

Note:

1. $C_{oss(er)}$ is energy related effective output capacitance in datasheet.
2. Device snubber resistor should not be too large, we recommend no more than 5 Ohm.
3. The given value of device snubber for each device provided by the following table is a starting point of evaluation. The optimal value is system dependent and should be verified by experiment in target application.

Snubber Rule	Gen3 3-Lead	Gen3 4-Lead
Cs	$3xC_{oss(er)}$	$2xC_{oss(er)}$
Rs (Ω)	1 to 4.7	1 to 4.7

Snubber Rule	Gen4 3-Lead	Gen4 4-Lead
Cs ($>50m R_{DS(on)}$)	$4xC_{oss(er)}$	Not required
Cs ($<50m R_{DS(on)}$)	$2xC_{oss(er)}$	$2xC_{oss(er)}$
Rs (Ω)	1 to 4.7	1 to 4.7

BOM

Cs (pF)	Series	Part Number	Package	Rated V
47	C0G	202R18N470JV4E	1206	2000V
68		C1206C680JGGAC7800	1206	
100		202R18N101JV4E	1206	
150	C0G	C1206C151JGGAC7800	1206	2000V
220		C1206C221JGGAC7800	1206	
330		C1210C331JGGACTU	1210	
680		C1808C681JGGAC7800	1808	

Notes:

"C0G" ceramic capacitors have most stable capacitance over temperature and voltage variation.

KEMET's X8G HV Class I dielectric features a 150°C maximum operating temperature, offering the latest in high temperature dielectric technology and reliability for extreme temperature applications and under the hood applications. X8G exhibits no change in capacitance with respect to voltage and boasts a minimal change in capacitance with reference to ambient temperature. It is a suitable replacement for higher capacitance and larger footprint devices that fail to offer capacitance stability. Capacitance change is limited to $\pm 30\text{ppm}/^\circ\text{C}$ from -55°C to +150°C. KEMET X8R is available with flexible termination technology which inhibits the transfer of board stress to the rigid ceramic body, therefore mitigating flex cracks which can result in low IR or short circuit failures.

Rs (Ω)	Power Rating (W)	Part Number	Package
4.7	0.5	CRCW08054R70FKEAHP	0805
	0.75	CRCW12104R70JNEAHP	1210
	1	CRCW20104R70JNEFHP	2010
	1.5	CRCW25124R70JNEGHP	2512

Notes:

The parts recommended in this document are all for general uses with functional isolations in mind. Customers need to adapt them to their specific needs in meeting all the regulation requirements. Customers can use slots or use multiple parts in series to increase the creepage distance according to their design requirements. Please pay attention to make the snubber loop as small as possible so that the performance of a snubber won't be impacted too much.

VISHAY "CRCW-HP e3" series provides excellent pulse load capability and AEC-Q200 qualified.

One of the main benefits of the CRCW-HP resistor is the power dissipation which is much higher than power dissipated from standard chip resistor of the same size. For example, a standard 1206 size thick film resistor is rated at 0.25W while CRCW1206-HP is rated at 0.75W. This is mainly achieved by the double-sided printed design. CRCW0805-HP, for instance, is rated at 0.5W, the same power rating as standard 1210 while occupying much less area on the PCB, so there is a significant PCB space that can be saved. This is one of the reasons why the HP series is recommended for densely populated PCBs. The biggest case size of the CRCW-HP series is 2512, rated at 1.5 W. Additionally, CRCW-HP OR Jumper offers much higher maximum current capability in the same package size as a standard OR jumper.

https://www.vishay.com/docs/48634/_crcw-hp_ppt_product_overview_nov2018.pdf

TE Connectivity offers 3540 series of SMD resistors that can handle 4W at 70°C in 2817 size package.



Recommendation table for all part number

Gen 3 SiC FET Usage Table UJ3C and UF3C/SC Devices

Product Name	Package	Vdsmax	Id (25°C)	Id (100°C)	RthjC (Typ)	Rds(on) (25°C)	Rbs(on) (125°C)	Rps(on) (175°C)	Gate Drive Voltage					Device RC Snubber	Rsnub	Csnub	Esnub @ 10A	Esnub @ 30A	Esnub @ 50A	Esnub @ 80A	Coss(er)
									Positive rail RGON			Negative rail RGOFF									
									10V	12V	15V	0V	-5V								
Units		V	A	A	C/W	mΩ	mΩ	mΩ	Ω	Ω	Ω	Ω	Ω		Ω	pF	μJ	μJ	μJ	μJ	pF
650V Devices																					
UJ3C065080T3S	TO220-3L	650	31	23	0.61	80	110	140	5	10	20	5	10	Recommended	4.7	220					77
UJ3C065080K3S	TO247-3L	650	31	23	0.61	80	110	140	5	10	20	5	10	Recommended	4.7	220					
UJ3C065080B3	D2PAK-3L	650	25	18.2	1	80	110	140	5	10	20	5	10	Recommended	4.7	220					
UF3C065080T3S	TO220-3L	650	31	23	0.61	80	110	140	5	10	20	10	20	Required	4.7	220					
UF3C065080K3S	TO247-3L	650	31	23	0.61	80	110	140	5	10	20	10	20	Required	4.7	220					
UF3C065080B3	D2PAK-3L	650	25	18.2	1	80	110	140	5	10	20	10	20	Recommended	4.7	220					
UF3C065080B7S	D2PAK-7L	650	27	20	0.83	80	110	140	15	20	30	5	10	Recommended	4.7	150					
UF3C065080K4S	TO247-4L	650	31	23	0.61	80	110	140	15	20	30	5	10	Recommended	4.7	150					
UF3C065040T3S	TO220-3L	650	54	40	0.35	42	58	78	5	10	20	10	20	Required	4.7	330					150
UF3C065040K3S	TO247-3L	650	54	40	0.35	42	58	70	5	10	20	10	20	Required	4.7	330	16	23			
UF3C065040B3	D2PAK-3L	650	41	30	0.65	42	58	70	5	10	20	10	20	Required	4.7	330					
UF3SC065040B7S	D2PAK-7L	650	43	31.5	0.59	42	58	70	15	20	30	5	10	Recommended	4.7	150					
UF3C065040K4S	TO247-4L	650	54	40	0.35	42	58	70	15	20	30	5	10	Recommended	4.7	150					
UJ3C065030T3S	TO220-3L	650	85	62	0.26	27	35	43	15	20	30	5	10	Recommended	4.7	680					230
UJ3C065030K3S	TO247-3L	650	85	62	0.26	27	35	43	15	20	30	5	10	Recommended	4.7	680	13.8	20.3			
UJ3C065030B3	D2PAK-3L	650	66	47	0.48	27	35	43	15	20	30	5	10	Recommended	4.7	680					



Product Name	Package	Vdsmax	Id (25°C)	Id (100°C)	RthjC (Typ)	Rds(on) (25°C)	Rbs(on) (125°C)	Rps(on) (175°C)	Gate Drive Voltage					Device RC Snubber	Rsnub	Csnub	Esnub @ 10A	Esnub @ 30A	Esnub @ 50A	Esnub @ 80A	Coss(er)
									Positive rail RGON			Negative rail RGOFF									
									10V	12V	15V	0V	-5V								
Units		V	A	A	C/W	mΩ	mΩ	mΩ	Ω	Ω	Ω	Ω	Ω		Ω	pF	μJ	μJ	μJ	μJ	pF
650V Devices																					
UF3C065030T3S	TO220-3L	650	85	62	0.26	27	35	43	15	20	30	10	20	Required	4.7	680					230
UF3C065030K3S	TO247-3L	650	85	62	0.26	27	35	43	15	20	30	10	20	Required	4.7	680	15.8	22.5			
UF3C065030B3	D2PAK-3L	650	66	47	0.48	27	35	43	15	20	30	10	20	Required	4.7	680					
UF3SC065030B7S	D2PAK-7L	650	62	44	0.54	27	35	43	15	20	30	5	10	Recommended	4.7	220					
UF3C065030K4S	TO247-4L	650	85	62	0.26	27	35	43	15	20	30	5	10	Recommended	4.7	220					
UF3SC065007K4S	TO247-7L	650	120	120	0.15	6.7	9.3	11.8	3	5	7	5	10	Recommended	4.7	1000					856
1200V Devices																					
UF3C120400K3S	TO247-3L	1200	7.6	5.9	1.2	410	780	1070	5	10	20	20	30	Recommended	2	47					17.5
UF3C120400B7S	TO247-3L	1200	7.6	5.9	1.2	410	780	1070	15	20	30	20	30	Recommended	2	30					
UJ3C120150K3S	TO247-3L	1200	18.4	13.8	0.7	150	255	330	5	10	20	20	30	Recommended	4.7	100					34
UF3C120150K3S	TO247-3L	1200	18.4	13.8	0.7	150	255	330	5	10	20	20	30	Recommended	4.7	100					
UF3C120150B7S	D2PAK-7L	1200	18.4	13.8	0.7	150	255	330	15	20	30	20	30	Recommended	2	68					
UF3C120150K4S	TO247-4L	1200	18.4	13.8	0.7	150	255	330	15	20	30	20	30	Recommended	2	68					59
UJ3C120080K3S	TO247-3L	1200	33	24	0.45	80	136	172	5	10	20	10	20	Recommended	4.7	150	5	8			
UF3C120080K3S	TO247-3L	1200	33	24	0.45	80	136	172	5	10	20	10	20	Recommended	4.7	150					
UF3C120080B7S	D2PAK-7L	1200	28.8	21	0.61	80	136	172	15	20	30	10	20	Recommended	2	115					
UF3C120080K4S	TO247-4L	1200	33	24	0.45	80	136	172	15	20	30	10	20	Recommended	2	115					
UJ3C120070K3S	TO247-3L	1200	34.5	25.5	0.45	70	111	148	5	10	20	10	20	Recommended	4.7	150					63
UJ3C120070K4S	TO247-3L	1200	34.5	25.5	0.45	70	111	148	15	20	30	10	20	Recommended	4.7	115					



Product Name	Package	Vdsmax	Id (25°C)	Id (100°C)	RthjC (Typ)	Rds(on) (25°C)	Rds(on) (125°C)	Rds(on) (175°C)	Gate Drive Voltage					Device RC Snubber	Rsnub	Csnub	Esnub @ 10A	Esnub @ 30A	Esnub @ 50A	Esnub @ 80A	Coss(er)
									Positive rail RGON			Negative rail RGOFF									
									10V	12V	15V	0V	-5V								
Units		V	A	A	C/W	mΩ	mΩ	mΩ	Ω	Ω	Ω	Ω	Ω		Ω	pF	μJ	μJ	μJ	μJ	pF
1200V Devices																					
UJ3C120040K3S	TO247-3L	1200	65	47	0.27	35	56	73	5	10	20	5	10	Recommended	4.7	330	14.7	21.6			112
UF3C120040K3S	TO247-3L	1200	65	47	0.27	35	56	73	5	10	20	10	20	Required	4.7	330	16.1	23.5			
UF3SC120040B7S	D2PAK-7L	1200	47	34	0.54	35	56	73	15	20	30	5	10	Recommended	4.7	110	6.9	11.4			
UF3C120040K4S	TO247-4L	1200	65	47	0.27	35	56	73	15	20	30	5	10	Recommended	4.7	110					
UF3SC120016K3S	TO247-3L	1200	107	77	0.22	16	26	34	6	8	10	5	10	Required	4.7	680					243
UF3SC120016K4S	TO247-4L	1200	107	77	0.22	16	26	34	6	8	10	5	10	Recommended	4.7	470					
UF3SC120009K4S	TO247-4L	1200	180	130	0.15	8.6	13.8	18.2	3	5	7	5	10	Recommended	4.7	680					395
1700V Devices																					
UF3C170400K3S	TO247-3L	1700	7.6	5.9	1.2	410	780	1070	20	30	40	10	20	Recommended	2	47					15.5
UF3C170400B7S	D2PAK-7L	1700	7.6	5.9	1.2	410	780	1070	10	15	20	5	10	Recommended	2	30					

Notes for Gen 3 products in hard-switching half-bridge applications:

- UF3CxxxxxyK4S gives the highest efficiency. Snubber is recommended to improve EMI.
- UF3CxxxxxyK3S with snubber is a fast solution for 3 lead applications. UF series in 3 terminal packages **MUST** use a snubber for hard-switching.
- Snubber resistor loss is system dependent. Its loss and heat dissipation should be verified in target application.

Notes for Gen 3 products in soft-switching half-bridge applications (LLC, PSFB, etc.):

- DFN8x8, D2PAK-7L, TO247-4L has highest efficiency using low gate resistance (Rg) with Cds across drain-to-source (no Rs).
- UJ3CxxxxxyK3S does not require snubber capacitance (Cds). For RDS(on) >80m, UJ3CxxxxxyK3S provides good balance of EMI & efficiency.
- A bus snubber with a Cds capacitor generally provides the best efficiency and waveforms. 0.1uF bus decoupling capacitor (Cd) is recommended. Cd should be placed as close as possible to half-bridge.



Gen 4 SiC FET Usage Table UJ4C/SC and UF4C/SC Devices

Product Name	Package	Vdsmax	Id (25°C)	Id (100°C)	RthjC (Typ)	Rds(on) (25°C)	Rds(on) (125°C)	Rds(on) (175°C)	Gate Drive Voltage					Device RC Snubber	Rsnub	Csnub	Esnub @ 10A	Esnub @ 30A	Esnub @ 50A	Esnub @ 80A	Coss(er)
									Positive rail RGON			Negative rail RGOFF									
									10V	12V	15V	0V	-5V								
Units		V	A	A	C/W	mΩ	mΩ	mΩ	Ω	Ω	Ω	Ω	Ω		Ω	pF	μJ	μJ	μJ	μJ	pF
750V Devices																					
UJ4SC075005L8S	MO-229	750	120	120	0.1	5.4	9.3	12.2	3	5	7	5	10	Required	4.7	680					475
UJ4SC075006K4S	TO247-4L	750	120	120	0.16	5.9	9.8	12.9	3	5	7	5	10	Required	4.7	680	18	21	32	60	475
UJ4SC075008L8S	MO-229	750	106	106	0.19	8.6	14.4	19	3	5	7	5	10	Required	4.7	560					286
UJ4SC075009K4S	TO247-4L	750	106	86	0.31	9	14.8	19.4	3	5	7	5	10	Required	4.7	560	15	25	33	60	286
UJ4SC075009B7S	D2PAK-7L	750	106	86	0.31	9	14.8	19.4	3	5	7	5	10	Required	4.7	560					
UJ4SC075010L8S	MO-229	750	106	92	0.21	10.7	18.1	24	4	6	8	5	10	Required	4.7	470					225
UJ4SC075011K4S	TO247-4L	750	104	75	0.33	11	18.4	24.2	6	8	10	10	20	Required	4.7	390	15	20	26	43	225
UJ4SC075011B7S	D2PAK-7L	750	104	75	0.33	11	18.4	24.2	6	8	10	10	20	Required	4.7	390					
UJ4C075018K4S	TO247-4L	750	81	60	0.3	18	31	41	15	20	30	20	30	Recommended	4.7	300					150
UJ4C075018K3S	TO247-3L	750	81	60	0.3	18	31	41	15	20	30	20	30	Recommended	4.7	300					
UJ4SC075018B7S	D2PAK-7L	750	81	60	0.45	18	29	37	15	20	30	20	30	Recommended	4.7	300					
UJ4SC075018L8S	MO-229	750	81	60	0.33	18	29	37	15	20	30	20	30	Recommended	4.7	300					
UJ4C075023K4S	TO247-4L	750	66	49	0.38	23	39	50	5	10	15	5	10	Recommended	4.7	200	8	17	25		116
UJ4C075023K3S	TO247-3L	750	66	49	0.38	23	39	50	15	20	30	50	55	Recommended	4.7	200	7	12	17		
UJ4C075023B7S	D2PAK-7L	750	66	49	0.38	23	39	50	5	10	15	5	10	Recommended	4.7	200					83
UJ4C075023L8S	MO-229	750	64	46	0.42	23	39	50	5	10	15	5	10	Recommended	4.7	200					
UJ4C075033K4S	TO247-4L	750	47	39	0.48	33	57	75	10	15	20	10	15	Recommended	4.7	100	7	12	24		
UJ4C075033K3S	TO247-3L	750	47	39	0.48	33	57	75	15	20	30	50	55	Recommended	4.7	100	6	11	15		66
UJ4C075033B7S	D2PAK-7L	750	47	39	0.48	33	57	75	10	15	20	10	15	Recommended	4.7	100					
UJ4C075033L8S	MO-229	750	44	33	0.56	33	57	75	10	15	20	10	15	Recommended	4.7	100					
UJ4C075044K4S	TO247-4L	750	37.4	27.6	0.57	44	75	101	3	4	5.6	22	27	Required	4.7	330	11	16			66
UJ4C075044K3S	TO247-3L	750	37.4	27.6	0.57	44	75	101	30	40	50	50	55	Required	4.7	330					
UJ4C075044B7S	D2PAK-7L	750	37.4	27.6	0.57	44	75	101	3	4	5.6	22	27	Required	4.7	330					
UJ4C075044L8S	MO-229	750	35.6	26	0.64	44	75	101	3	4	5.6	22	27	Required	4.7	330					



Product Name	Package	Vdsmax	Id (25°C)	Id (100°C)	RthjC (Typ)	Rbs(on) (25°C)	Rbs(on) (125°C)	Rbs(on) (175°C)	Gate Drive Voltage					Device RC Snubber	Rsnub	Csnub	Esnub @ 10A	Esnub @ 30A	Esnub @ 50A	Esnub @ 80A	Coss(er)
									Positive rail RGON			Negative rail RGOFF									
									10V	12V	15V	0V	-5V								
Units		V	A	A	C/W	mΩ	mΩ	mΩ	Ω	Ω	Ω	Ω	Ω		Ω	pF	μJ	μJ	μJ	μJ	pF
750V Devices																					
UJ4C075060K4S	TO247-4L	750	28	20.6	0.75	58	106	147	2	3	5	10	15	Recommended	4.7	330					50
UJ4C075060B7S	D2PAK-7L	750	28	20.6	0.75	58	106	147	2	3	5	10	15	Recommended	4.7	330					
UJ4C075060L8S	MO-229	750	27.8	20.6	0.75	58	106	147	2	3	5	10	15	Recommended	4.7	330					
UJ4C075060K3S	TO247-3L	750	28	20.6	0.75	58	106	147	2	3	5	10	15	Recommended	4.7	330					
1200V Devices																					
UF4SC120023K4S	TO247-4L	1200	53	52	0.3	23	42	57	5	10	15	5	10	Recommended	4.7	100	6	7.5	9		108
UF4SC120023B7S	D2PAK-7L	1200	70	51	0.3	23	42	62	5	10	15	5	10	Recommended	4.7	100	6	7.5	9		
UF4SC120030K4S	TO247-4L	1200	56	41	0.34	30	56	77	15	22	27	27	30	Required	1	560			27	40	82
UF4SC120030B7S	D2PAK-7L	1200	56	41	0.34	30	56	77	15	22	27	27	30	Required	1	560					
UF4C120053K4S	TO247-4L	1200	34.5	25.6	0.44	53	112	159	2	3	5	10	15	Not Required							54
UF4C120053B7S	D2PAK-7L	1200	34	24.6	0.46	53	112	159	2	3	5	10	15	Not Required							54
UF4C120053K3S	TO247-3L	1200	34.5	25.6	0.44	53	112	159	2	3	5	10	15	Recommended	4.7	220					54
UF4C120070K4S	TO247-4L	1200	27.5	20.7	0.53	70	140	197	2	3	5	10	15	Not Required							42
UF4C120070B7S	D2PAK-7L	1200	25.7	19.2	0.63	72	140	197	2	3	5	10	15	Not Required							42
UF4C120070K3S	TO247-3L	1200	27.5	20.7	0.53	70	140	197	2	3	5	10	15	Recommended	4.7	220					42

Notes for Gen 4 products in hard-switching half-bridge applications:

- All Gen 4 750V devices are measured with a 2.5Ω, 100nF bus snubber
- All Gen 4 750V TO247-3L devices **require** either a 2.5Ω, 100nF Bus snubber or a recommended device snubber (across device drain-to-source).
- For switching currents above 20A per device, a device snubber is **required**, except for 1200V 53mΩ & 1200V 70mΩ in TO247-4L.
- Snubber resistor loss is system dependent. Its loss and heat dissipation should be verified in target application.
- Target application for UG series is with very high currents and relatively slow dv/dt (<20V/ns) like circuit protection, etc.



SiC E1B Module Usage Table

Product Name	Package	Vdsmax	Id (25°C)	Id (100°C)	RthjC (Typ)	RDS(on) (25°C)	RDS(on) (125°C)	RDS(on) (150°C)	Gate Drive Voltage					Device RC Snubber	Rsnub	Csnub	Esnub @ 10A	Esnub @ 30A	Esnub @ 50A	Esnub @ 80A	Coss(er)
									Positive rail RGON			Negative rail RGOFF									
									10V	12V	15V	0V	-5V								
Units		V	A	A	C/W	mΩ	mΩ	mΩ	Ω	Ω	Ω	Ω	Ω		Ω	pF	μJ	μJ	μJ	μJ	pF
1200V Devices																					
UHB50SC12E1BC3N	E1B HB	1200	69	45	0.46	19	30	35	10	12	15	4.7	4.7	Recommended	4.7	560					240
UHB100SC12E1BC3N	E1B HB	1200	100	88	0.23	9.4	15	17.5	10	12	15	4.7	4.7	Recommended	4.7	680					480
UFB15C12E1BC3N	E1B FB	1200	24	16	1	70	111	129	20	24	30	10	10	Recommended	4.7	270					63
UFB25SC12E1BC3N	E1B FB	1200	36	23	0.85	35	55	64	20	24	30	10	10	Recommended	4.7	330					120

Notes for SiC E1B modules:

- Snubbers are strongly recommended for SiC E1B modules due to their intrinsic fast-switching speed. Also, snubber greatly reduces turn-off switching loss making SiC E1B modules extremely attractive in ZVS (zero voltage turn-on) soft-switching applications such as phase-shifted full-bridge (PSFB), LLC, etc.
- This product is recommended for use with **solder pin attach** for PCB assembly and **phase change thermal interface materials** for heatsink assembly. It is **NOT** recommended using press fit for PCB assembly and application of thermal grease for heatsink assembly. Please refer to E1B module [mounting guidelines](#) and [technical overview](#) documents for detailed information.

Important Notice

The information contained in this Data Sheet and any associated documents (“Data Sheet Information”) is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.

© 2020 Qorvo US, Inc. All rights reserved. This document is subject to copyright laws in various jurisdictions worldwide and may not be reproduced or distributed, in whole or in part, without the express written consent of Qorvo US, Inc. | QORVO® is a registered trademark of Qorvo US, Inc.