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# High Performance GaN Thermal Evaluation - Limitations of Infrared Microscopy

*Dylan Murdock, Mechanical Engineer - Advanced Packaging, Infrastructure & Defense Products, Qorvo*
*Mark C. Woods, Mechanical Engineer - Advanced Packaging, Infrastructure & Defense Products, Qorvo*

## Abstract

This paper addresses the limitations of infrared microscopy when used to measure high performance microwave GaN HEMT devices and MMICs. It will also describe Qorvo's integrated approach to thermal analysis which leverages modeling, empirical measurements (including micro-Raman thermography), and finite element analysis (FEA). This methodology is highly effective and has been empirically validated. By acknowledging the limitations of infrared microscopy, predictions and measurements can be made more accurate than traditional methods developed with lower power density technology.

## GaN Device Thermal Estimates

Qorvo's approach to thermal estimates for GaN product datasheets follows the process illustrated in Figure 1. To construct the baseline thermal model for a given process, an electrical simulation of the GaN device using non-linear models for the field effect transistors is used to obtain estimates of heat generation which allow for an initial prediction of thermal performance. The device is then physically fabricated and tested.

Empirical thermal data is collected with both electrical measurements and micro-Raman measurements. Raman thermography is a non-invasive optical technique, based on Raman scattering spectroscopy, that enables temperature measurements with sub-micron spatial and nanosecond time resolution.[1] It probes the temperature-induced phonon shift in a material, with respect to a reference phonon frequency measured at ambient temperature.[2] Additional details on experimental setups and applications of micro-Raman thermography are described in [1,2].

Raman thermography has been established as an important high fidelity regimen for physically small geometries. It offers proven, accurate and repeatable improvement in spatial resolution down to 0.5μm as well as micron-scale depth resolution for true 3D thermography. As will be discussed below, Raman thermography improves upon the underestimation of device peak temperature due to lateral spatial averaging associated with conventional infrared (IR) thermography measurements.

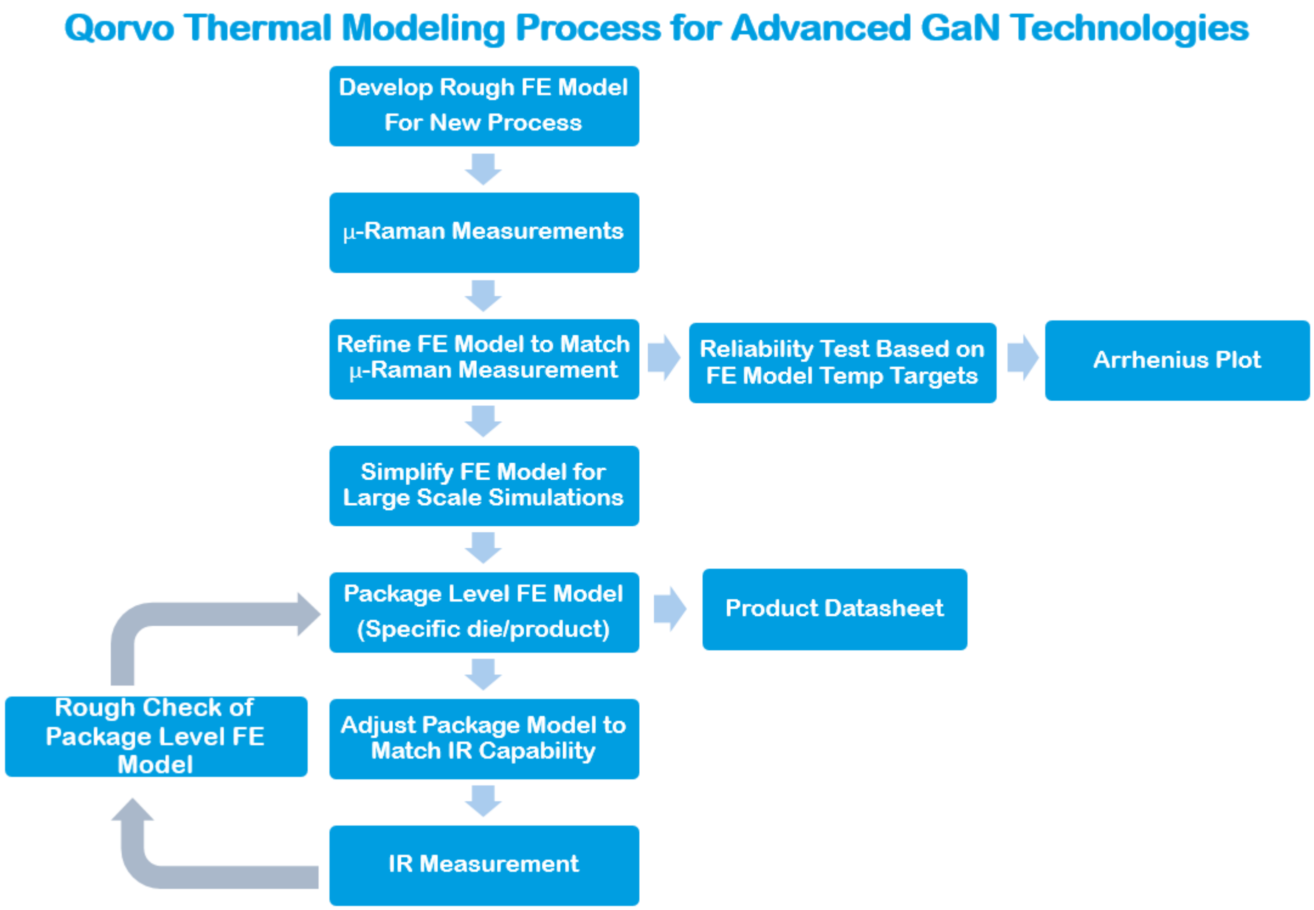


***Figure 1: GaN Thermal Modeling Process***

A combination of measurement methods, including micro-Raman and electrical, should be used in conjunction with thermal simulations, in order to gain accurate information on the thermal properties of GaN devices.

Using the measured data as the empirical baseline, an FEA model is constructed, which then becomes the baseline for modeling and predicting thermal performance. There are typically multiple iterations between the micro-Raman measurements and the FEA in order to build models that provide good correlation over different geometries and material stack-ups.

Finite element simulations are used to determine the power and environmental conditions required to run devices at specific elevated temperatures in order to properly accelerate and measure the life of the device. This measured life data is used for construction of a device reliability Arrhenius plot. Today's GaN transistors include gate lengths measuring down to 0.15μm in size and lower, meaning that there is still some area-averaging that occurs with micro-Raman thermography. With this methodology these averages are reflected in both the thermal model and device reliability Arrhenius plots. This process enables a tightly-coupled mean time to failure (MTTF) curve and product level thermal analysis that accurately predicts product life.

Once the baseline thermal model development is complete, FEA is then employed to accurately predict channel temperature and thermal resistances at the product level. The FEA begins with a die-level simulation, proceeds to the package level, and continues all the way to system level, where it examines the packaged product within the next higher assembly.  Figure 2 shows a typical device-level FEA thermal model.

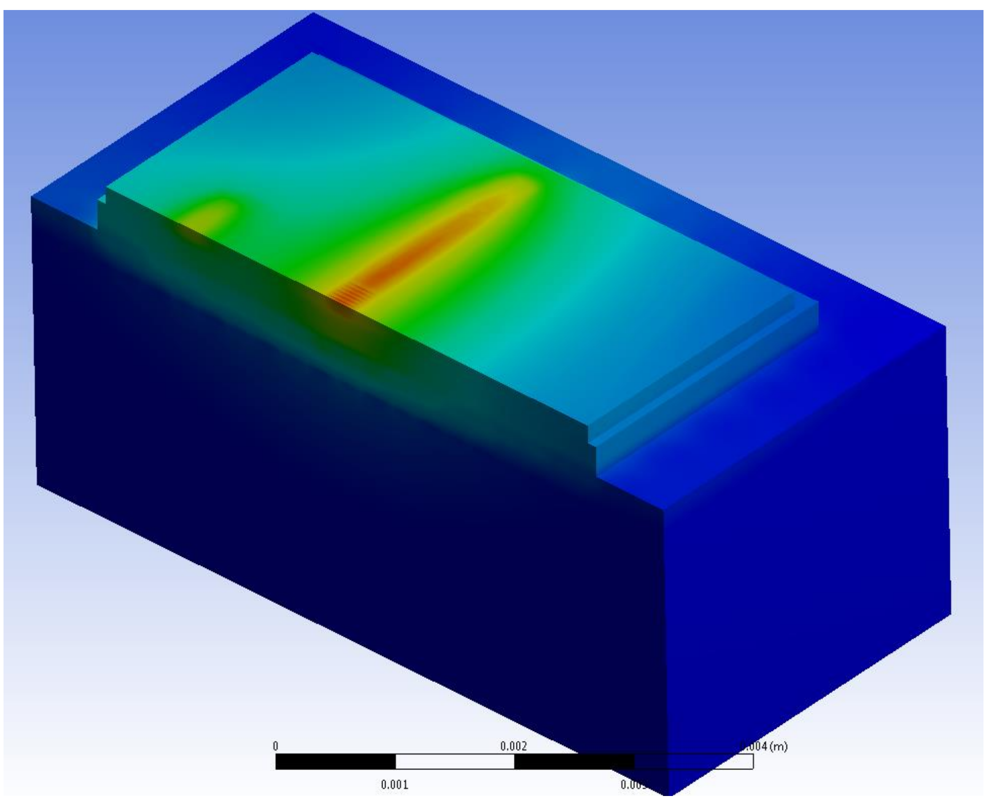


***Figure 2: GaN device-level thermal model***

When modeling and measuring heat generation and removal, it is critical to select proper boundary conditions and to understand the impact of those assumptions. Commonly, unrealistic or improper assumptions are made on temperature and heat removal boundary conditions. The unrealistic predictions and measurements that result often lead to product designs that appear to work well on a datasheet, but will fail in application.

Finally, the FEA model is simplified to represent the low-detail image that an IR microscope can resolve, along with its synthetically low measurement result. This modified model is then compared against IR microscopy measurements to empirically inspect for gross error.

**Using Infrared Microscopes with GaN Devices**

Infrared (IR) microscopes are widely-used for determining fault location by searching for hot spots in semiconductor devices. However the application of IR for thermal characterization is limited due to spatial resolution incompatibility. IR microscopes cannot resolve a spot size as small as the active area of a GaN transistor. Therefore, IR measurement necessarily averages-in colder, non-active areas with the active area that needs to be measured. In other words, when an IR measurement is taken of a feature that is only 0.25µm wide, for example, the resultant temperature reading can be 25% cooler than the peak temperature of that feature. An example IR image of a discrete GaN transistor is shown in Figure 3.

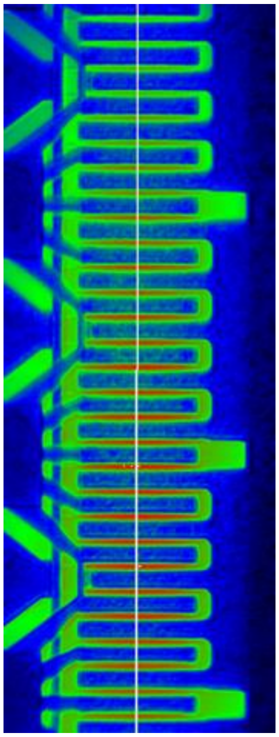

***Figure 3: IR image of a typical GaN FET cell***

A typical IR microscope collects light in the Mid Wave Infrared (MWIR) spectrum. The theoretical spatial resolution limits of MWIR measurement can be calculated using Rayleigh's resolution criteria:

$$D = \frac{0.61\lambda}{N.A.}$$

D = distance between resolvable targets

λ = wavelength (3-5µm for MWIR)

N.A. = numerical aperture (cannot exceed 1, typically near 0.9 in application)

The result is a theoretical lower limit on spot size of roughly 2.5µm. Since today's GaN geometries are an order of magnitude smaller, peak channel temperatures cannot be resolved.

To demonstrate the impact of IR resolution limits when measuring GaN devices, a half symmetry finite element model of a GaN device was constructed. The model assumes bilateral symmetry about the y-axis. This simulation places the device on a .040" thick copper-tungsten base with AuSn die-attach. A boundary condition of 85$^{o}$C has been applied at the base of the CuW.

A volumetric heat load typical of GaN devices has been applied beneath the channel; the resulting 3D temperature field is shown in the contour plot of Figure 4(a) and the corresponding surface temperature is shown in Figure 4(b).

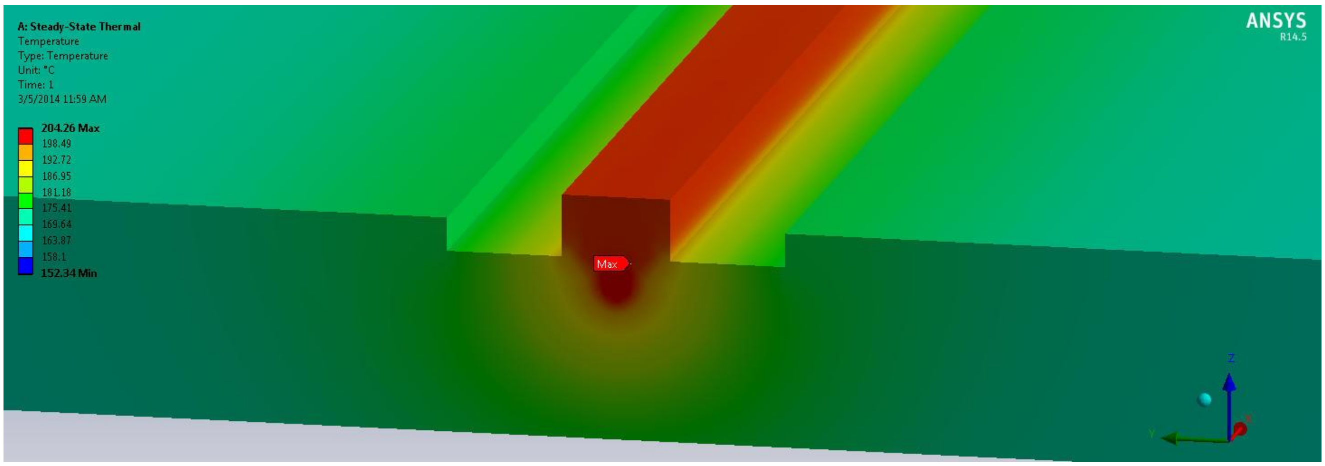


***Figure 4(a): Temperature field in the ~2 micron thick GaN layer above the SiC substrate***

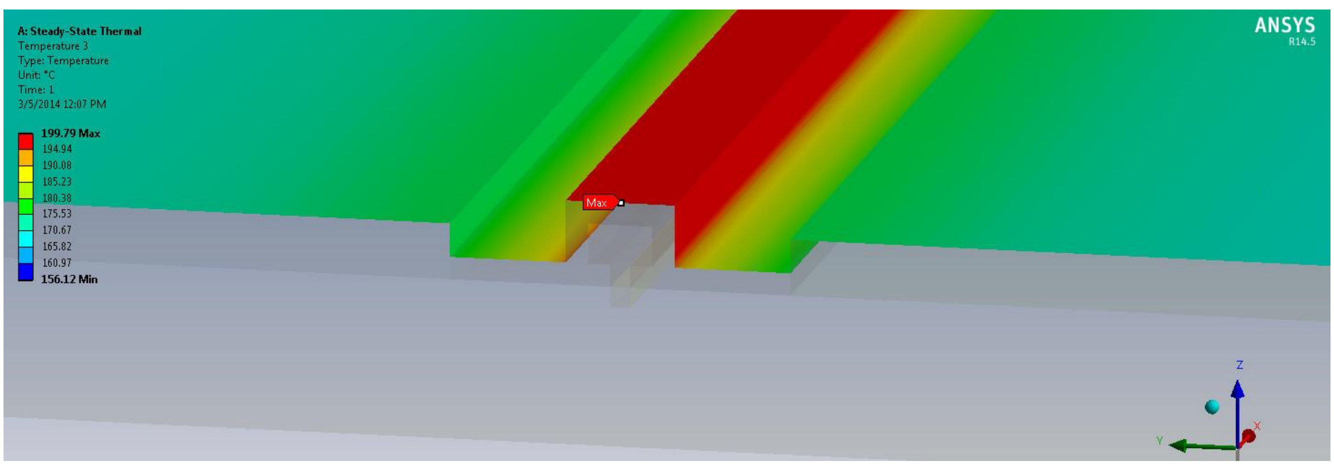


***Figure 4(b): Surface temperature above the gate***

The peak temperature recorded in the simulation is 204ºC at the midpoint of the GaN channel (x = 0 for this half-model). This condition occurs below the surface of the substrate and cannot be imaged by infrared thermography.

Table 1 lists the maximum and average temperatures for the surface regions as would be recorded by IR microscopes with spatial resolution limits representative of the technology. These surface regions are pictured in Figures 5(a) through 5(d).

**Table 1: FEA Temperature Solution vs. IR Measurement, Resolution Error**

| Measured Body or Area | Size (μm x μm) | Pixel Alignment to Hot Spot | True Maximum Temp., ºC | Surface Temp. as Measured with IR, ºC |
|---|---|---|---|---|
| Simulated GaN Device | - | - | 204.3 | - |
| Surface region #1 | 2.5 x 2.5 | centered | - | 195.9 |
| Surface region #2 | 2.5 x 2.5 | offset | - | 189.1 |
| Surface region #3 | 5.0 x 5.0 | centered | - | 188.3 |
| Surface region #4 | 5.0 x 5.0 | offset | - | 183.0 |

In this ideal example, the application of infrared thermography to image a 2.5μm x 2.5μm area, a representative IR resolution limit, of the surface above the channel results in a measurement which underestimates the peak channel temperature by 8-15$^{o}$C. The range of offset is caused by an inability to precisely align the center of one pixel on top of the hottest section of a channel. Figures 5(b) and 5(d) show the impact of having the pixel alignment such that the channel lies at the boundary of the area imaged by the pixel. In this case, the average surface temperature of a 2.5μm x 2.5μm area underestimates maximum channel temperature by more than 15$^{o}$C. Using a 5μm x 5μm area pushes the error to 21$^{o}$C.

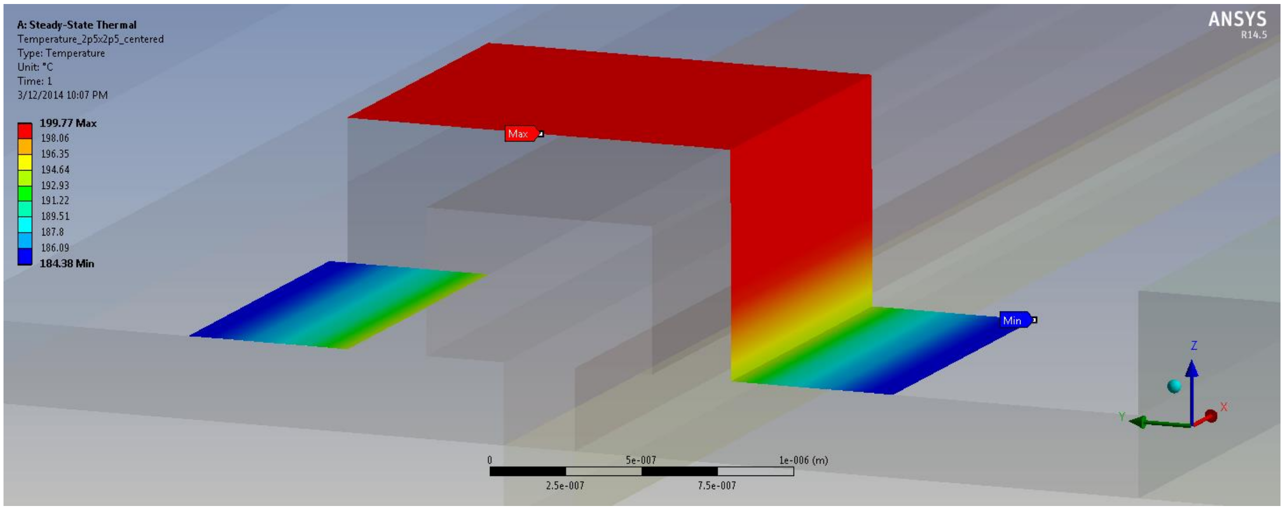


***Figure 5(a) Surface Region #1: Width = 2.5 microns (centered over hottest part of channel)***

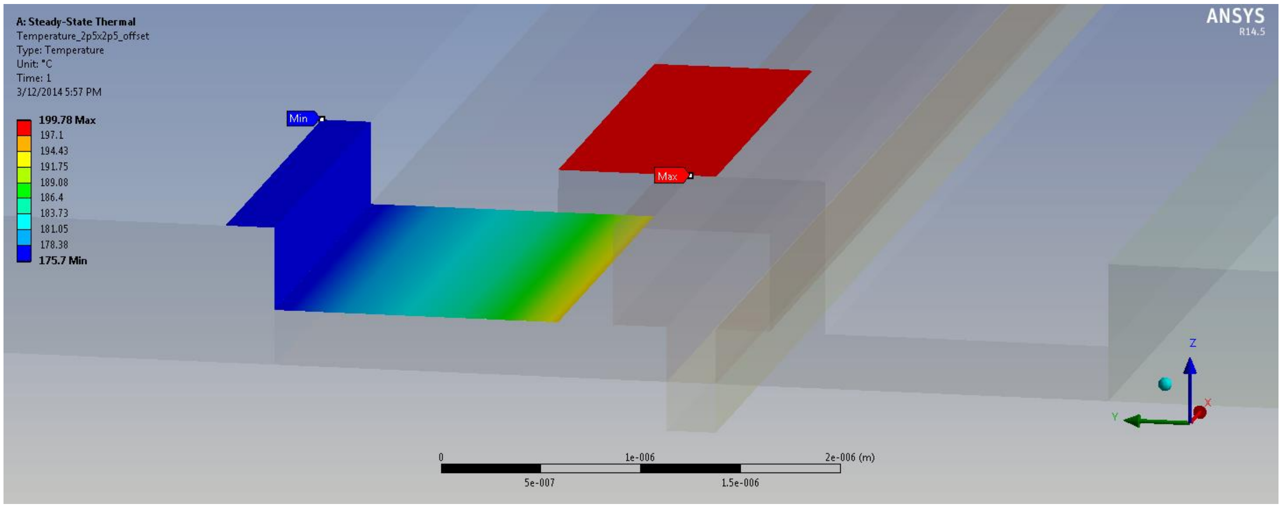


***Figure 5(b) Surface Region #2: Width = 2.5 microns (offset in both x and y)***

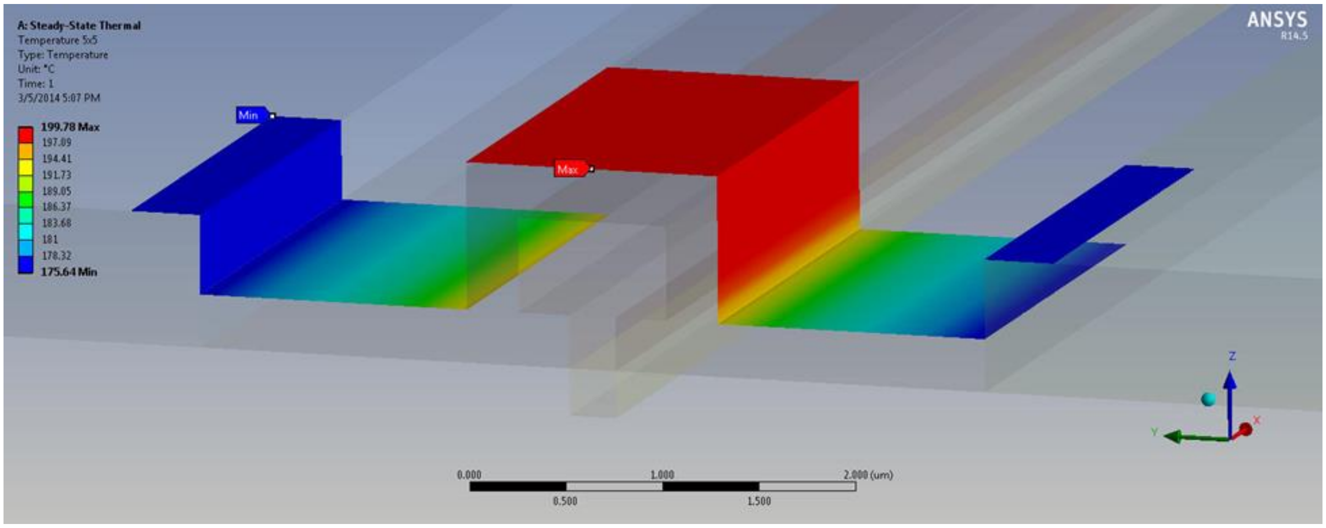


***Figure 5(c) Surface Region #3: Width = 5 microns (centered over hottest part of channel)***

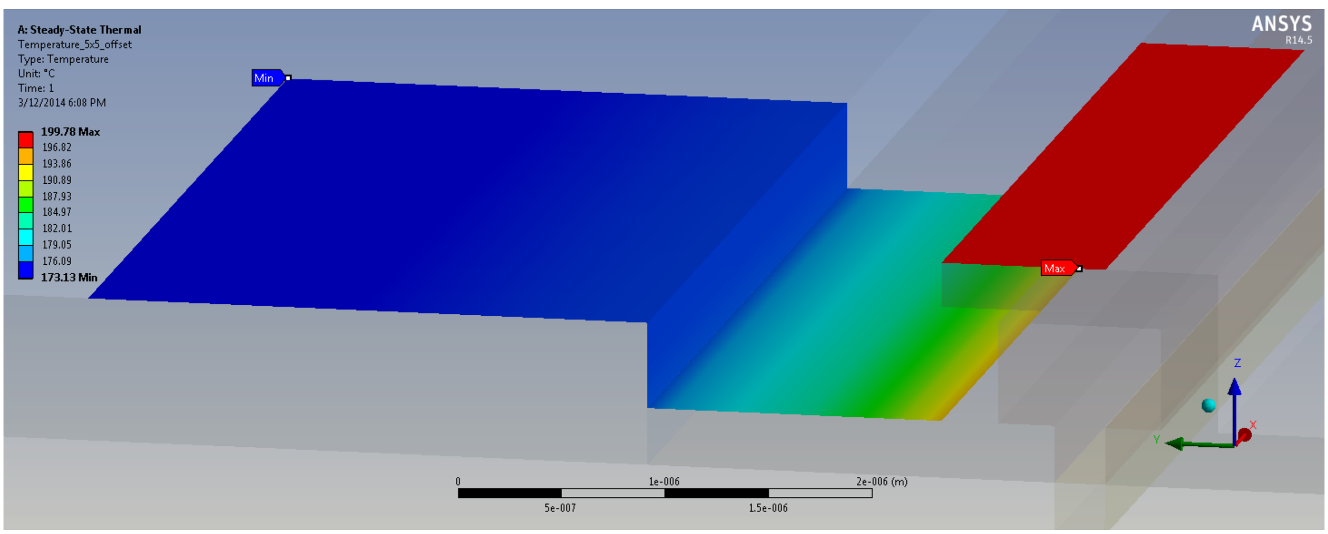


***Figure 5(d) Surface Region #4: Width = 5 microns (offset in both x and y)***

In the case of GaN thermal analysis, sub-micron processes are used to make the transistors, with hotspots that are significantly smaller than 0.25µm, and IR microscopy is only capable of resolving - in complete detail - something that is an order of magnitude larger.

Additionally, IR thermography only measures the surface temperature of the transistor, whereas the peak temperature actually occurs below the surface, in the gallium nitride epitaxy. This reduction in measured temperature is exaggerated during pulsed operation where the thermal time constant of the semiconductor material above the heat source dampens the measured temperature range.

Finally, emissivity (ε) on the surface of a die varies significantly. The common solution is to paint the die matte black to achieve a near $\varepsilon = 1$, but a true and consistent blackbody cannot be created. Another challenge this creates is that paint imparts a dielectric load on the die, which can be difficult to predict and is typically inconsistent. This changes RF performance and as a result, accuracy and repeatability suffer.

**Table 2: FEA Temperature Solution vs. IR Measurement, Total Error**

| Measured Body or Area | Size (μm x μm) | Emissivity | True Maximum Temp., ºC | Surface Temp. as Measured with IR, ºC |
|---|---|---|---|---|
| Simulated GaN Device | - | - | 204.3 | - |
| Surface Area | 2.5 x 2.5 | 1.00 | - | 189.1 |
| Surface Area | 2.5 x 2.5 | 0.85 | - | 171.7 |
| Surface Area | 5.0 x 5.0 | 1.00 | - | 183.0 |
| Surface Area | 5.0 x 5.0 | 0.85 | - | 164.9 |

The effects of emissivity are included in this extension of the previous example. Here it is shown that IR thermography underestimates peak GaN channel temperatures by as much as 40ºC for the conditions listed.

The modeling results above demonstrate the importance of compatible and consistent thermal measurement techniques for GaN devices. Employing tools and techniques originally developed for lower-power semiconductor technology and/or larger geometries can cause significant errors; these errors can lead to incorrect reliability estimates and compromised product function. Qorvo's thermal design and analysis process has been developed for GaN using the most sensitive measurement tools available today and represents industry-leading accuracy.

**References**


[1] N. Killat and M. Kuball, University of Bristol, H.H. Wills Physics Laboratory; T.-M. Chou, U. Chowdhury, and J. Jimenez, Qorvo, Inc. *Temperature Assessment of AlGaN/GaN HEMTs: A Comparative study by Raman, Electrical and IR Thermography*

[2] J. Pomeroy, M. Bernardoni, M. Kuball, H.H. Wills Physics Laboratory, University of Bristol; D.C. Dumka, D.M. Fanning, Qorvo, Inc. *Low Thermal Resistance GaN-on-Diamond Transistors Characterized by 3-D Raman Thermography Mapping*

[3] S. Kiefer, M. Nair, P. Sanders, J. Steele, M. Sutton, R. Thoma, S. Wilson, Motorola Digital DNA Laboratories; G. Albright, C. Li, J. McDonald, Quantum Focus Inc. *Infrared Microthermography for Integrated Circuit Fault Location; Sensitivity and Limitations*