

Introduction

This document describes the design of a 10-W power amplifier for the 2.0–2.7 GHz bands using Modelithics' T2G6000528 Angelov model. This model was developed by Modelithics in Tampa, Florida, and is the result of a cooperative effort between TriQuint and Modelithics.

The simulation design described below demonstrates that the model can effectively support designers who do not have access to load pull measurement data or the means to carry out complex load pull tasks. The model is also useful for designers who require quick turnaround designs.

Design Parameters

For demonstration purposes, the design goal was limited to simulating an amplifier that could provide flat saturation power across the 2.0–2.7 GHz bands, which is commonly used by the communications industry. While the main goal was to observe the saturation power, other parameters such as gain, efficiency, and return loss were also closely watched.

Design Steps

The design steps from model simulation to layout realization are described. The method used can also be used for other design goals, which can be achieved by thoroughly analyzing the simulated load pull data. The simulation software used was Agilent Technologies' Advanced Design System (ADS) 2012. The software used for data analysis was MATLAB® from MathWorks.

Load and Source Pull

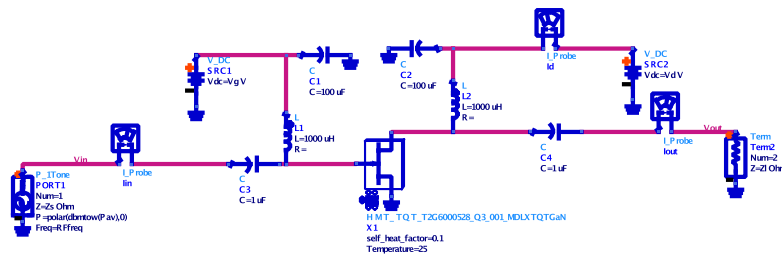
To select the appropriate source and load impedances, the following steps were used:

1. Perform source pulling for maximum gain.
2. Perform load pulling for maximum saturation power.

These steps were repeated until the source and load impedances no longer significantly changed.

A typical setup for an ADS load or source pull simulation environment has a fixed input or output impedance while varying or pulling the impedance of the other end. The contours of a parameter such as 3-dB compression power represent the impedances over which a constant parametric value is obtained. This type of setup resembles the actual load pull setup. However, simulation does not require the design and calibration of load pull fixtures.

Figure 1 shows the setup of the load pull in the ADS simulation environment. Other simulation settings used were $V_d = 28$ V, $I_{dq} = 50$ mA, pulse duty cycle = 10 percent, temperature = 25°C. The model version was 1.4.8.



OPTIONS

Options
Options1
Temp=25
TNoise
V_Refl=5e-5
V_AbsTol=1e-5V
L_Refl=5e-5
L_AbsTol=1e-5A
GiveAWARNING=0
NewWarnings=0

PARAMETER SWEEP

ParamSweep
SweepReGamma
SweepParam="ReGamma"
SInstanceName[1]="Sweep_InGamma"
SInstanceName[2]
SInstanceName[3]
SInstanceName[4]
SInstanceName[5]
SInstanceName[6]
Start=gr_start
Stop=gr_stop
Steps=1

PARAMETER SWEEP

ParamSweep
SweepReGamma
SweepParam="InGamma"
SInstanceName[1]="HB1"
SInstanceName[2]
SInstanceName[3]
SInstanceName[4]
SInstanceName[5]
SInstanceName[6]
Start=gr_start
Stop=gr_stop
Steps=1

HARMONIC BALANCE

HarmonicBalance
HB1
Freq[1]=R.Freq
Order[1]=7
MaxIter=
SweepParam="Pav"
StartPav_start
StopPav_stop
Steps=1

VAR

VAR2
HarmonicImpedance=
Z1=LoadArray[Load]
Z2=SourceArray[Load]
LoadArray=ReflZ1,Z1,Z2,Z3
SourceArray=ReflZ2,Z1,Z2,Z3
GammaL1_mag=refl0.95,angleGamma_j
GammaL1_L_phase=ReGamma_j
GammaL1_L_mag=GammaL1_mag*exp(j*GammaL1_ph*3.1416/180)
f[1]=Z0*(1+)(1-x)
Z0=50
Z01=25

VAR

VAR3
Z1=fg(GammaS,1,Z0)
Z2=fg(GammaS,2,Z0)
Z3=fg(GammaS,3,Z0)
Z11=fg(GammaL,2,Z0)
Z12=fg(GammaL,2,Z0)
Z13=fg(GammaL,2,Z0)
Pav=0
ReGamma=0
InGamma=0

28V	
25mA	-2.634V
-25mA	-2.950V

28V, 50mA, 2.0GHz	
VAR Terminal_Loadings13	VAR Terminal_Loadings14
GammaS 1-0.217j*0.402	GammaS 1-0.263j*0.440
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias27	VAR Bias28
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.0 GHz	RFFreq=2.1 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.3	gr_start=0.3
gr_stop=0.6	gr_stop=0.6
gfm_start=0.3	gfm_start=0.3
gfm_stop=0.6	gfm_stop=0.6

28V, 50mA, 2.1GHz	
VAR Terminal_Loadings13	VAR Terminal_Loadings14
GammaS 1-0.217j*0.402	GammaS 1-0.263j*0.440
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias27	VAR Bias28
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.0 GHz	RFFreq=2.1 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.3	gr_start=0.3
gr_stop=0.6	gr_stop=0.6
gfm_start=0.3	gfm_start=0.3
gfm_stop=0.6	gfm_stop=0.6

28V, 50mA, 2.2GHz	
VAR Terminal_Loadings3	VAR Terminal_Loadings9
GammaS 1-0.333j*0.387	GammaS 1-0.341j*0.389
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias28	VAR Bias20
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.2 GHz	RFFreq=2.3 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.5	gr_start=0.5
gr_stop=0.5	gr_stop=0.5
gfm_start=0.3	gfm_start=0.4
gfm_stop=0.5	gfm_stop=0.6

28V, 50mA, 2.4GHz	
VAR Terminal_Loadings5	VAR Terminal_Loadings8
GammaS 1-0.264j*0.391	GammaS 1-0.322j*0.411
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias21	VAR Bias22
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.4 GHz	RFFreq=2.5 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.5	gr_start=0.4
gr_stop=0.5	gr_stop=0.6
gfm_start=0.4	gfm_start=0.4
gfm_stop=0.6	gfm_stop=0.6

28V, 50mA, 2.5GHz	
VAR Terminal_Loadings11	VAR Terminal_Loadings12
GammaS 1-0.301j*0.467	GammaS 1-0.313j*0.565
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias25	VAR Bias26
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.5 GHz	RFFreq=2.7 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.4	gr_start=0.6
gr_stop=0.5	gr_stop=0.5
gfm_start=0.4	gfm_start=0.5
gfm_stop=0.6	gfm_stop=0.6

28V, 50mA, 2.6GHz	
VAR Terminal_Loadings11	VAR Terminal_Loadings12
GammaS 1-0.301j*0.467	GammaS 1-0.313j*0.565
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias25	VAR Bias26
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.6 GHz	RFFreq=2.7 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.4	gr_start=0.6
gr_stop=0.5	gr_stop=0.5
gfm_start=0.4	gfm_start=0.5
gfm_stop=0.6	gfm_stop=0.6

28V, 50mA, 2.7GHz	
VAR Terminal_Loadings12	VAR Terminal_Loadings12
GammaS 1-0.313j*0.565	GammaS 1-0.313j*0.565
GammaS 2-0	GammaS 2-0
GammaS 3-0	GammaS 3-0
GammaL 2-0	GammaL 2-0
GammaL 3-0	GammaL 3-0
VAR Bias26	VAR Bias26
Vg=-2.634	Vg=-2.634
Vd=28	Vd=28
RFFreq=2.7 GHz	RFFreq=2.7 GHz
Pav_start=10	Pav_start=10
Pav_stop=25	Pav_stop=25
gr_start=0.6	gr_start=0.6
gr_stop=0.5	gr_stop=0.5
gfm_start=0.5	gfm_start=0.5
gfm_stop=0.6	gfm_stop=0.6

FIGURE 1: Setup of the ADS Load Pull Simulation

Data Analysis and Formulation of Design Optimization Goals

After the load and source pull data were obtained, contours were plotted. The next step was to incorporate the design goal into the data analysis to formulate achievable and reasonable design optimization goals for the matching networks.

Circuit theory implies that it is impossible to obtain a matching network with a limited number of components that can match predefined impedances over a wide frequency bandwidth. For instance, a matching network that can match all optimal power impedances is unrealizable with a limited number of matching components. A compromise has to be made. This idea comes directly from the work by Bode and Fano^{1,2} on the physical limitation of the reflection coefficient of a matching network.

The approach is to identify a region on a Smith chart that is bounded by compromised performance. The existence of this region and its size provides a quantitative evaluation of the device's bandwidth. Although this method may not produce the best matching network, it provides a quantitative approach that can be used to obtain a reasonable design.

The work started with careful observation of load and source pull data. Next, a single contour at each frequency was drawn and the area of interest was obtained. A MATLAB program was written to perform the load and source pull data analysis. Figure 2 shows the gain contours obtained from the source pull data and corresponding to predefined gain values at frequencies from 2.0–2.7 GHz in increments of 100 MHz.

The shaded area shows the gamma region bounded by the lower gain limits. The contours, shown in different colors, represent constant gains over frequencies. The solid dots, also shown in different colors, represent maximum gain points. Table 1 lists the performance data that is obtained if the reflection coefficients of the input matching network are bounded in the shaded area.

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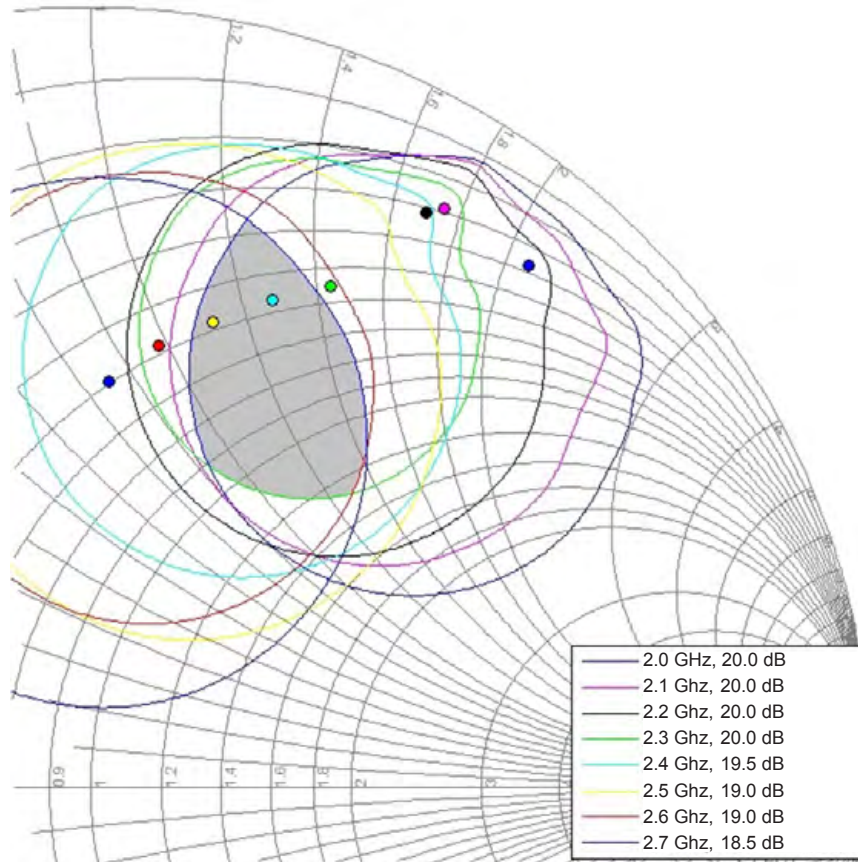


FIGURE 2: Source Pull Contours

TABLE 1: Performance Data Obtained If the Reflection Coefficients of the Input Matching Network Are Bounded in the Shaded Area Shown in Figure 2

FREQUENCY (GHz)	GAIN LOWER LIMIT (dB)	GAIN UPPER LIMIT (dB)
2.0	20.0	< 22.7
2.1	20.0	< 21.9
2.2	20.0	< 21.6
2.3	20.0	< 20.8
2.4	19.5	20.6
2.5	19.0	20.2
2.6	19.0	< 19.8
2.7	18.5	< 19.5

If the gain is tightened at high frequencies the shaded area will be smaller, making the design of the matching network more challenging. This observation reveals the bandwidth limitation of the device.

The same analysis was applied to the load pull data, represented in Figure 3. The P3dB power contours were analyzed.

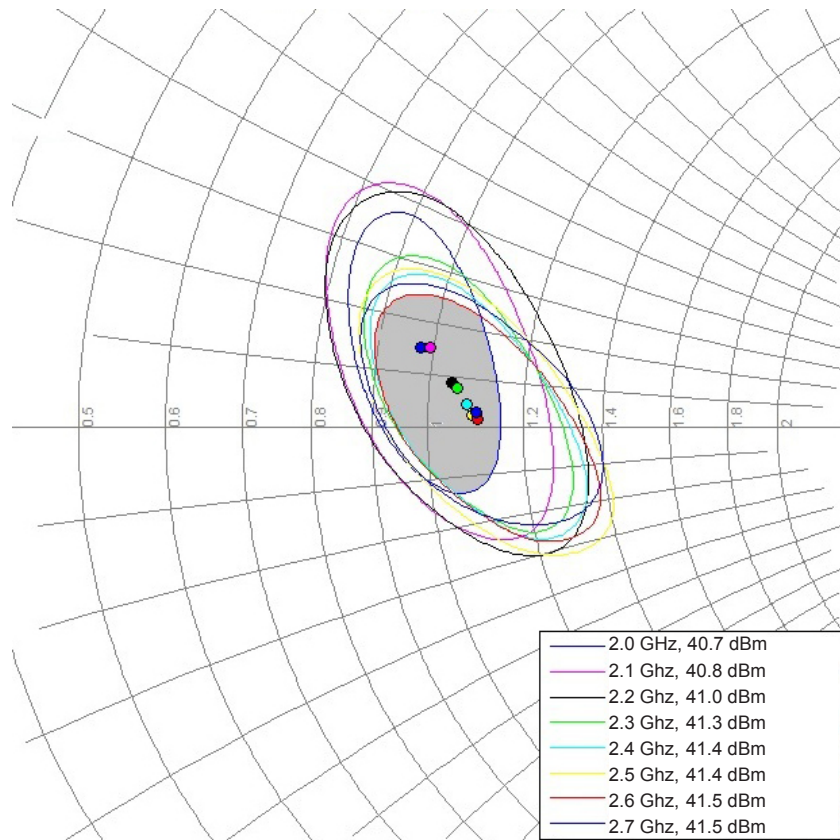


FIGURE 3: Load Pull Contours

The load pull contours are tightly packed, which, together with the internal structure of the device and previous observation on the input side, indicates that the device's bandwidth is limited by the input pre-match network.

The obtained shaded areas show the constraints to which circuit optimization can be done. The feasibility of optimization is a matter of study and is not presented in this report. Generally, the larger the constraint area, the easier it is to synthesize matching networks. One may want to use more complicated matching networks to synthesize over a much smaller area. However, this approach may create a counter-effect, because complicated networks tend to be lossier and have unwanted frequency responses.

Table 2 lists the P3dB power data that is obtained if the output matching network produces impedances that are bounded in the shaded area.

TABLE 2: Power Data Obtained If the Output Matching Network Produces Impedances That Are Bounded in the Shaded Area Shown in Figure 3

FREQUENCY (GHz)	P3dB LOWER LIMIT (dBm)	P3dB UPPER LIMIT (dBm)
2.0	40.7	40.8
2.1	40.8	41.1
2.2	41.0	41.4
2.3	41.3	41.5
2.4	41.4	41.6
2.5	41.4	41.7
2.6	41.5	41.7
2.7	41.5	41.7

Matching Networks Synthesis

After the matching criteria were established, the matching networks were designed. The design began with a schematic network. However, the final verification and optimization were performed in an electromagnetic (EM) simulation environment. ADS Momentum simulations give much better performance prediction than a schematic. Based on Modelithics' Application Note 48,³ the following recommendations were incorporated into the setup of the ADS Momentum simulation.

- If a port had a microstrip line attached, TML (Transducer Markup Language) calibration was used with the proper offset.
- If a port had a lumped component, such as a capacitor or inductor, attached, an internal port without port calibration was used. If component pads were included in the layout, the component was set to have no "pad stacks" in schematic co-simulation.
- At the device interface, an edge port without port calibration was used. The length of the edge was the same as the width of the device's paddles.
- Requirements such as mesh frequency, the use of "edge mesh," and so on followed ADS guidelines.

Distributed component designs were adapted for the matching networks. Figure 4 shows the layout of the matching networks for both input and output that were obtained after significant optimization.

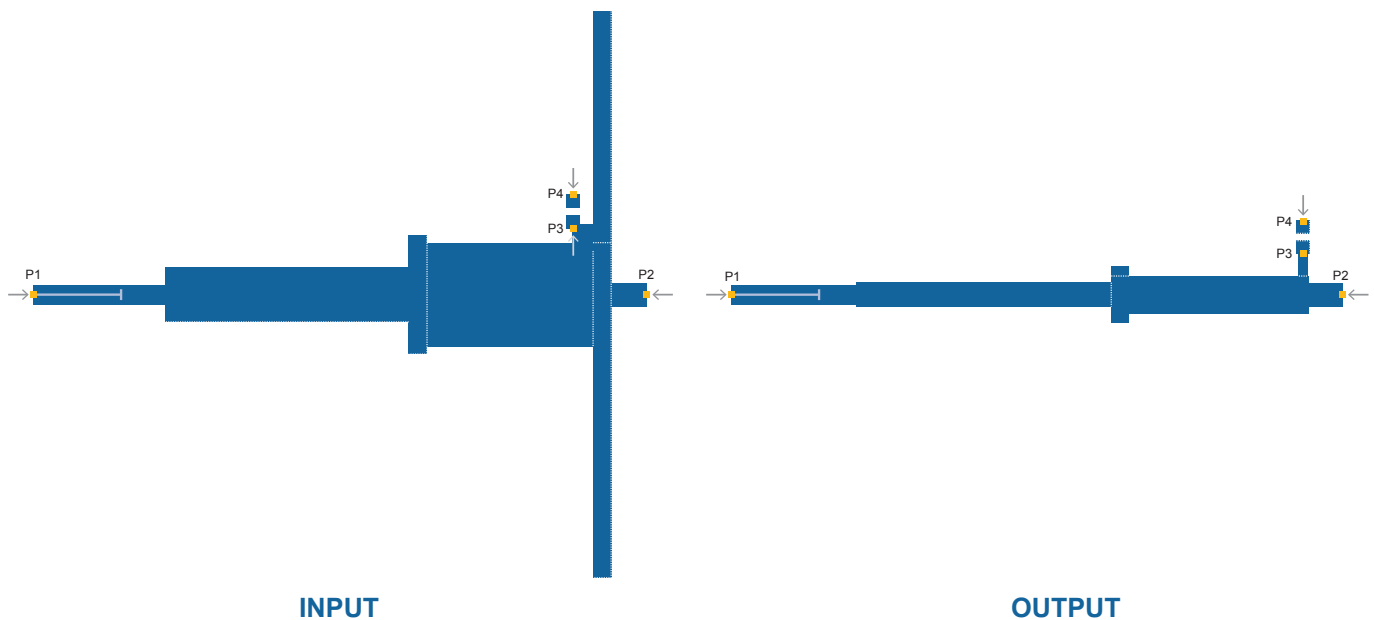


FIGURE 4: Layout of Input and Output Matching Networks

The evaluation board material used for the designs was Isola Group's IS680-345DK. The thickness of the board was 20 mils with 1 ounce of copper.

As shown in Figure 5 and Figure 6, the load pull plots were overlain with the EM simulation data to show how close the simulated gammas were when included in the shaded areas shown in Figure 2 and Figure 3.

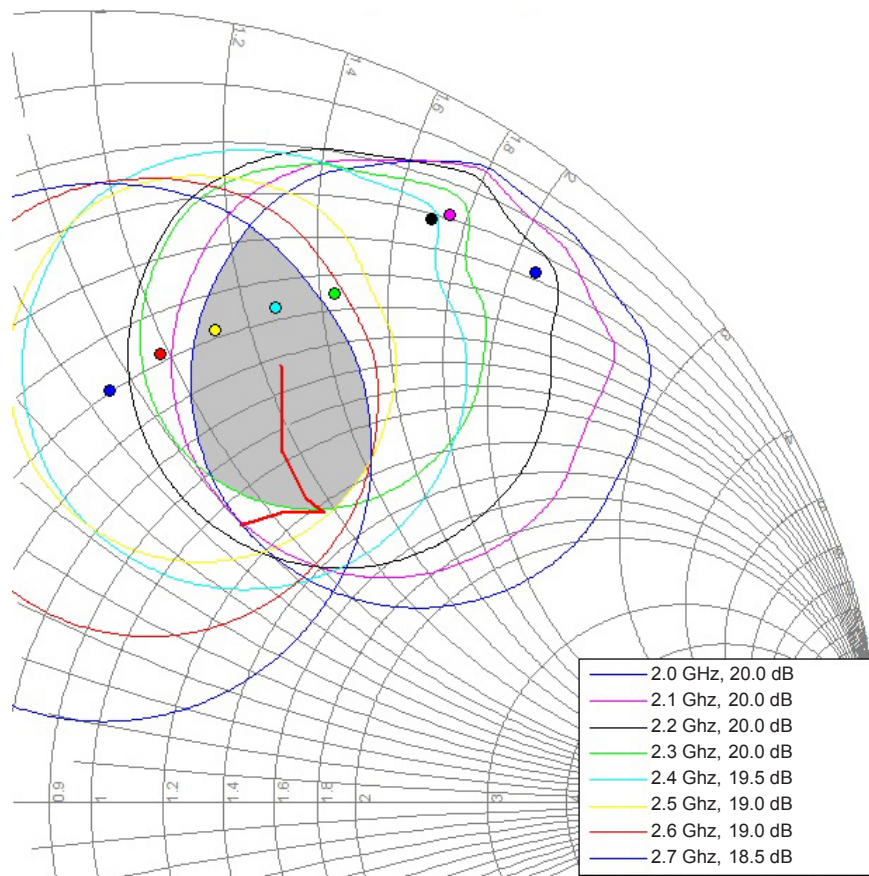


FIGURE 5: EM-Simulated Source Impedance Overlaying the Source Pull Plots

Despite having almost half of the simulated gammas outside the shaded area, this input matching network was used for better gain flatness.

The synthesis of the output matching network showed much better results, with most of the load gammas lying inside the shaded area of Figure 6.

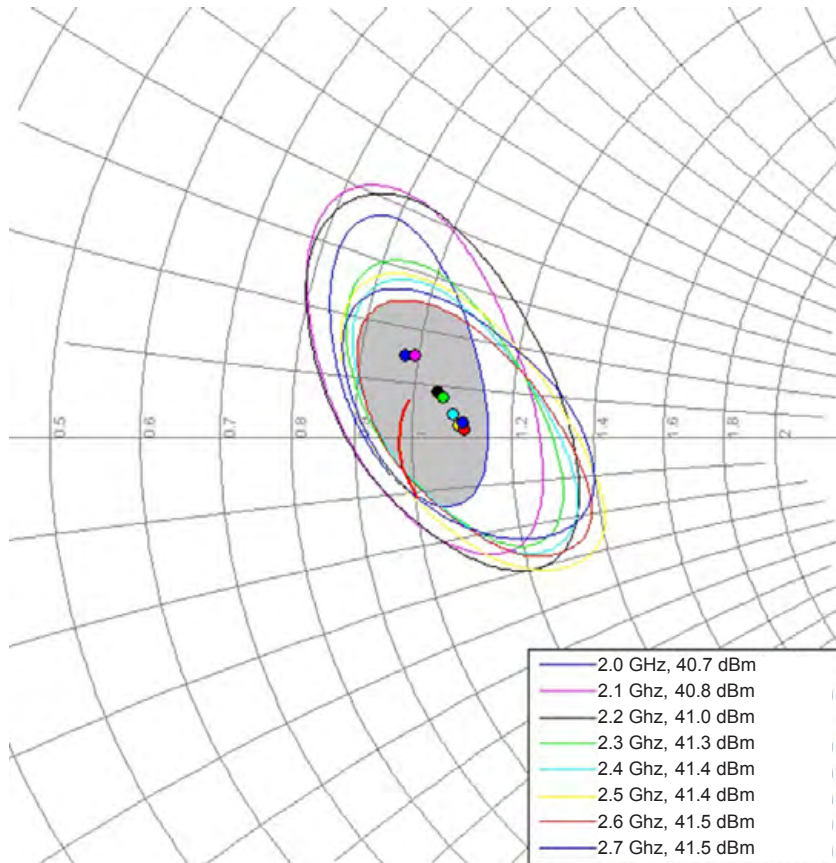


FIGURE 6: EM-Simulated Load Impedances Overlaying the Load Pull Contours

Measurement Results

The evaluation boards were built and tested at TriQuint’s facility in Richardson, Texas. Table 3 lists the obtained measurement data without any test bench tuning.

TABLE 3: Measurement Data for the Evaluation Boards

FREQUENCY (GHz)	P3dB (dBm)	G3dB (dB)	PAE3dB (%)
1.8	40.8	14.9	50.6
1.9	40.7	15.3	50.2
2.0	40.7	15.5	50.0
2.1	40.7	15.7	50.2
2.2	40.7	15.6	48.8
2.3	40.6	15.5	49.5
2.4	40.7	15.3	51.5
2.5	40.8	15.0	53.3
2.6	40.8	14.5	53.6
2.7	40.8	13.0	52.5
2.8	40.8	10.0	50.1

With the output loss of the matching network close to 0.5 dB, the output power directly from the device came close to the predicted load pull values shown in Figures 3 and 6. The gain was also close. Since Figure 5 showed a small signal gain and the loss of the input matching network was around 0.5 dB, the linear gain interpreted from Table 3 was about 19 dB. The power-added efficiency (PAE) was low because the load impedances were in the Smith chart region of optimal power where efficiency is typically low.

Although the design was originally intended for the 2.0–2.7 GHz bands, it worked at frequencies even as low as 1.8 GHz. However, at 1.8 GHz the input return loss was only about 3 dB.

Comparison of Measured and Simulated Data Results

For effective comparison purposes, the entire amplifier, including the EM models of the input and output matching network, was simulated. Table 4 shows a side-by-side comparison of the measured and simulated data.

TABLE 4: A Side-By-Side Comparison of the Measured and Simulated Data of the Amplifier

Frequency (GHz)	P3dB (dBm)		G3dB (dB)		PAE3dB (%)		RL @ 35dBm Output Power (dB)	
	MEASURED	SIMULATED	MEASURED	SIMULATED	MEASURED	SIMULATED	MEASURED	SIMULATED
1.8	40.8	41.0	14.9	15.6	50.6	57.7	-3.2	-2.5
1.9	40.7	41.0	15.3	16.2	50.2	57.8	-4.5	-3.4
2.0	40.7	40.9	15.5	16.6	50.0	57.6	-6.5	-4.7
2.1	40.7	41.0	15.7	17.0	50.2	57.5	-9.6	-6.1
2.2	40.7	40.9	15.6	16.7	48.8	57.7	-10.2	-7.1
2.3	40.6	41.0	15.5	16.7	49.5	59.1	-8.9	-7.5
2.4	40.7	41.0	15.3	16.6	51.5	60.2	-10.9	-8.0
2.5	40.8	41.0	15.0	16.5	53.3	61.2	-14.2	-9.4
2.6	40.8	41.0	14.5	16.5	53.6	62.1	-11.3	-13.5
2.7	40.8	41.0	13.0	16.1	52.5	62.7	-7.4	-17.6
2.8	40.8	41.0	10.0	14.6	50.1	62.6	-3.7	-6.4

Based on the comparison, the following was observed:

- P3dB tracked well between the measured and simulated results. While the simulated results inflated power by a small amount, they correctly predicted the wideband behavior of the output matching network and power flatness, which is really impressive.
- Observation on PAE3dB seemed to point to a small shift in power-tuned load impedances between the model and real device. There might be some inflation on the part of the model when predicting efficiency. Many other factors, such as harmonic terminations, were not accurately modeled in simulation but played an important role in the real measurement.
- While the model over-predicted the gain, there were many factors that were not correctly modeled in the simulation setup, such as the narrowband behavior of the test bench. Even so, the model correctly predicted the behavior of G3dB, especially the drop off at the high end of the band.
- The low return loss (RL) and high gain predicted by the model indicated that the model's source impedance may be shifted toward a higher gain direction and lower RL.

Summary

While there were discrepancies in gain and PAE between the simulated and measured data, the model was effective in producing a viable design and product. It is also important to note that the amplifier module performed even without any bench tuning. Had actual load pull measurements been done, the measured performance would likely have been the same. This outcome demonstrates that the model is an extremely useful tool, giving designers an advantage when a quick turnaround prototype is required and there is no available capital or time to produce actual load pull data.

References

- ¹ Fano, R. M., "Theoretical Limitations on the Broadband Matching of Arbitrary Impedances," *Journal of the Franklin Institute*, Vol. 249, Nos. 1, 2, pgs. 57–38 and 139–154, 1950.
- ² Bode, H. W., *Network Analysis and Feedback Amplifier Design*, New York: Van Nostrand, 1945.
- ³ Modelithics, "Recommendations for Port Setup When Using ADS Momentum and Modelithics Models," Tampa Bay, 2014.