



ACT85411

Power Loss Protection with Power Management

ACT85411 Datasheet Brief

Please refer to the [ACT85411 Product Page](#) for more information. Click [here](#) for a link to request the full datasheet.

BENEFITS and FEATURES

• HIGH-PERFORMANCE POWER LOSS PROTECTION

- Wide Operating Input Range 2.7V to 14.4V.
- Withstanding 20V Max Input Voltage.
- Inrush Current Control to Soft-Start VBUS Output.
- Hot-plug Compatible.
- Programmable 10A Input Current Limit for eFuse.
- Adjustable Start-Up Slew Rate.
- Highly Configurable Power-Fail Detection.
- Power Loss Indicator “PLI” Signal.
- Discharge Input Option to Allow Discharge and Reset the PLP Function.
- Programmable up to 2.25MHz Buck Operating Frequency for Small Inductor Size.
- 8A Synchronous Buck With 100% Duty Cycle Operation During Supplement Mode.
- Programmable 5.5V to 31V Boost Storage Voltage.
- Seamless Transition from Input Supply to Storage Capacitor Backup Power.
- Compatible with Many Types of Storage Caps: Super Caps, Electrolytic, Tantalum, POSCAP etc.
- Autonomous Health Monitoring Function.
- Early Storage Capacitor Failure Detection.
- Storage Capacitance Measurement (Capacity).
- PG_STR - Storage Okay Status Indicator.
- eFuse, Boost, and Buck UV/OV/OC Protection.

• HIGH EFFICIENCY, FULLY SYNCHRONOUS BUCK REGULATORS

- 2 High Voltage DC-DC Buck Converters.
- Integrated Synchronous Power Stage.
- High Efficiency Up to 96%.
- Optimized Single Stage Conversion from $V_{in} = 12V$.
- Wide Configurable Output Range, 0.6V – 5.26V.
- Excellent Dynamic Response.
- Proprietary COT Control Algorithm.
- Small Inductor Sizes.
- 500 kHz – 2.0MHz Configurable Fsw Range.
- Near Constant Switching Frequency Operation.
- Output Currents Up to 12A.
- Sensorless Over Current Protection (OCP).
- Output UV and OV Detection.
- Optimized for Ceramic Output Capacitors.

• HIGH EFFICIENCY, FULLY SYNCHRONOUS BUCK-BOOST REGULATOR

- 1 High Voltage DC-DC Buck-Boost Converter.

- Integrated Synchronous Power Stage with Full H-Bridge Control.
- High Efficiency Up to 96%.
- Wide Configurable Output Range, 9.6V – 15.95V.
- Up to 1A DC Output Current with 12V Output, 12V Input Voltage and 600mA Output with 3.3V Input Voltage.
- Sensorless Over Current Protection (OCP).
- Output UV and OV Detection.
- Optimized for Ceramic Output Capacitors.
- 1125 or 562 kHz Configurable Switching Frequency.

• LDO

- Programmable Output Voltage.
- Configurable Input Power Source – VCC/VAUX.
- Automatic Switch Over to VCC Power when VAUX is not available.
- 200mA Output Current Capability.

• SYSTEM CONTROL AND INTERFACE

- Dedicated Power Loss Indicator (PLI) Pin.
- Dedicated EN/DISCHG Input to Control PLP.
- 6 Programmable General Purpose I/Os.
- I²C Serial Interface with Password Protection.
- ADC Monitoring of Critical Signals.
- Independent On & Off Sequencing Control.
- Reset/Power Good Output.
- Configurable Rails On/Off through I²C/GPIO.
- Input Current (Power), UV, and OV Monitoring.
- Configurable Interrupt Function to Inform Host of Faults/Status Change.
- Thermal Alert and Protection.
- GPIO Control to Power External NTC for ADC Reading of External Temperature.
- External Current Sensing with ADC Read- out.

• OTHER SYSTEM FUNCTIONS

- Versatile GPIO Functions.
- I²C Watchdog Supervision.
- Interrupt Function.
- I²C Safety Bits to Enhance Immunity against Spurious I²C Transactions.
- Thermally Enhanced 6mm X 6mm FCQFN Package.

APPLICATIONS

- Solid State Drives
- Industrial Applications
- Backup Power
- Hot Plug / Hot Swap Devices

TYPICAL APPLICATION DIAGRAM

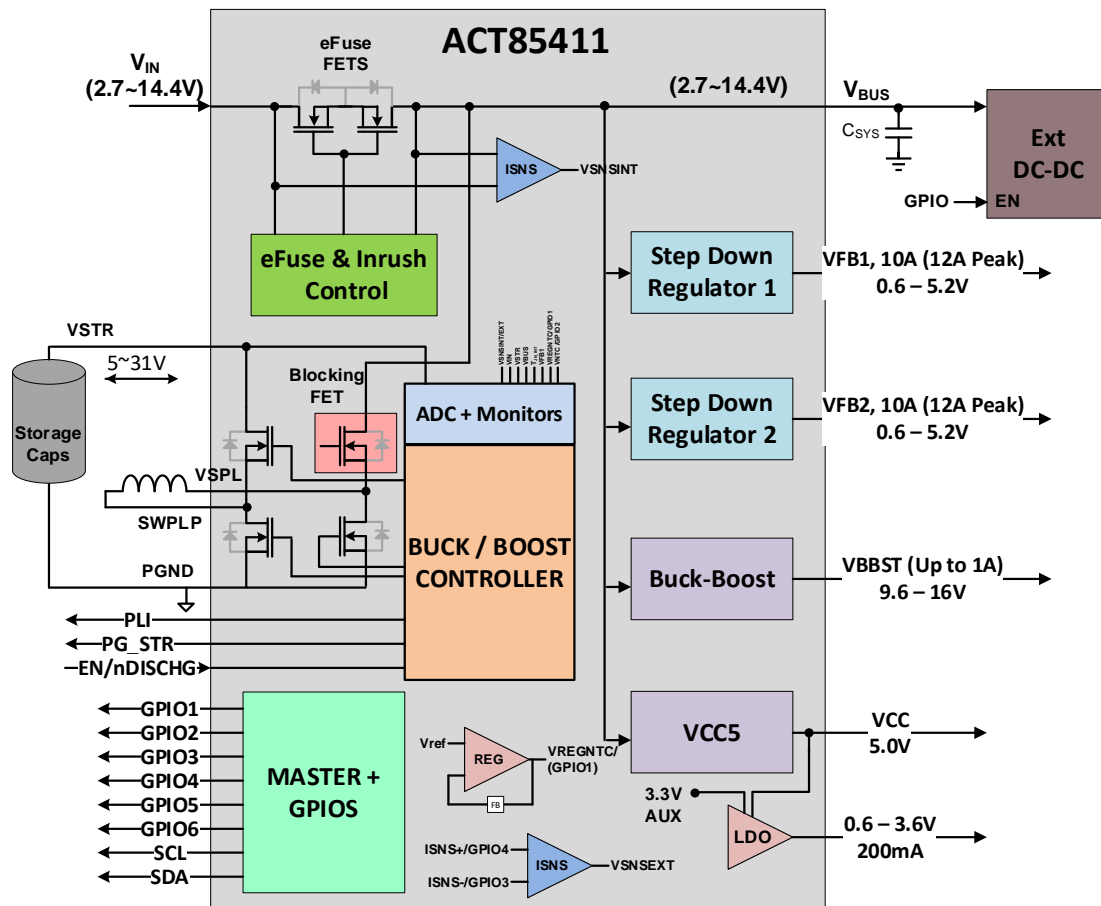


Figure 1: ACT85411 Block Diagram

FUNCTIONAL BLOCK DIAGRAM

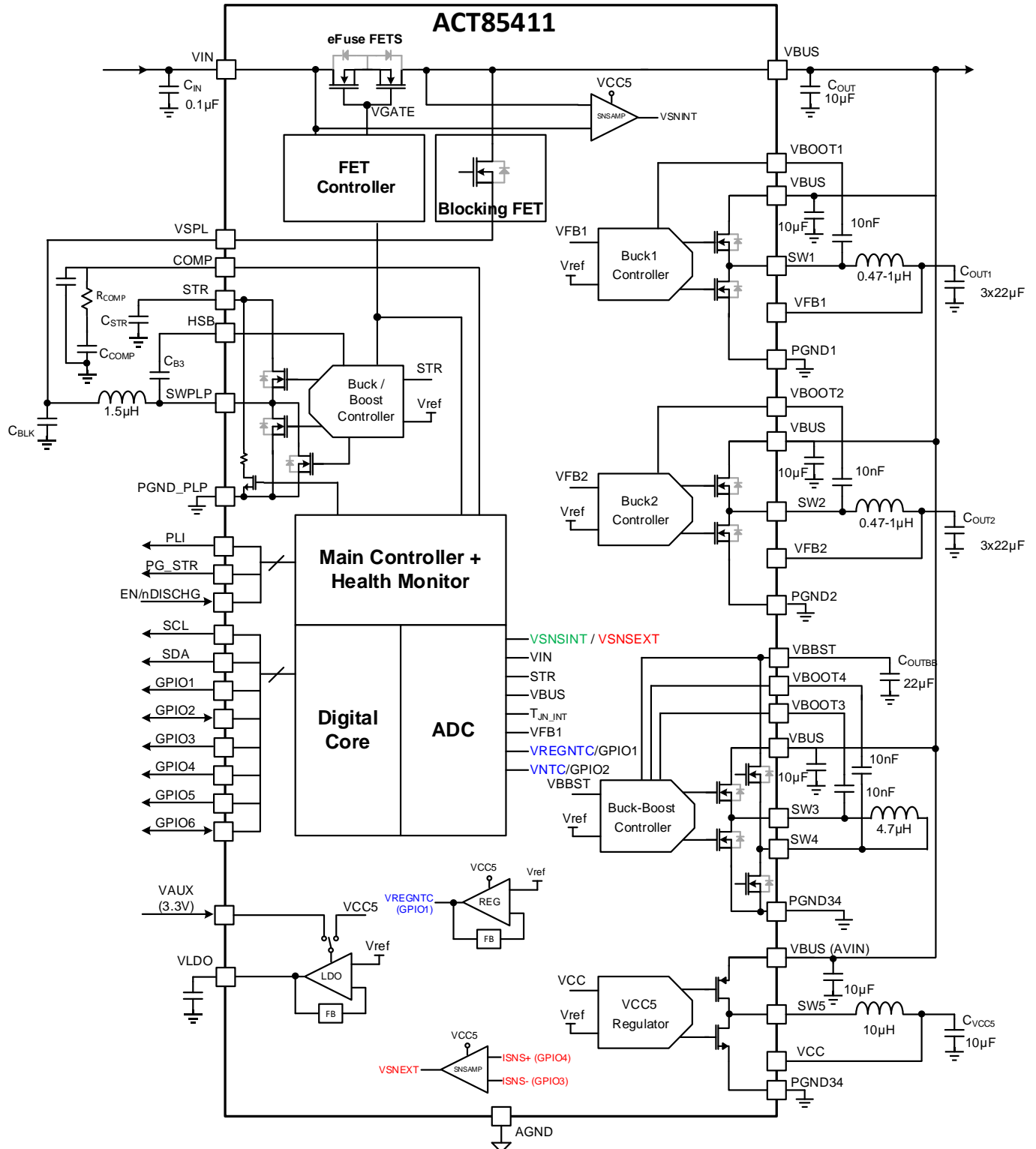


Figure 2: ACT85411 Functional Block Diagram

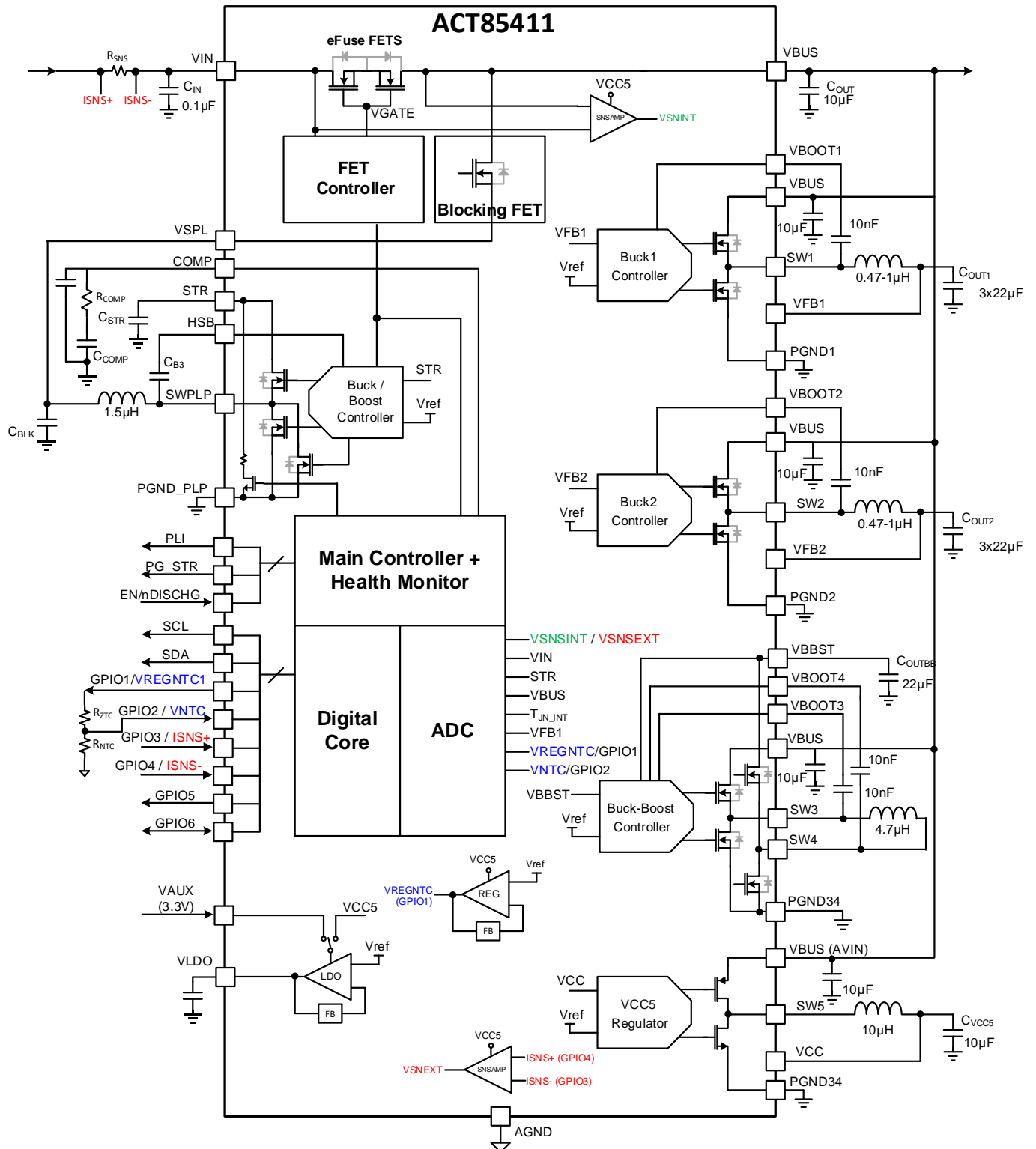
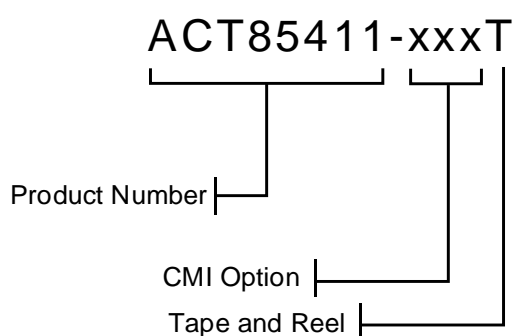


Figure 2b: ACT85411 Functional Block Diagram with Alternate GPIO Function (Optional Functions)

ORDERING INFORMATION

PART NUMBER	V _{IN}	V _{STR}	V _{OUT1}	V _{OUT2}	V _{BBST}	V _{LDO}	V _{SUPPL}	V _{HL-THCHK}	V _{IN_UV1}	V _{IN_UV2}	T _{DETUV1}	T _{DETUV2}
ACT85411-101T	12.0V	31.0V	3.3V	2.8V	12.0V	3.3V	6.0V	+1.0V	0.8	0.78	15μs	4μs
ACT85411-102T	12.0V	31.0V	3.3V	2.8V	12.0V	3.3V	6.0V	+1.0V	0.8	0.8	0μs	24μs
ACT85411-103T	12.0V	31.0V	3.3V	2.8V	12.0V	3.3V	6.0V	+1.0V	0.8	0.8	0μs	24μs



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: "xxx" represents the CMI (Code Matrix Index) version. The CMI identifies the IC's default register settings and configuration.

Note 3: "T" represents the tape and reel option.

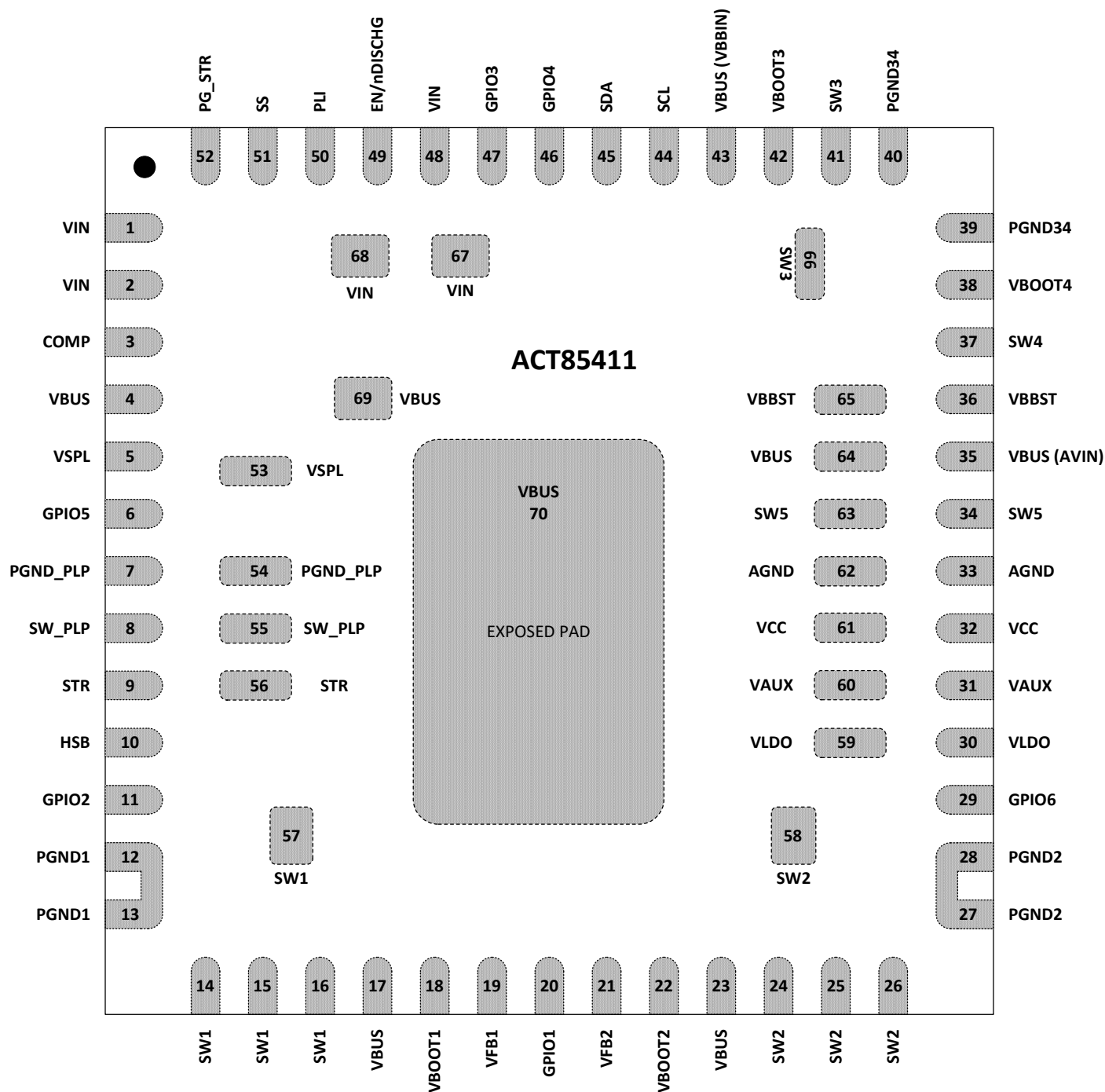


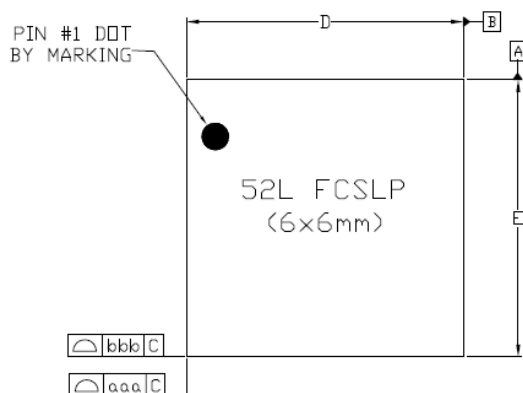
Figure 3: Pin Configuration – Top View (pins facing down). 6mmx6mm - 52 QFN

PIN DESCRIPTIONS

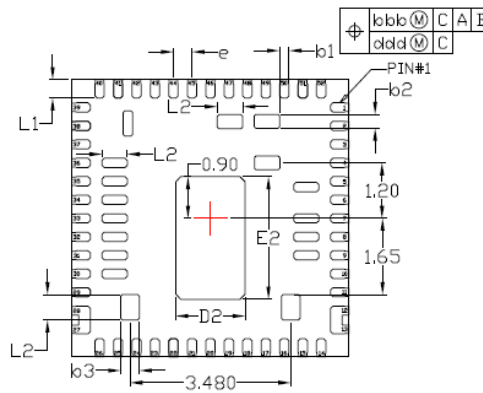
PIN	NAME	DESCRIPTION
1, 2, 48, 66, 67, 68	VIN	Power Supply Input to the eFuse. Connect a 0.1μF capacitor between VIN and PGND close to the IC.
3	COMP	Compensation input pin for the PLP Buck converter (active in supplement mode).
4, 17, 23, 35, 43, 64, 69, 70	VBUS	Output for bypass mode, in-rush, and eFuse functionality. VBUS is also the input voltage bus for the downstream regulators.
5	VSPL	Supplement buck circuit output pin (Boost input pin). It is isolated from VBUS by the internal blocking FET.
6	GPIO5	GPIO5 Pin
7, 54	PGND_PLP	PLP Power Ground. Connect to large ground plane on PCB.
8, 55	SW_PLP	Power loss protection Buck/Boost switching node. Place an inductor between VSPL & SW_PLP.
9, 56	STR	Storage capacitor input/output. Connect the storage capacitors to STR. (Minimum 100μF).
10	HSB	High side bootstrap pin. Connect a 47nF capacitor between HSB & SW_PLP pins.
11	GPIO2	GPIO2 Pin
12, 13	PGND1	Buck1 power ground pin. Connect to large ground plane on PCB
14, 15, 16, 57	SW1	Switch pin for HV Buck1 regulator
18	VBOOT1	Bootstrap voltage for Buck1 regulator. Connect a 0.1μF capacitor between VBOOT1 and SW1 pins.
19	VFB1	Output and feedback pin for Buck1 regulator.
20	GPIO1	GPIO1 Pin
21	VFB2	Output and feedback pin for Buck2 regulator.
22	VBOOT2	Bootstrap voltage for Buck2 regulator. Connect a 0.1μF capacitor between VBOOT2 and SW2 pins.
24, 25, 26 58	SW2	Switch pin for HV Buck2 regulator.
27, 28	PGND2	Buck2 power ground pin. Connect to large ground plane on PCB
29	GPIO6	GPIO6 Pin
30, 59	VLDO	LDO output pin. Place 2.2uF or larger ceramic between this pin and AGND.
31, 60	VAUX	VAUX Input pin. This is used as input voltage to the LDO.
32, 61	VCC	Output and feedback pin for VCC Buck regulator. Connect a 10μF capacitor between VCC and AGND.
33, 62	AGND	Analog GND Pin. Connect to clean ground on the PCB.
34, 63	SW5	Switch pin for VCC Mini-Buck regulator. Connect an inductor between SW5 and VCC pins.
36, 65	VBBST	Output and feedback pin for Buck-Boost regulator. Connect a 10μF capacitor between VBBST and PGND
37	SW4	Second Switch pin for Buck-Boost regulator. Connect an inductor between SW4 and SW3 pins.
38	VBOOT4	Second Bootstrap pin for Buck-Boost regulator. Connect a 0.1μF capacitor between VBOOT4 and SW4.
39, 40	PGND34	Power Ground connection for the Buck-Boost regulator and the mini-buck regulator.
41	SW3	Switch pin for Buck-Boost regulator. Connect an inductor between SW3 and SW4 pins.
42	VBOOT3	Bootstrap pin for Buck-Boost regulator. Connect a 0.1μF capacitor between VBOOT3 and SW3.
44	SCL	I ² C clock input. Needs an external pull up resistor.
45	SDA	I ² C data input /output pin. Needs an external pull up resistor.
46	GPIO4	GPIO4 Pin
47	GPIO3	GPIO3 Pin
49	EN / nDISCHG	Enable pin for the eFuse and PLP circuit. When EN = 0, the eFuse blocks output from the input and the supplement mode is turned on. The PLI output goes low when EN = 0 to indicate supplement mode.
50	PLI	Power Loss Indicator, Open-Drain Output for VIN. PLI goes high when the eFuse is turned on and goes low when the IC enters supplement mode. PLI is referenced to AGND.
51	SS	Soft Start Input. Place a capacitor from SS to VSS to control the eFuse startup voltage slew rate.
52	PG_STR	Storage Okay Output Pin. The output of the health monitoring circuit indicates the health monitoring status and if the STR output voltage is okay (higher than the STR_OK threshold).
Exposed Pad	VBUS	Tie to top layer VBUS plane. All VBUS pins should be directly connected to the exposed pad on the top layer.

PACKAGE DETAILS

QFN-52 PACKAGE OUTLINE AND DIMENSIONS

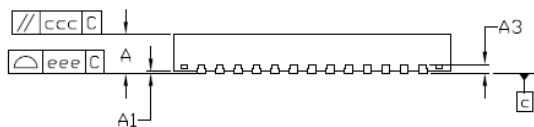


TOP VIEW



BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	5.950	6.000	6.050
E	5.950	6.000	6.050
D2	1.450	1.500	1.550
E2	2.600	2.650	2.700
b1	0.150	0.200	0.250
b2	0.250	0.300	0.350
b3	0.350	0.400	0.450
e	0.400 BSC		
L1	0.350	0.400	0.450
L2	0.500	0.550	0.600
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		



SIDE VIEW

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- SVHC Free
- PFOS Free
- Antimony Free
- TBBP-A (C15H12Br4O2) Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

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For technical questions and application information:

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