ACT72350EVK1

Power Application Controllers

www.qorvo.com

CONTENTS

OVERVIEW

The ACT72350 is an integrated tri phase BLDC/PMSM motor driver optimized for driving medium voltage tri phase BLDC/PMSM motors. Based on the PAC5x32 family of devices, the ACT72350 contains all of the blocks found within the aforementioned device, minus the microcontroller core. The ACT72350 is fully equipped with Qorvo's proprietary highly configurable Power manager, Qorvo's patent-pending Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control solution available.

The Configurable Power Manager (CPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable high-voltage switching supply controller capable of operating a buck converter, a configurable medium-voltage switching regulator, and three linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are 180V power drivers designed for half bridge, H-bridge, 3-phase, and general-purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.

The ACT72350 is interfaced through the tri phase inverter PWM control input signals. An SPI port grants access to register configuration. All analog resources are made available for easy access with the externally provided microcontroller core.

Qorvo's ACT72350EVK1 evaluation kit consists of the following:

- ACT72350EVK1 Body module
- ACT72350EVK1 User's Guide
- External MCU Board Module (Optional)
- Schematics, BOM and Layout Drawings

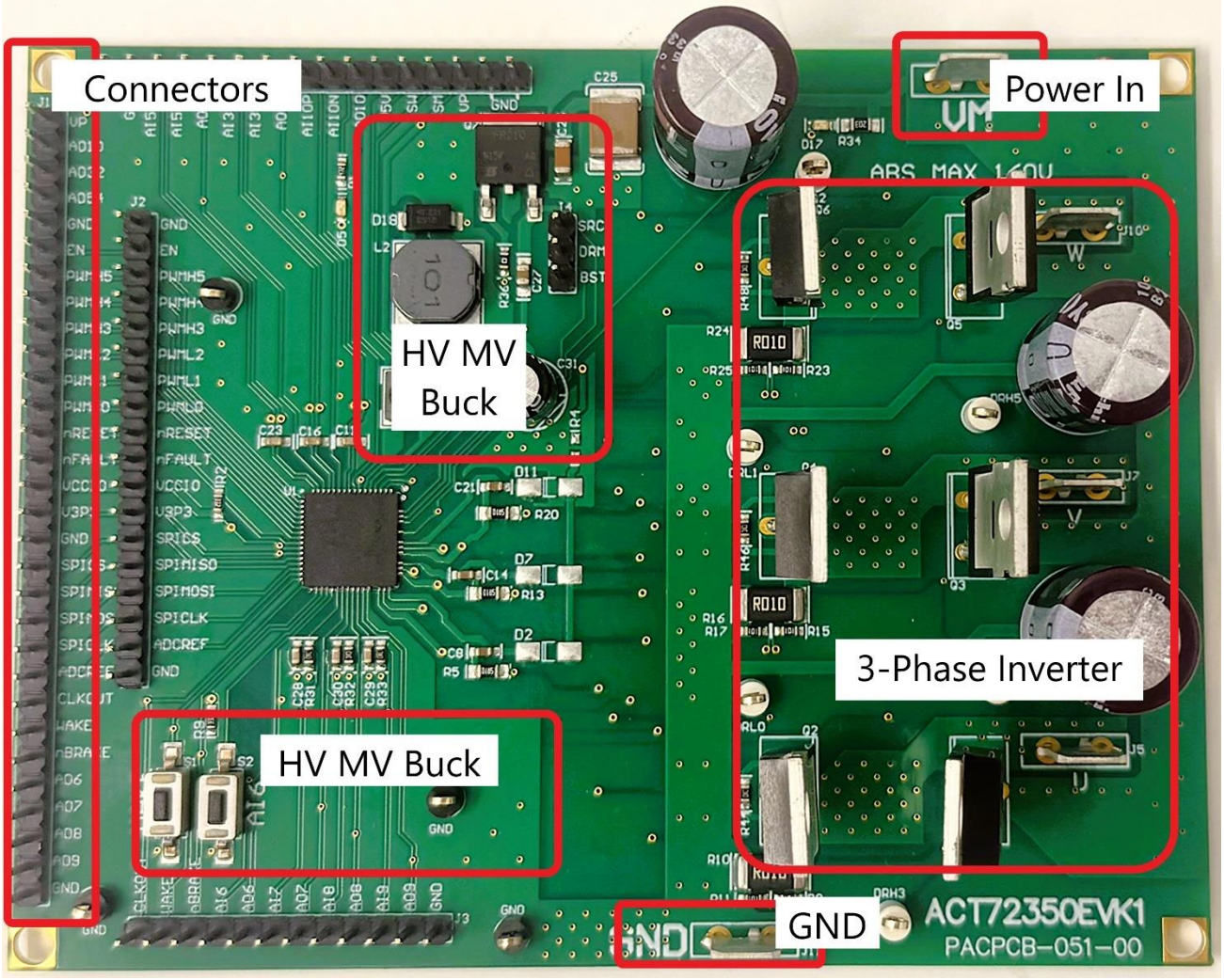

Figure 1. ACT72350EVK1 Block Diagram

Solution Benefits:

- The ACT72350 is ideal for battery powered applications between 48V and 120V.
- 10 Analog Front-End IO pins, 3 Differential Programmable Gain Amplifiers.
- 3 160V (180V Bootstrap) high-side gate drivers with 2A gate driving capability.
- Schematics, BOM, Layout drawings available

The following sections outline the hardware features of Qorvo's ACT72350EVK1 turnkey solution.

ACT72350EVK1 RESOURCES

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the ACT72350EVK1 evaluation module, as seen from above:

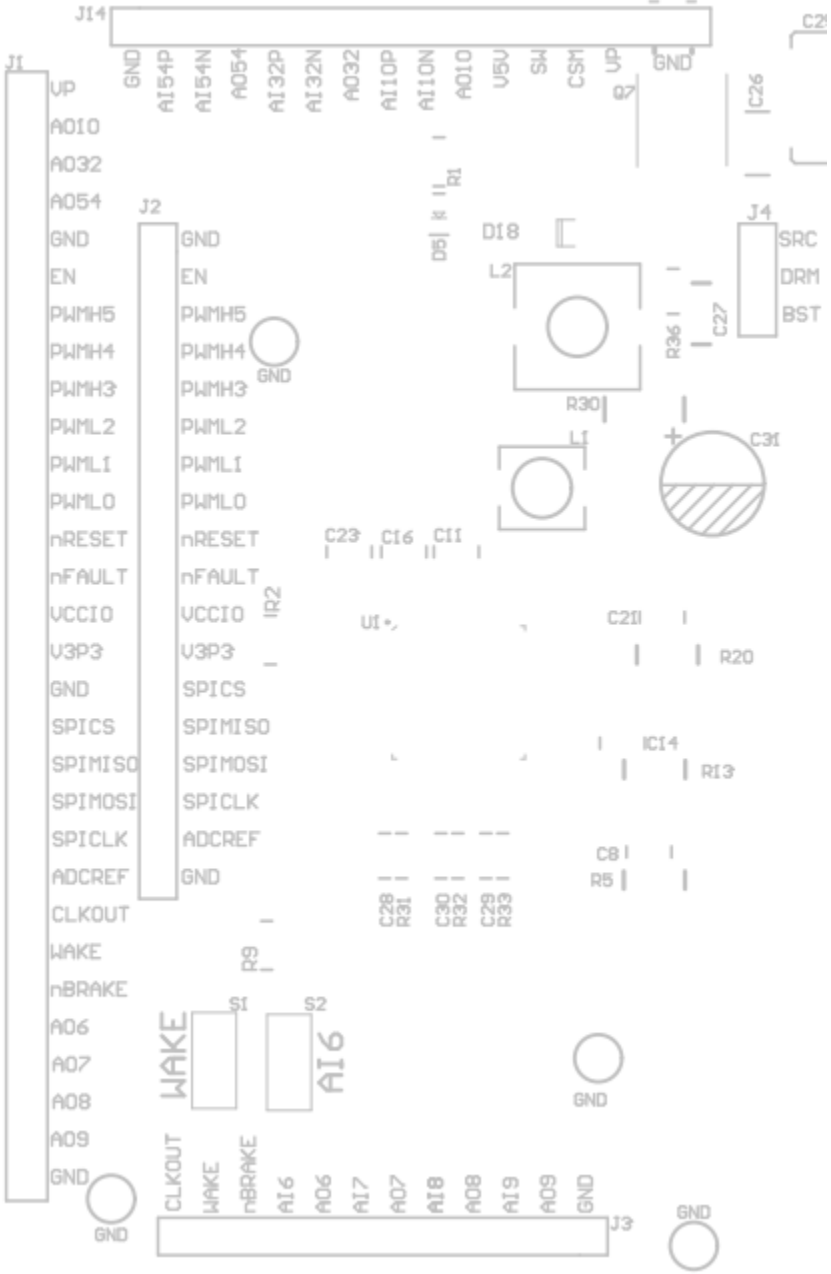

Figure 2. ACT72350EVK1 Headers and Test Stakes Pinout

Power Input

Power to the ACT72350EVK1 evaluation module can be applied to the VM and GND spade connectors. Power to the ACT72350EVK1 evaluation module should not exceed 160V (Abs Max).

The ACT72350EVK1 is optimized to operate with voltages ranging from Input voltage 25V – 160V nominal (160V Abs Max). When the VIN input voltage goes above 25V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D5 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.8V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D5	VSYS (5V). Light up when the ACT72350 device is successfully powered up by VM.
D17	VM. Lights up as VM voltage is applied.

External interface

J1 Pin	Terminal	Description
1	VP	VCCIO (default is 5V)
2	AO10	SWD Serial Data
3	AO32	SWD Serial Clock
4	AO54	GND (System Ground)
6	GND	GND (System Ground)
7	EN	Tri Phase Inverter Enable
8	PWMH5	High Side Gate Driver 5 (Half H Bridge 52) PWM Input
9	PWMH4	High Side Gate Driver 4 (Half H Bridge 41) PWM Input
10	PWMH3	High Side Gate Driver 3 (Half H Bridge 30) PWM Input
11	PWML2	Low Side Gate Driver 2 (Half H Bridge 52) PWM Input
12	PWML1	Low Side Gate Driver 1 (Half H Bridge 41) PWM Input
13	PWML0	Low Side Gate Driver 0 (Half H Bridge 30) PWM Input
14	nFAULT	Open Drain fault output
15	VCCIO	Internally generated digital I/O 3.3V
16	V3P3	Internally generated 3.3V power supply.
17	GND	GND (System Ground)
18	SPI_CS	SPI Communications Port Chip Select
19	SPI_MISO	SPI Communications Port Master Input Slave Output
20	SPI_MOSI	SPI Communications Port Master Output Slave Input
21	SPI_CLK	SPI Communications Port Clock
22	ADCREF	2.5V or 3.0V ADC reference output
23	CLKOUT	Open Drain 32KHz CLK Output
24	WAKEUP	Enter Hibernate mode input (asserted low)
25	nBRAKE	Enter Brake mode (asserted low)
26	AO6	Analog 6 Output
27	AO7	Analog 7 Output
28	AO8	Analog 8 Output
29	AO9	Analog 9 Output
30	GND	GND (System Ground)

Schematic diagrams

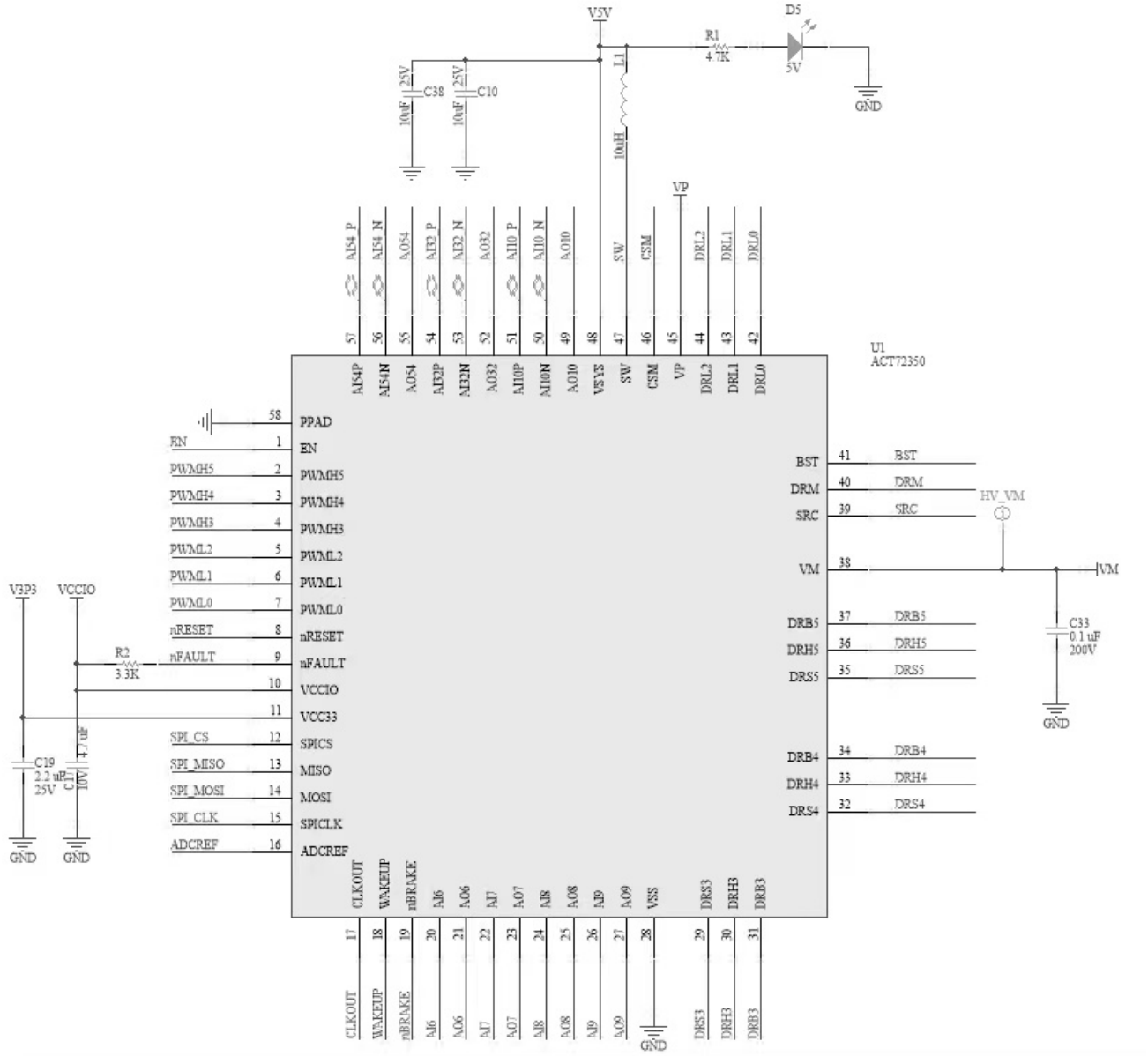

Figure 3. ACT72350EVK1 schematic

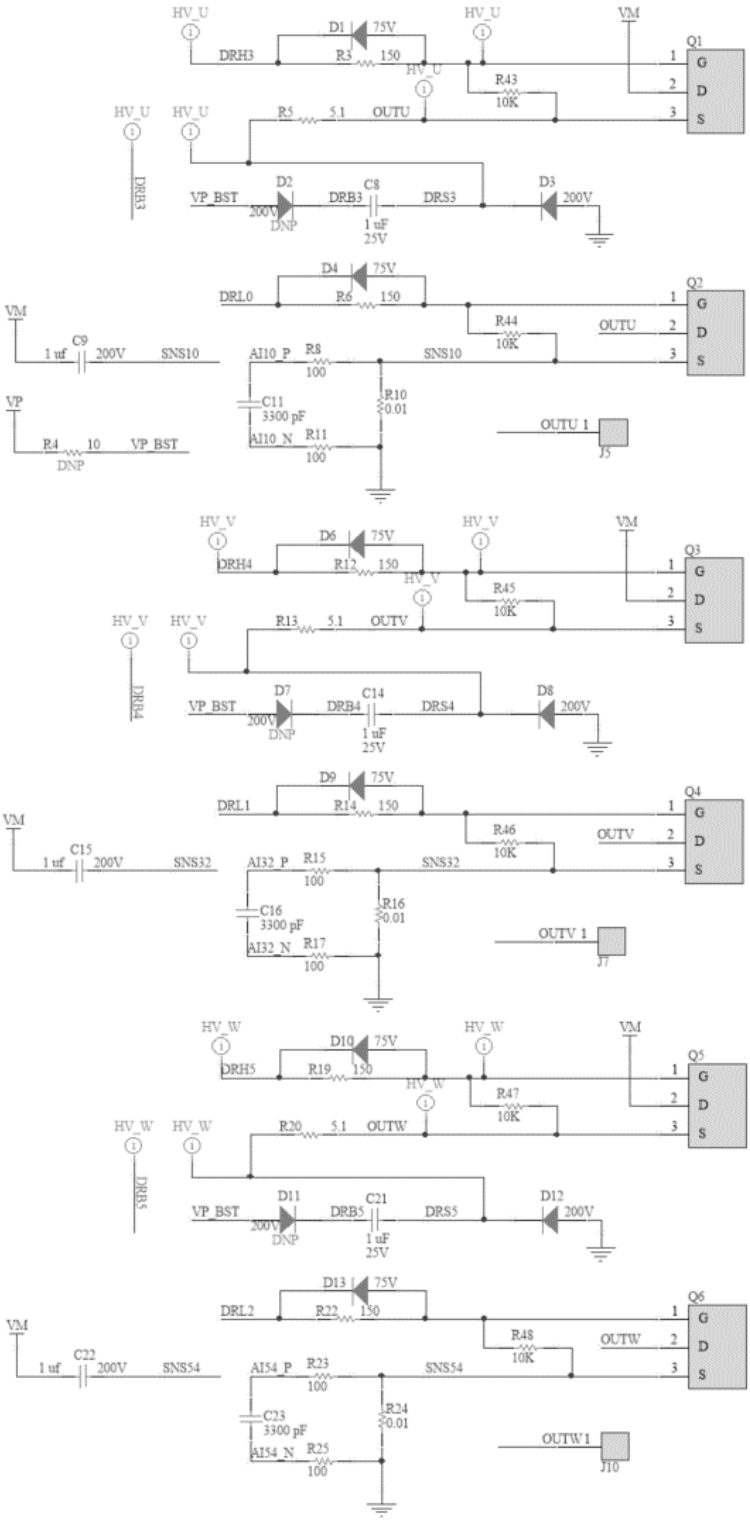

Figure 4. ACT72350EVK1 Schematic - Power Stage

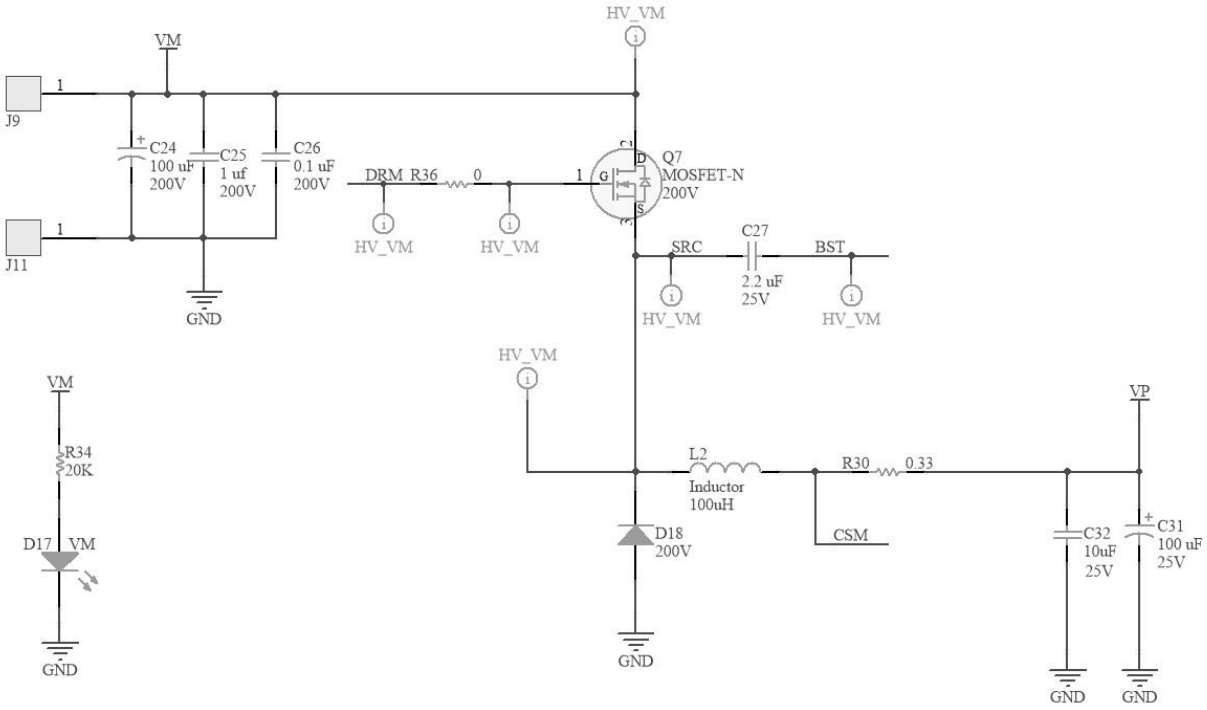

Figure 5. ACT72350EVK1 schematic - Auxiliary Power Supply

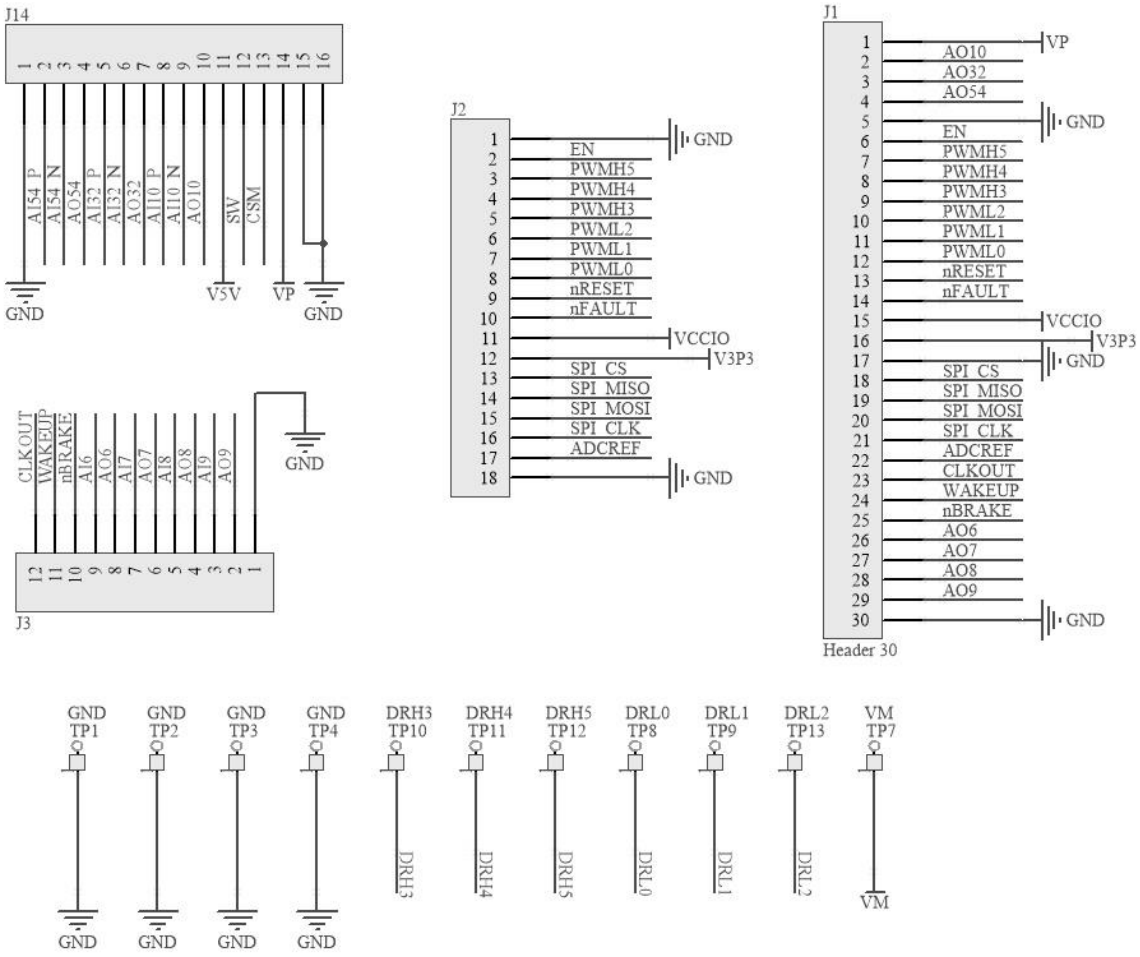

Figure 6. ACT72350EVK1 schematic – Interfaces and Test point

ACT72350 is a combination of analog front-end and motor driver, requiring an external MCU for motor control. To enable motor operation, user can choose one of the following options:

1) External MCU (provided by the User):
    a. User supplies their own MCU to generate PWM signals and communicate with the ACT72350 via SPI
2) RD5524_ACT3250 Development Board as MCU (Optional)
    a. PAC5524 Dev Board serves as the MCU, utilizing its PWM pins to drive the motor.

PAC5524 DEVELOPMENT BOARD AS MCU (OPTIONAL)

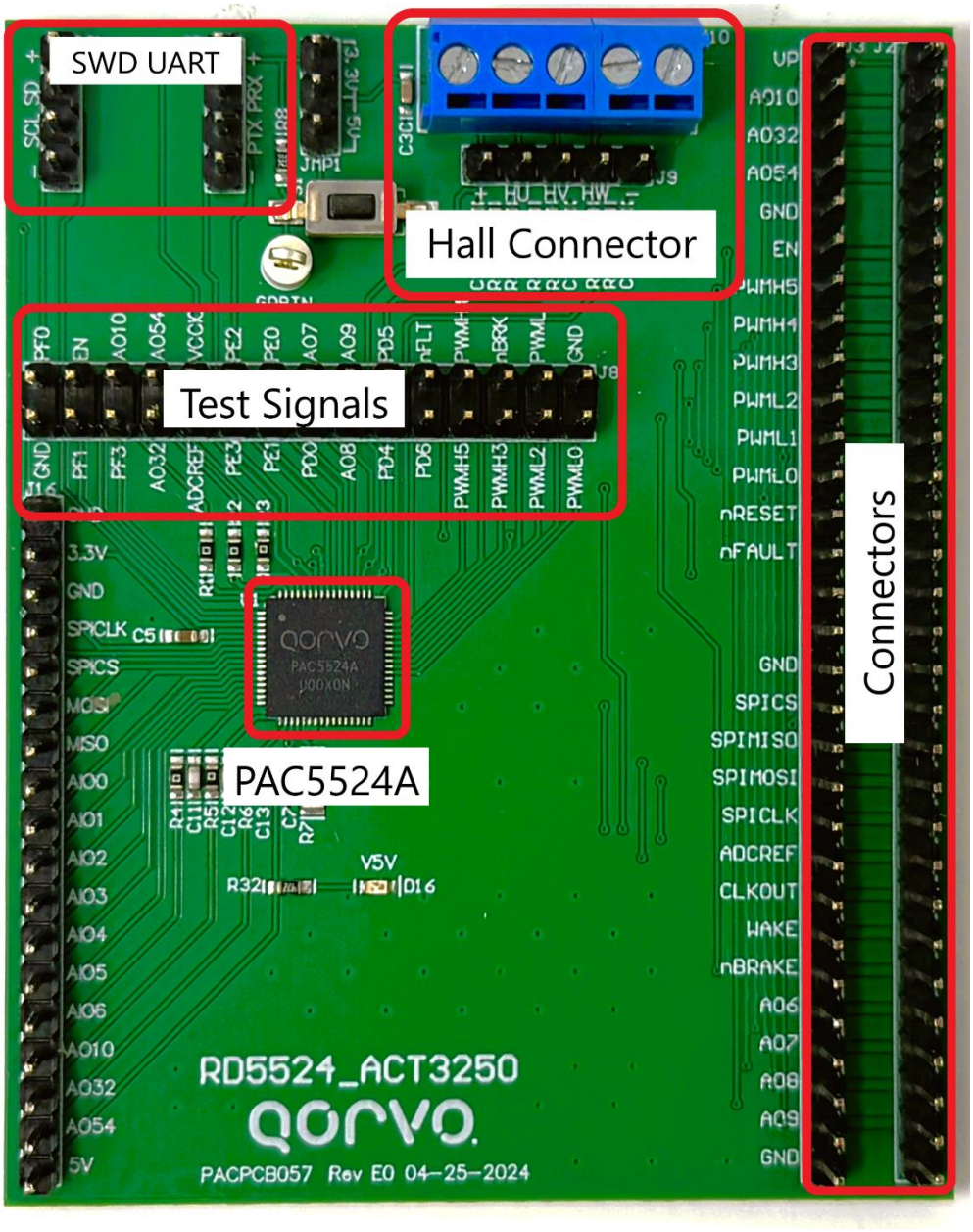

Figure 7. External MCU Board Block Diagram

SWD Debugging

Connector J1 offers access to the PAC5524 SWD port lines.

J1 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND (System Ground)

Serial Communications

Connector J7 offers access to the PAC5524 UART port lines.

J7 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	TX	MCU Transmit Line
3	RX	MCU Receive Line
4	-	GND (System Ground)

Hall Sensor Interface

Connector J10 offers access to the PAC5524 resources on PORTD utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for in real time debugging.

J10 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	Hall Sensor U	PORTD4 (PWMB0 function)
3	Hall Sensor V	PORTD5 (PWMB1 function)
4	Hall Sensor W	PORTD6 (PWMD0 function)
5	GND	GND (System Ground)

ACT72350EVK1 SETUP

The setup for the ACT72350EVK1 evaluation module requires up to five simple connections.

1. Connect the power source via spade tab connectors VM and GND. As VIN power is applied, the LED D17 will light up. Once VIN voltage goes above 25V, the ACT72350's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D5 lighting up.
2. Connect the 3 Phase BLDC/PMSM motor via space tab connectors PHASE U, PHASE V and PHASE W.
3. Connect the External MCU Board suitable for motor control.
4. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J7.
5. For debugging/programming, connect a suitable USB SWD module to J1 by using a standard 4 wire cable.

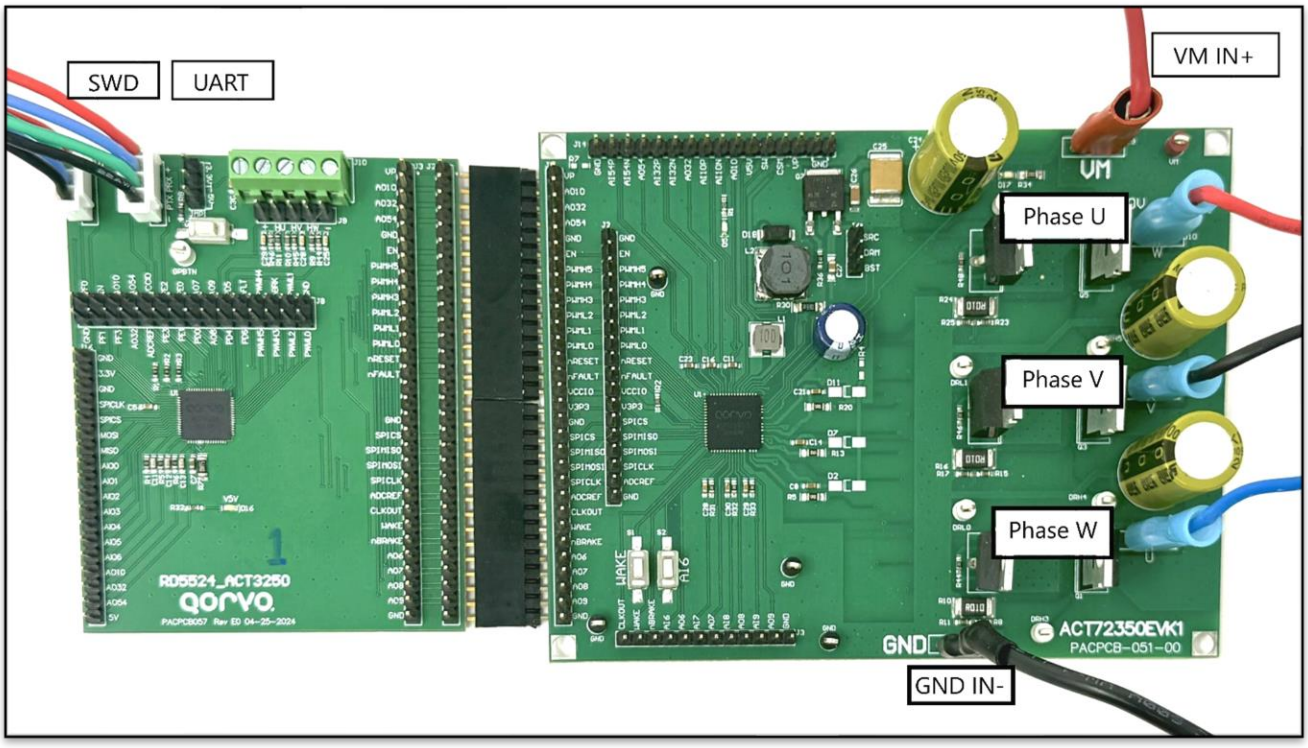

Figure 8: ACT72350EVK1 Evaluation Module Connections

CONTACT INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

IMPORTANT NOTICE

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**
Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.