1 Introduction

This User Manual describes how to use the Crystal Procurement Tool. This tool can be used to check if the electrical parameters, given in the crystal specification, can meet Qorvo procurement requirements. As the 2.4 GHz carrier frequency of Qorvo communication-controllers (“chips”) is also derived from the external crystal (i.e., 32 MHz or 16 MHz for older generations), the device will not be able to meet frequency offset specifications if the crystal is not meeting our requirements.

IEEE 802.15.4 PHY specifications require a maximum carrier frequency tolerance of ± 40 ppm under different operating temperatures and over product lifetime. This limit includes the offsets introduced by the initial frequency tolerance at 25 ºC, frequency stability over temperature range, aging over lifetime and frequency variations due to variations in the load capacitance.

This tool will also examine if the loop gain is sufficient to oscillate reliably without overdriving the crystal, even in corner cases. Therefore, a reliable and accurate carrier frequency can be guaranteed.

Note: crystal / RF carrier frequency calibration is not required during production.

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2 Getting Started with the Crystal Procurement Tool

Before getting started with the Crystal Procurement Tool, please make sure the crystal specification contains the electrical parameters as listed in Table 1 below. If there is any missing parameter, please contact the crystal vendor for this data. Otherwise, using this tool will cause incomplete results or an error message.

Table 1: Required Electrical Parameters from the Crystal Specification

Parameter	Symbol	Unit
Load Capacitance	CL	pF
Maximum Drive Level	DL (max)	µW
Maximum Shunt Capacitance	C0 (max)	pF
Maximum Equivalent Series Resistance	ESR (max)	Ω
Frequency Tolerance at 25°C	|ΔF0/F0|	ppm
Aging 1st year	|Fa|	ppm
Frequency Stability (over operating temperature)	|TC|	ppm
Trim Sensitivity / Pulling Factor *	TS	ppm/pF
Typical Shunt Capacitance *	C0 (typ)	pF
Motional Capacitance *	C1 (typ)	fF

*Please fill in either Trim Sensitivity / Pulling Factor or both typical Shunt Capacitance and typical Motional Capacitance.

2.1 Project Information

Please select or enter the following parameters:

a. Qorvo chip
By selecting the desired Qorvo chip in the dropdown list, the required crystal frequency will be shown in the field **Crystal Nominal Frequency**. For example, 32 MHz is used when the GP570 is selected.

b. Operating Temperature
This parameter is only available for selection of chips supporting high temperature applications.

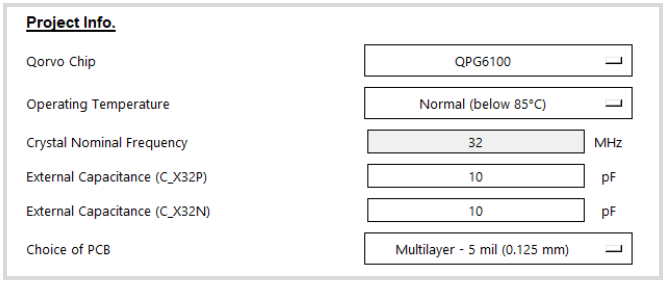

Figure 1: Chip Parameters

c. Crystal Nominal Frequency
This field shows the required crystal frequency of the selected Qorvo chip.

d. External Capacitance (C_X32P) / External Capacitance (C_X32N)
These are the external capacitors connected to pin X32MP and X32MN on the chip as shown in Figure 2 below. These two capacitances, together with the chip's and parasitic capacitances, determine the actual load capacitance for the crystal. If incorrect values are used, suggested values can be found with **Result – Load Capacitance**. Therefore, the user can start with a guess of these parameters.

Note: C_X32P and C_X32N should have equal values. If it is not possible to meet the required load capacitance with equal values, the C_X32P value should have a smaller value than C_X32N.

e. Choice of PCB
Please select the appropriate PCB layer type and its thickness (RF signal to RF GND) from the list.

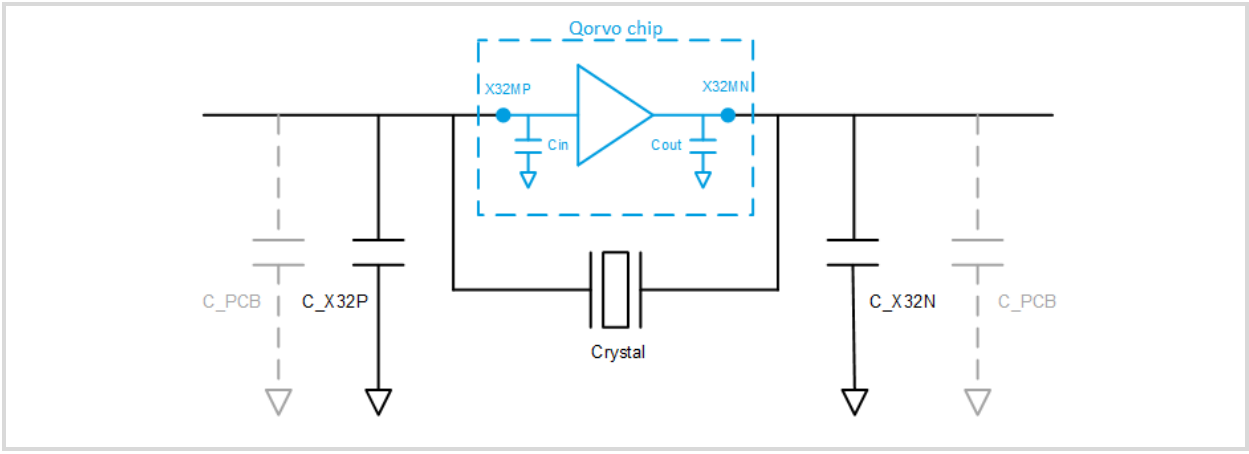

Figure 2: Connections between Crystal, External Capacitors and the Qorvo Chip

! The difference between capacitance C_X32P and C_X32N should be a maximum of one step in the E12 range. Also, Qorvo requires C_X32P ≤ C_X32N.

2.2 Crystal Parameters

Please enter the parameters, as shown in Figure 3 below, according to the crystal's datasheet. If there is any item missing, an error message will pop up. For example, when the trim sensitivity of the crystal is missing, an error will be reported as shown in Figure 4. Please contact the crystal vendor for the missing item(s).

Crystal Specification

Load Capacitance :	CL	8	pF
Maximum Drive Level :	DL (max)	150	µW
Maximum Shunt Capacitance :	C0 (max)	2	pF
Maximum Equivalent Series Resistance :	ESR (max)	50	Ω
Frequency Tolerance at 25 degrees :	ΔF/F0	10	ppm
Aging 1st Year :	|Fa|	3	ppm
Frequency Stability (over Operating Temperature) :	|TC|	15	ppm
Trim Sensitivity / Pulling Factor * :	TS	9.8	ppm/pF
Typical Shunt Capacitance * :	C0 (typ)		pF
Motional Capacitance * :	C1		fF

* Please fill in both Typical Shunt Capacitance and Motional Capacitance

Figure 3: Input for Crystal Parameters

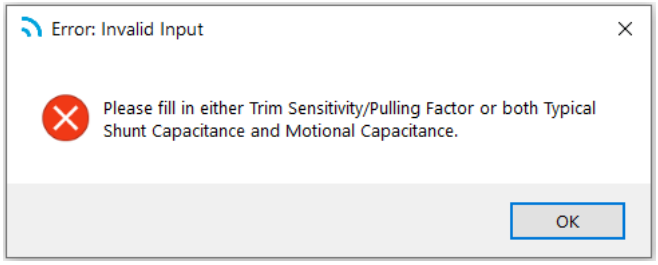

Figure 4: Error Message for Missing Crystal Parameter

3 Results

Once all the parameters are entered, the results can be obtained by clicking the button titled **Load Results**. The results will be shown in both text and graphical format. Please make sure all displayed results are “Pass” before further using the Crystal Procurement Tool.

3.1 Load Capacitance

Based on the external capacitance (C_X32P/ C_X32N), on-chip and parasitic PCB capacitance, the total load capacitance will be calculated by the tool. Then, the frequency error due to load capacitance mismatch can be found.

3.1.1 Pass

It means that the external capacitances (C_X32P / C_X32N) are correct and the calculated actual load capacitance and frequency error introduced by the residual load capacitance offset will be shown.

3.1.2 Marginal

The frequency error due to the selected external capacitance (C_X32P / C_X32N) is slightly higher than our requirement. It is still acceptable, but Qorvo highly recommends using the suggested values to further minimize the frequency error.

3.1.3 Fail

The frequency error due to the selected external capacitance (C_X32P / C_X32N) is higher than our requirement. Please use the suggested values.

3.2 Maximum Drive Level

Although the crystal is driven by the chip’s internal circuit using automatic gain control, there is possibility that the circuit will over-drive the crystal in corner cases (the worst C0-ESR combination) and cause damage to it. Therefore, a check is needed to verify if the crystal maximum drive level is enough. The drive level in the application is calculated based on the crystal maximum shunt capacitance C0 (max), maximum Equivalent Series Resistance ESR (max) and actual load capacitance.

3.2.1 Pass

No problem expected with the maximum drive level.

3.2.2 Fail

The maximum drive level of the crystal is too low; the actual drive level may cause damage to the crystal. Please contact the crystal vendor for another crystal with higher maximum drive level. Reducing the maximum C0 and or ESR will also reduce the drive level.

3.3 C0-ESR Combination

There is a requirement on the combination of the maximum shunt capacitance C0 (max) and the maximum Equivalent Series Resistance ESR (max) such that the loop gain of crystal oscillator circuit is enough for reliable oscillation.

3.3.1 Pass

If the maximum ESR (green triangle) from the crystal is below the dotted green line (in the green region), the crystal oscillator will oscillate reliably, see Figure 5.

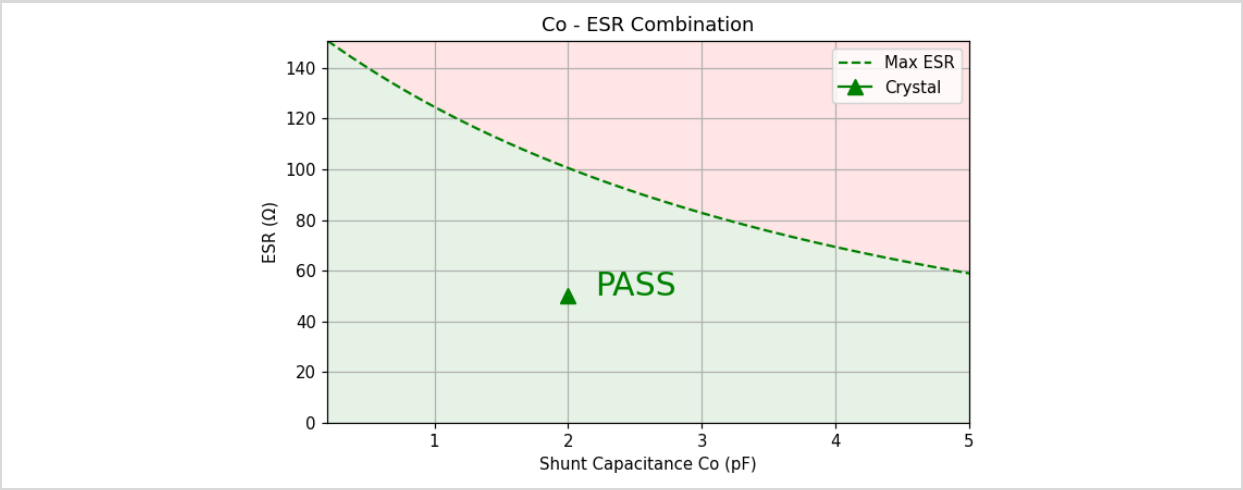

Figure 5: C0 and ESR (max) Combination - Pass

3.3.2 Fail

If the maximum ESR (red triangle) from the crystal is above the dotted green line (in the red region), as shown in Figure 6, it implies the ESR (max) and/or C0 (max) are too high. Please contact the crystal vendor for a crystal with a lower ESR (max) and or lower C0 (max).

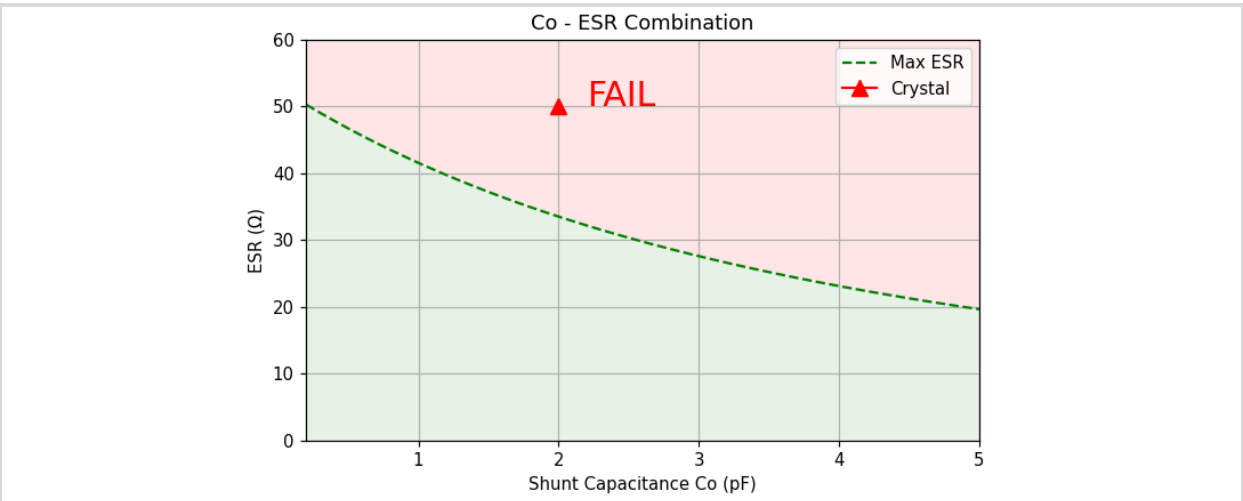

Figure 6: C0 and ESR (max) Combination - Fail

3.4 Frequency Offset Error

The total frequency offset error includes:

1. frequency tolerance at 25 °C,
2. frequency error due to trim sensitivity, as known as the “pulling effect” of load capacitance offset, i.e., the frequency error due to load capacitance mismatch (refer to Section 3.1),
3. aging and
4. frequency drift over operating temperature. The IEEE 802.15.4 PHY specification requires a maximum carrier frequency tolerance of ± 40 ppm, the remaining margin can be calculated by the tool.

3.4.1 Pass

Whenever there is margin remaining, the crystal can pass Qorvo’s requirements. It implies that there is no issue, even at corner cases.

3.4.2 Fail

In case of a fail, a user can either update the external capacitance (C_X32P / C_X32N) if the result in section 3.1 is marginal, or find another crystal with lower frequency tolerance at 25 °C, lower aging or lower frequency drift over operating temperature. When changing the external capacitors (C_X32P / C_X32N) please click the **Load Results** button to see the effect.

3.5 Frequency Offset Limits at Room Temperature

This section will check if the crystal has enough margin to guarantee accuracy over product lifetime and provides test limits for production testing.

3.5.1 Pass

The crystal circuit has enough margin and a production test limit is recommended.

3.5.2 Fail

The crystal does not have enough margin (< 14 ppm). This may introduce yield loss at finished good (end-product) production test. Please find another crystal with a lower frequency offset at 25 ˚C, lower aging or a better frequency stability over the operating temperature range.

3.6 Frequency Error due to Tolerance of Capacitors

Throughout the tool's analysis, the external capacitances (C_X32P and C_X32N) are assumed to be with 2% tolerance. However, some customers may desire to further reduce BOM cost by loosening the tolerance of these capacitors. For that option, the frequency error due to tolerance of capacitors is provided (see Figure 7). If the maximum frequency pulling error for that particular tolerance stays in the green region (Pass) or yellow region (Marginal), the settings are fine to use.

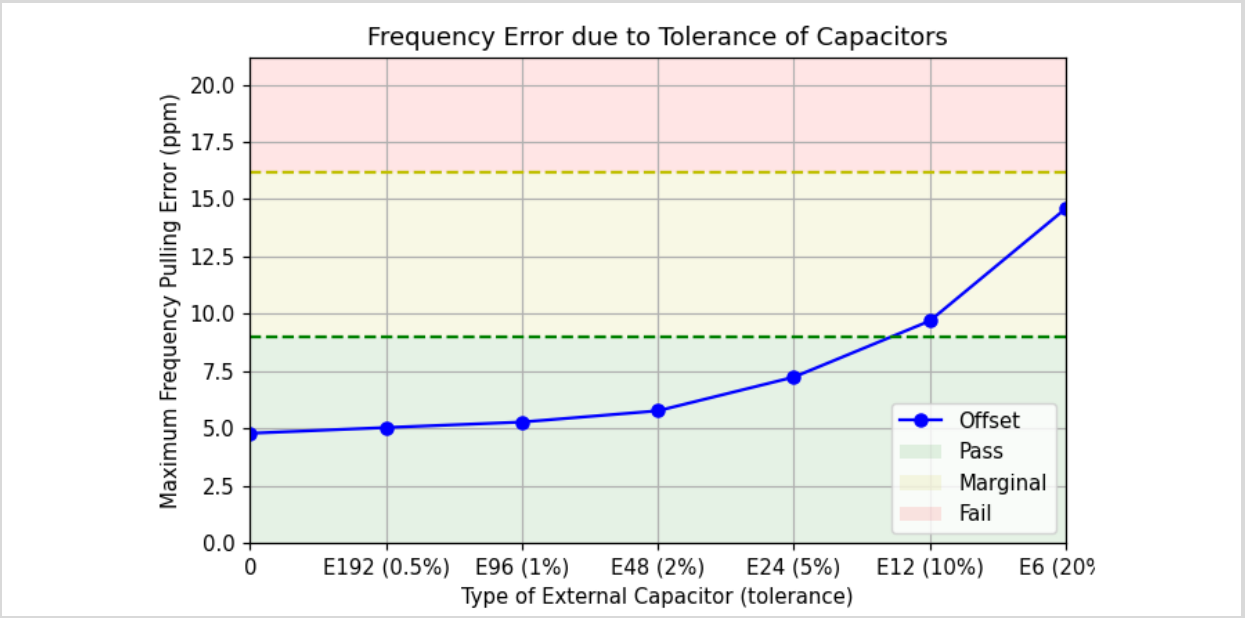

Figure 7: Frequency Error due to Tolerance of External Capacitors

3.7 Generation of Header File

When all the results are passed (green), header file can be generated and used in the software. In the Crystal Procurement Tool select menu item **File → Generate SDK BSP Header File** (see Figure 8 below), enter the crystal part number for reference, browse the file destination. Then, *gpAppUcSubsystem_CalibrationDefaultsForEVB.h* will be generated.

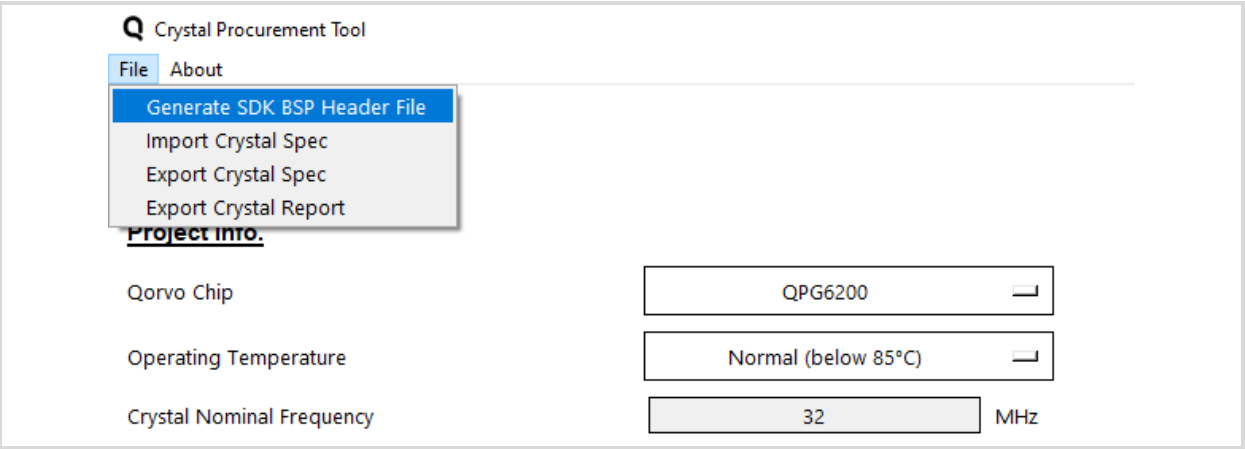

Figure 8: BSP Header File Generation

! This feature is available only for specific chips.

3.8 High Temperature Applications

This section is only applicable to Qorvo chips that support high temperature applications (e.g., smart LED bulbs). These chips have a maximum operating temperature up to 125 °C. For high temperature applications it is necessary to examine if the internal switching capacitors in the Qorvo chip can correct the crystal's temperature drift to meet the required frequency offset error limit under extreme operating temperature conditions. Therefore, the characteristic of the crystal's frequency stability over its operating temperature (-40 ˚C to 125 ˚C) is required.

This tool supports both a manual 3-zone compensation and an optimized multiple zone compensation. The 3-zone frequency trimming is used as the first order assessment on the selected crystal, this allows users to get familiar with the frequency trimming mechanism. The multiple zone one is the recommended trimming topology for application use. User can go to Section 3.8.2 and 3.8.3 directly if they aim to get the best board support package (BSP) setting directly.

To start with, the frequency offset characteristic of the crystal must be entered into the tool. This frequency characteristic will be divided into three temperature regions based on the zero-crossing points (i.e., frequency offset due to temperature |TC| = 0 ppm). The first zero-crossing typically occurs at 25 °C, while the second is crystal dependent. The region below 25 °C is defined as the *Low temperature range*. The region between the first and second zero-crossing is the *Mid temperature range* and the region above the second zero-crossing is the *High temperature range*. See also Figure 9 for clarification.

By entering the averaged value of maximum and minimum frequency offset in each temperature range, the whole frequency characteristic over temperature range of the crystal will be modelled by this tool.

Note: The curve is just a modelling based on the provided zero-crossing points, maximum and minimum frequency offset.

For example, the crystal vendor provides a temperature offset curve as shown in Figure 9. For the *Low temperature range* (always -40 ˚C to 25 ˚C), the maximum value is ~ +19 ppm while the starting value is +12 ppm at -40 ˚C. Therefore, the value in (a) and (b) in the Frequency Trimming section of the tool (see Figure 10) must be set to 12 and 19 ppm respectively. For the *Mid temperature range*, (c) must be set to the worst condition, i.e. -22 ppm. Similarly, the maximum point (d) must be set to +26 ppm in the *High temperature range*. As the second zero crossing is around 110 °C, (e) must be set to 110 °C. Note that the lower left field automatically copies (e).

The function of the slider bars (Switch Capacitance Mode) will be discussed in Section 3.8.1.

Note: For now, keep the slider bars to **Mode 0**.

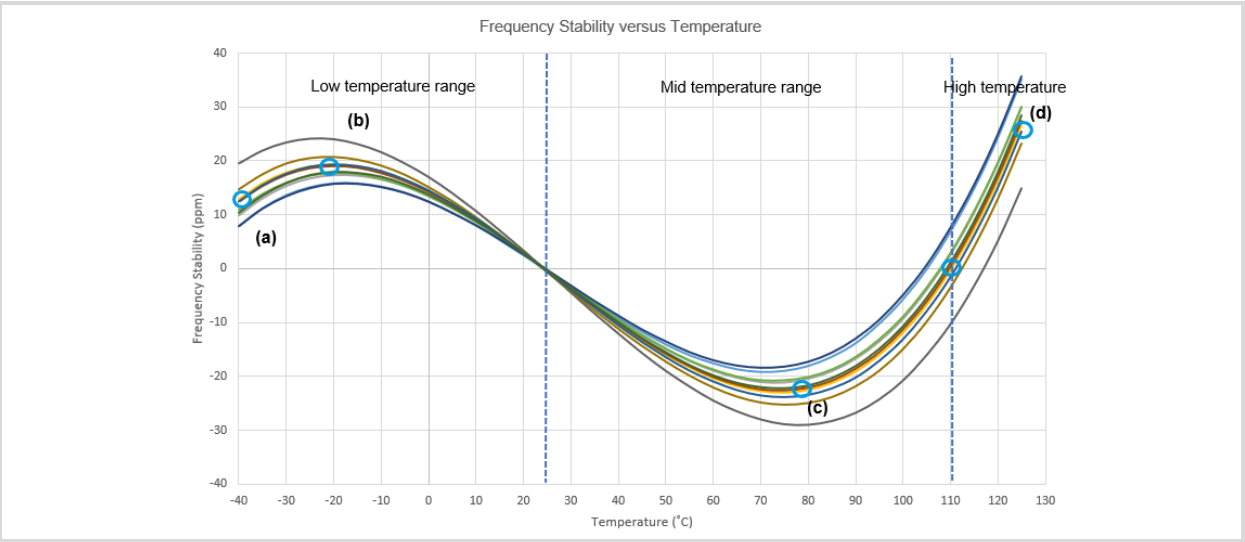

Figure 9: Frequency Offset over Temperature

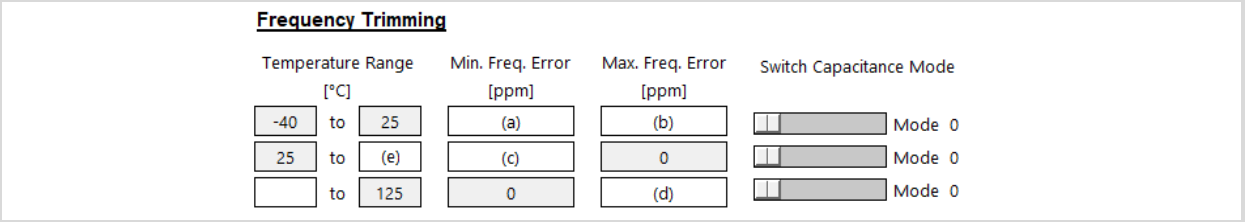

Figure 10: Crystal Input for Frequency Offset over Temperature

Once all the rest of the results are Pass, user can see the modelled temperature offset curve as shown in Figure 11. The dotted line is the modelled frequency error curve of the crystal while the solid blue line is the modelled curve using the actual load capacitance in the circuit, so considering frequency offset due to the external capacitors, trace capacitance and chip pin capacitance (= actual load capacitance). The blue shaded region is the frequency error considering capacitance tolerance. The target is to get all curves, including the shaded curves, inside the green (Pass) region.

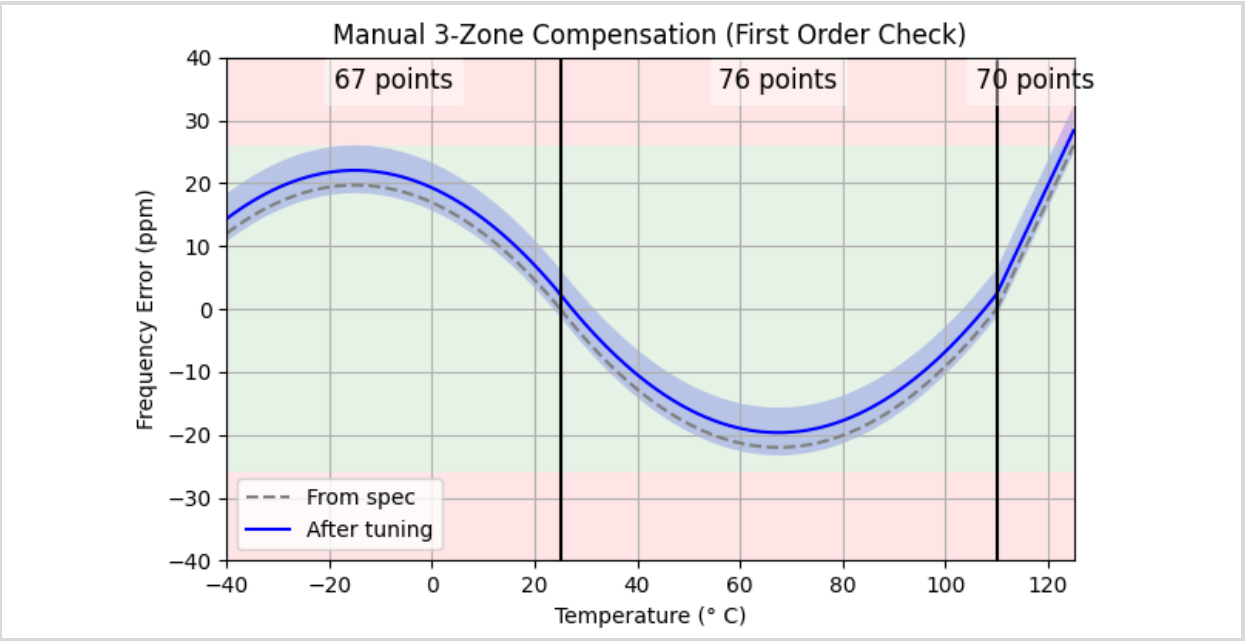

Figure 11: Frequency Error versus Temperature

The red (Fail) regions in Figure 11 are calculated based on frequency tolerance at 25˚C and aging.

3.8.1 Manual 3-Zone Compensation (First Order Check Only)

The frequency stability over operating temperature characteristic curve is divided into 3 zones where the internal switching capacitor setting can be tuned manually in each zone and the external load capacitances should also be optimized if needed. Scores are given for each temperature range (the number above the curve) to show how good it is. The higher the number, the better the frequency accuracy is (100 points is perfect). The target is again to have the whole temperature offset curve inside the green region. To achieve that, there are 2 methods introduced below.

Note: Manual 3-Zone compensation is just for first order check (not implement).

3.8.1.1 Method 1 – Switching Capacitors

Switching capacitors are available in Qorvo chips that are rated for an operating temperature of 125 °C. User can make use of the on-chip 4-step switching capacitor (sliding the bar in the **Frequency Trimming** field) in the desired temperature range to turn on these additional capacitors.

There are four modes available; **Mode 0** has the lowest capacitance and **Mode 3** has the highest capacitance. User can enable these on-chip capacitances to tune the resultant load capacitance and thus, “pull down” the frequency offset curve in the desired temperature range. This is used to compensate for the positive frequency offset errors.

For example, the frequency offset of the crystal represented in Figure 11 fails in the low temperature range. Now, the user can enable **Mode 2** in the low temperature range to pull the curve down to the green region as shown in Figure 12 and Figure 13.

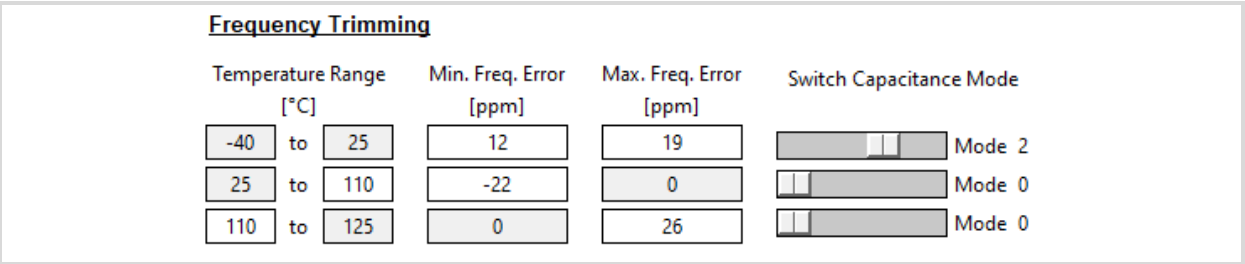

Figure 12: Frequency Trimming Slider Bar

Note: the temperature compensation can be further improved by also selecting Mode 3" or "Mode 2" for the 110 ˚C to 125 ˚C temperature range.

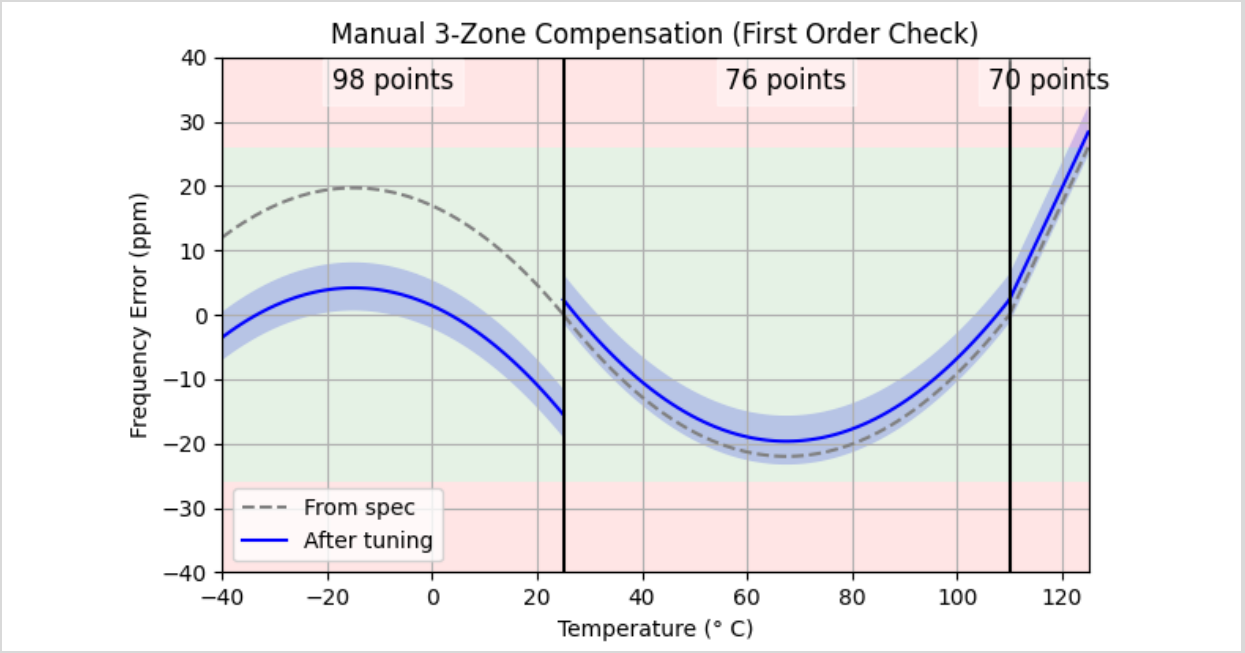

Figure 13: Frequency Error Curve after Using Method

3.8.1.2 Method 2 – Changing the External Capacitor and Switching Capacitor

The limitation of Method 1 discussed in Section 3.8.1.1 can compensate for the positive frequency offset error but not for the negative, i.e. the frequency offset curve can be pulled down from **Mode 0** to **Mode 3** but not able to be pulled up from **Mode 0**. **Method 2** discussed in this section is to detune the external load capacitances in advance to **Method 1**. The idea is to reduce the load capacitance to a lower value that introduces positive frequency offset in **Mode 0**. As a result, the curve is then shifted up to compensate the negative frequency offset error.

For initial guess, the value of the external capacitors should be chosen such that these capacitances are about 1.5 pF (QPG6095) or 3 pF (QPG6100 / QPG6105) smaller than the external caps (C_X32P and C_X32N) that give lowest offset at 25 degrees. Then, user can pull down the curve by enabling the switching capacitor in the corresponding temperature range such that the crystal meets the Qorvo requirements.

For example, when the crystal configuration fails as shown in Figure 13 (the curve in mid temperature range cannot fall into the green region with switching capacitor – pull down only), so user can reduce the capacitance of C_X32P and C_X32N to pull up the curve.

After updating C_X32P and C_X32N, result will update by clicking the button **Load Result**. Then, the entire frequency offset curve (solid blue line) will be pulled up. However, it may still fail in a certain temperature region. At that time, user can make use of the switching capacitors, using the slider bar, to “pull down” the temperature offset curve in the desired temperature range.

Eventually, the temperature offset curve will be within the green region and get the highest scores with the low, mid, and high temperature range setting as mode **3**, mode **0** and mode **3** respectively as shown in Figure 14.

! Make sure Mode 0 is selected for the complete temperature range before using Method 2.

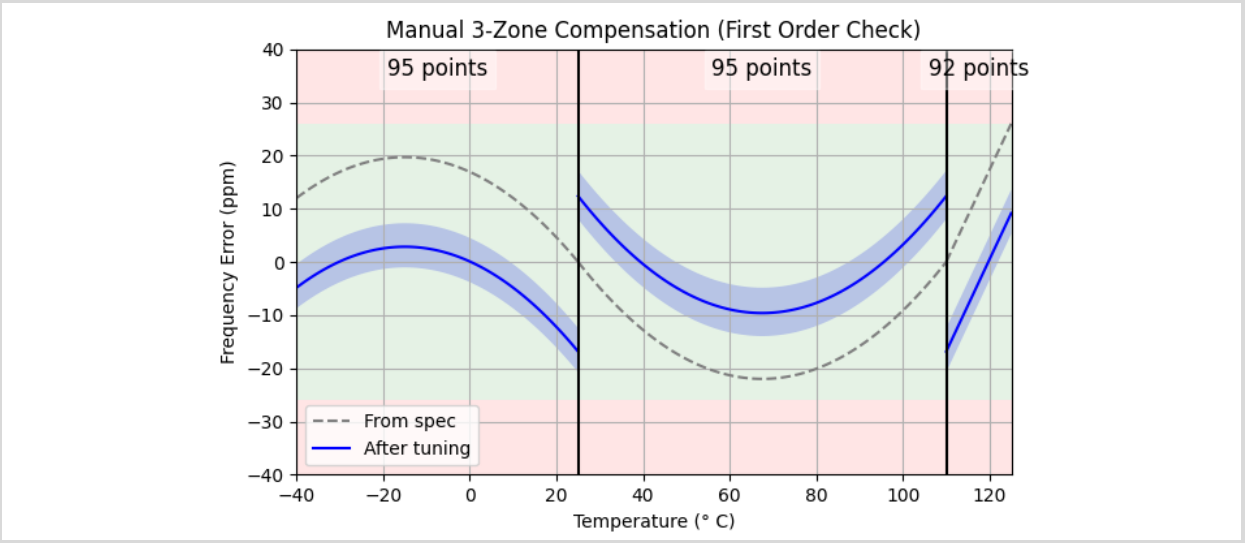

Figure 14: Example of Frequency Error versus Temperature

3.8.2 Automated Optimized Multiple Zone Compensation

The tool will provide the optimized multiple zone compensation as a BSP header file directly if the frequency characteristic of the crystal is correctly entered. Therefore, user can neglect the slide bars in the **Frequency Trimming** field and the plot of “*Manual 3-Zone Compensation (First Order Check)*”. User only needs to check the results in **High Temperature** and the plot of “*Optimized Multiple Zone Compensation*”.

! Make sure all the results in the previous sections are “Pass” (Load Capacitance, Maximum Drive level, C0-ESR Combination) before jumping to this section

3.8.2.1 Pass

If the complete curve (solid blue line and blue shaded region) in all temperature ranges is within the green region, the crystal can pass Qorvo's requirements.

The result in **High Temperature** will be shown as follows:

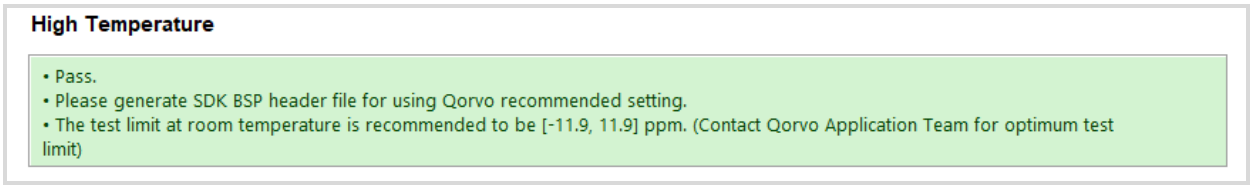

Figure 15: Result of High Temperature – Pass

If only the blue solid line (not all the blue shaded region) is in the green region, the crystal can still pass our requirements. But the tolerance of the external capacitance (C_X32P and C_X32N) must be at least E48 (2%).

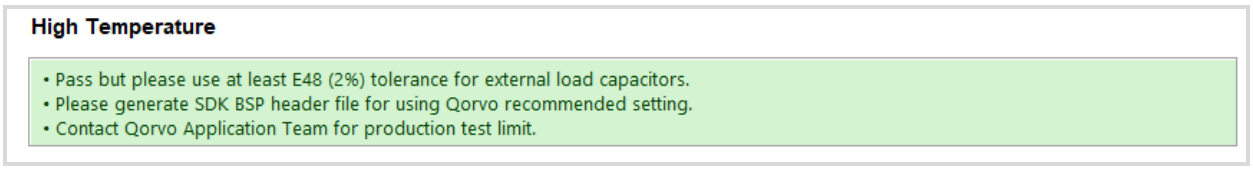

Figure 16: Result of High Temperature – Pass with Restriction

Note: The recommended test limits for the finished good production test of the DUT are calculated for a test condition from 20°C to 40°C with crystal frequency offset algorithm enabled. User can contact Qorvo Application Team for optimum test limit.

3.8.2.2 Fail

If other external capacitors provide better result, the tool will ask user to change them. Please follow the recommendation to update the C_X32P and C_X32N.

The result in **High Temperature** will be shown as follows:

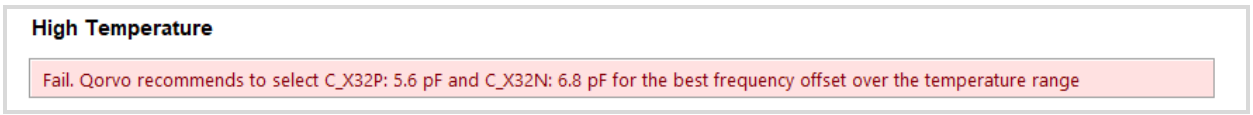

Figure 17: Result of High Temperature - Fail 1

In the case that the frequency offset error over the crystal's operating temperature varies too much, result will be shown in the tool's **High Temperature** section as depicted in Figure 18. Another crystal, with lower temperature offset over the operating temperature, is then needed.

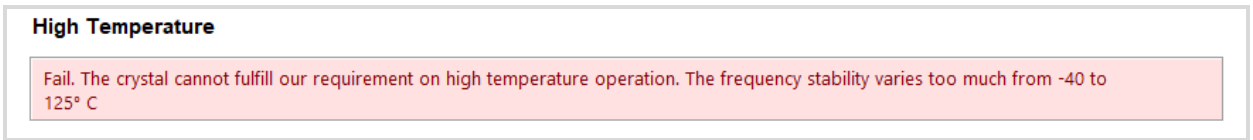

Figure 18: Result of High Temperature - Fail 2

3.8.3 Generation of Header File for High Temperature Application

Once all the results are passed (green), the optimized setting will be shown in the plot "*Optimized Multiple*

Zone Compensation". For example, from -40˚C to 6˚C use Mode 3; from 6˚C to 18˚C use Mode 2; as shown in Figure 19.

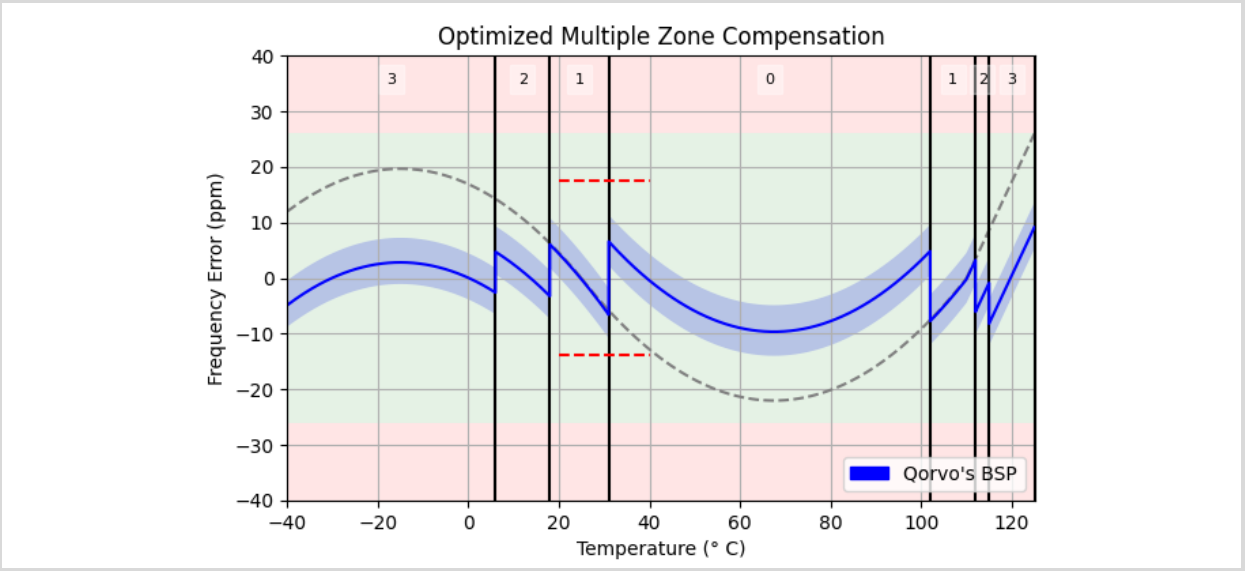

Figure 19: Optimized Multiple Zone Compensation

The next step is to generate the SDK BSP header file and include it in the software, so that the mode and temperature range settings can be implemented. In the Crystal Procurement Tool select menu item **File → Generate SDK BSP Header File** (see Figure 20 below), enter the crystal part number for reference, browse the file destination. Then, *gpBsp_TrimXtal_XXpF.h* (where XX is the load capacitance of the crystal) or *gpAppUcSubsystem_CalibrationDefaultsForEVB.h* will be generated.

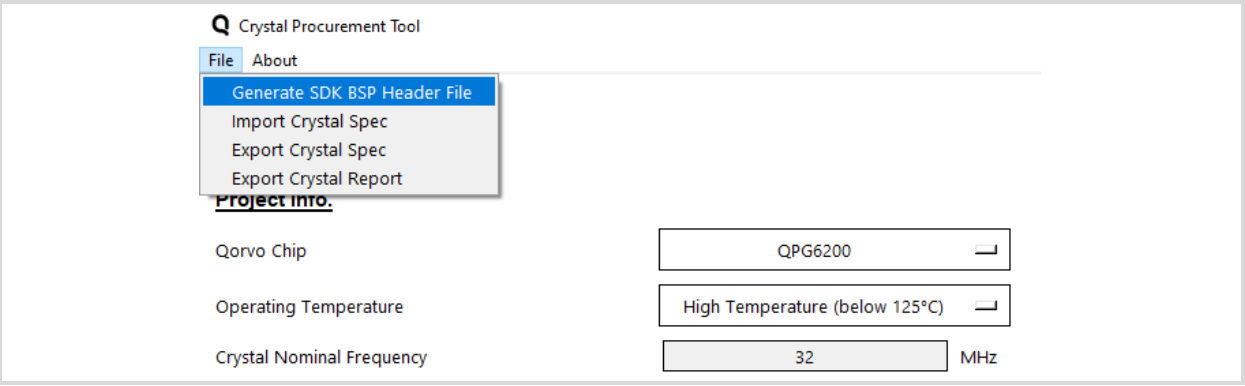

Figure 20: SDK BSP Header File Generation – High Temperature Application

4. Generate Report

Once all the results are passed (green), the crystal can pass Qorvo's 16 / 32 MHz crystal procurement requirements. The next step is to generate the report and share it, together with the crystal's datasheet, with the Qorvo hardware application team for a final check.

In the Crystal Procurement Tool select menu item **File → Export Crystal Report** (see Figure 21 below). Then, browse the file destination and enter a file name for the report.

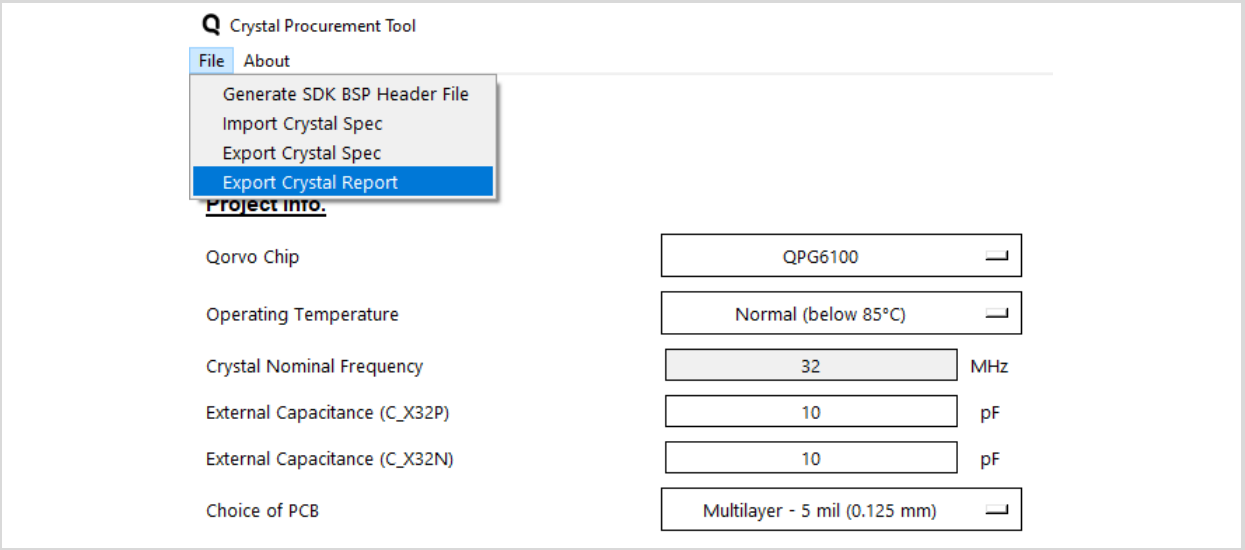

Figure 21: Report Generation

Parasitic Capacitances Crystals

Depending on the crystal manufacturer and depending on the size of the crystal package there are hidden parasitic capacitors present in the crystal. These parasitic capacitances are located between the two active pins of the crystal and the crystal ground pins. This means that the parasitic capacitances are in parallel with C_X32P and C_X32N, see Figure 22 below. These parasitic capacitances are normally NOT mentioned in the crystal data sheets.

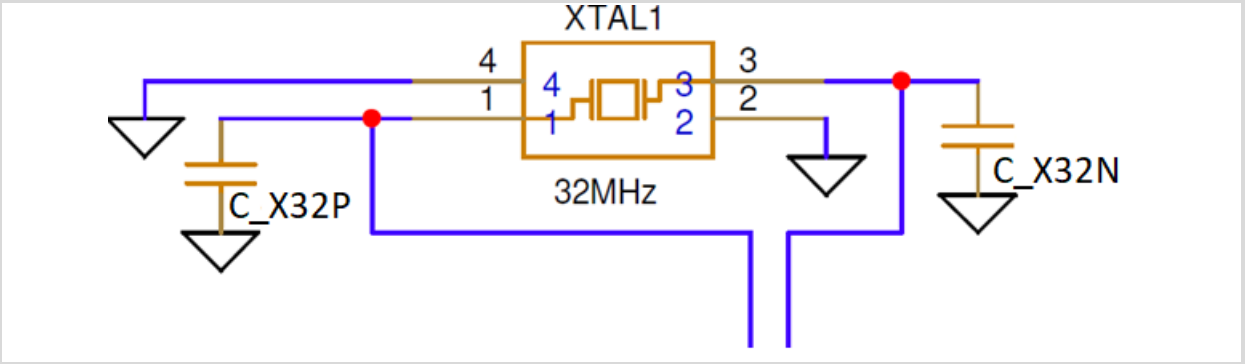

Figure 22: Schematic Crystal with External Load Capacitances

Values parasitic capacitances:

- Crystal size code 3225 (3.2 * 2.5 mm): between about 0.2 pF and 0.7 pF per pin
- Crystal size code 2016 (2.0 * 1.6 mm): between about 1.0 and 1.5 pF per pin.

The parasitic capacitances are most of the time not equal for the two active pins, further the parasitic capacitances may differ per crystal manufacturer. The impact of these parasitic capacitances is that they will lower the oscillation frequency of the crystal oscillator depending on the trim sensitivity of the crystal.

Recommendations:

- Always ground the crystal. If the crystal is not grounded the two parasitic capacitances will be in parallel to C0 and reduce the oscillator gain and increase the drive level of the crystal.
- Limit the Cload pull-ability or trim sensitivity of the crystal.
  Qorvo recommends using a Cload of 12 pF (or higher) for normal temperature applications up to 85 degrees Celsius. (Extended range up to 105 degrees Celsius depending on crystal).
- In case of 125 degrees Celsius applications Qorvo recommends a Cload of 9 pF.
- If needed, lower the C_X32P and C_X32N values to center the average frequency offset of a large batch to be around 0 ppm. The adjustment of the external load caps should be in the same range as the parasitic capacitances of the crystal.

References

[1] 16 MHz Crystal – 20 pF; Qorvo document GP_P004_PS_01620
[2] 16 MHz Crystal – 3225; Qorvo document GP_P004_PS_02507
[3] 32 MHz Crystal – Metal Can; Qorvo document GP_P007_PS_06541
[4] 32 MHz Crystal – 3225; Qorvo document GP_P007_PS_06542
[5] 32 MHz Crystal – 2016; Qorvo document GP_P007_PS_06543
[6] 32 MHz Crystal – 2520; Qorvo document GP_P007_PS_06544

Abbreviations

XTAL	Crystal	GND	Ground
PCB	Printed Circuit Board	PHY	Physical Layer
RF	Radio Frequency	ESR	Equivalent Series Resistance

Important Notices

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Document History

Version	Date	Section	Changes
1.0	26 Jan 2021		Approved version.
1.1	16 Feb 2022	3.7	Update section.
1.2	9 Jan 2023	3, 4	Remove tool version number from figures
1.3	16 Aug 2023	3.7.2.1	Update production test limit
1.4	25 Mar 2024	3.7.2.1	Update production test limit based crystal procurement tool v1.3.0
1.5	17 Jul 2024	3.7	Add generation of header file for normal application based on crystal procurement tool v1.3.2
1.6	29 Nov 2024	3.7	Rename header file