ACT72350 Data Sheet

160V 3-phase BLDC Motor Driver with Integrated Power Manager and Configurable AFE

Configurable Analog Front End™

Application Specific Power Drivers™

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1 GENERAL DESCRIPTION

The ACT72350 is an integrated three-phase BLDC/PMSM motor driver optimized for medium voltage applications. Derived from the PAC5x32 family, it includes all necessary components except the microcontroller core, providing a comprehensive motor control solution.

Featuring Qorvo's proprietary technologies, the ACT72350 includes a Configurable Power Manager, a patent-pending Configurable Analog Front-End™, and Application Specific Power Drivers™. The Power Manager supports various power sources with a high-voltage switching supply controller, a medium-voltage regulator, and three linear voltage supplies.

The Application Specific Power Drivers (ASPD) are designed for half-bridge, H-bridge, and three-phase driving. The Configurable Analog Front End (CAFE) offers programmable gain amplifiers, comparators, and digital-to-analog converters for flexible signal processing and sensor monitoring.

The ACT72350 interfaces via tri-phase inverter PWM control signals, with an SPI port for register configuration. It allows easy integration with an external microcontroller core, enhancing design flexibility.

Available in a 57-pin, 9x9 mm QFN package, the ACT72350 is ideal for efficient, reliable motor control with reduced component count and enhanced safety features.

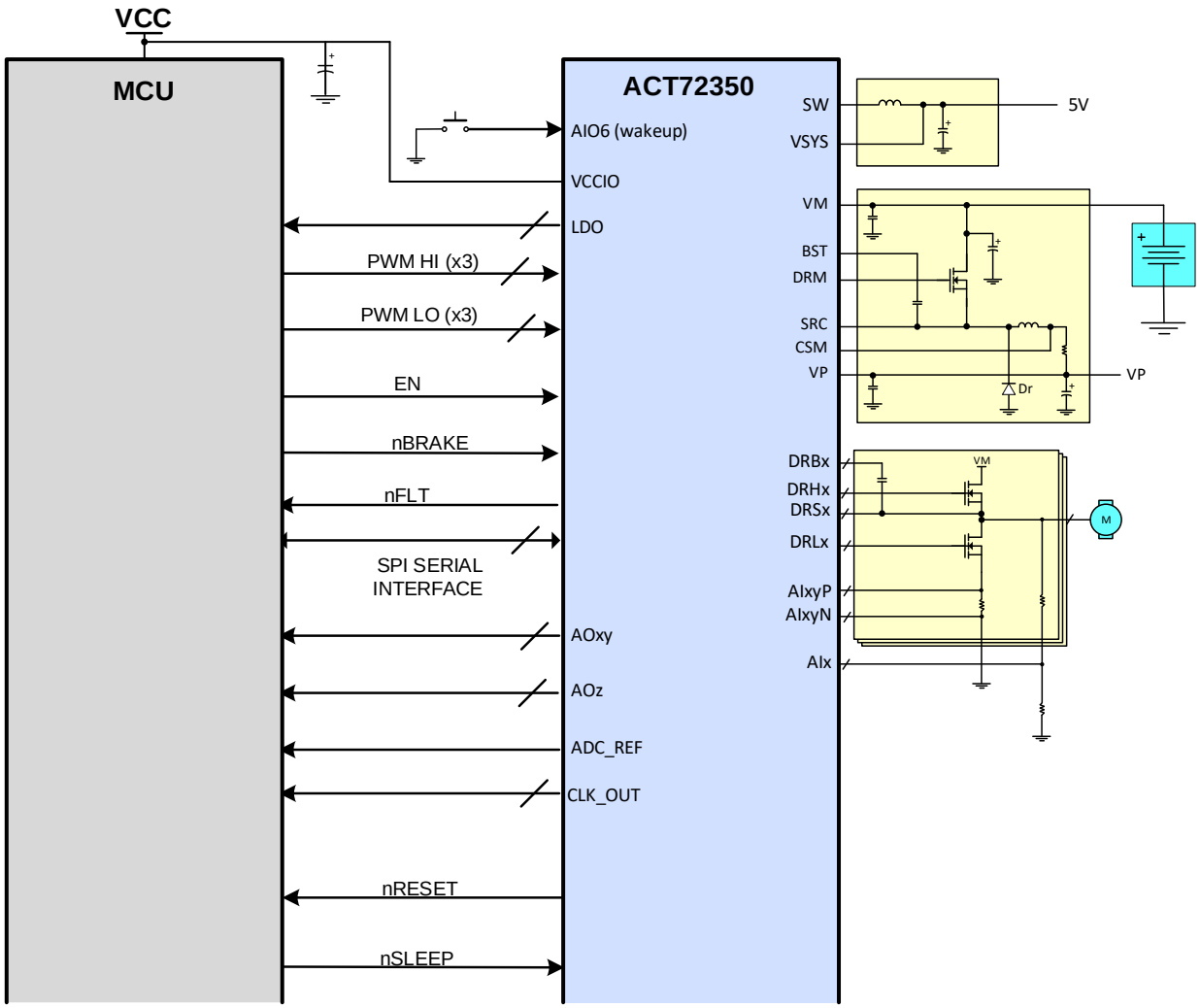
2 PAC FAMILY APPLICATIONS

The ACT72350 is ideal for battery powered applications between 48V and 120V.

Target applications for this device include:

- Power Tools
- Garden Tools
- Motor Controllers
- Drone/RC
- E-Bike
- E-Vehicle
- Ped-Electric Bikes
- Light HEV

Figure 2-1. Simplified Application Diagram



3 PRODUCT SELECTION SUMMARY

Table 3-1 Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END			APPLICATION SPECIFIC POWER DRIVERS				PRIMARY APPLICATION
		INPUT VOLTAGE	DC/DC	DIFF-PGA	PGA	COMPARATOR	DAC	VBST/VSRC	POWER DRIVER	PWM CHANNEL	
ACT72350	57L 9x9 QFN	25V-160V	Y	3	4	4	2	160V	3 LS (2A) 3 HS (2A)	6@VP	3 half-bridge 3 phase control BEMF Trapezoidal or FOC

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

4 ORDERING INFORMATION

Table 4-1 Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT72350-T	-40°C to 125°C	57L 9x9 QFN	57 + Exposed Pad	Tape & Reel (3K Units)

5 FEATURES

5.1 Feature Overview

- **Configurable Power Manager**
  - High-voltage buck switching supply controller
    - Input Voltage: 25V – 160V
    - Configurable Output Voltage: 12V or 15V
  - 5V medium-voltage switching supply regulator
  - 2 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 6 Over-Current Protection Comparators
  - 4 General Purpose Comparators with BEMF sensing Special Mode option
  - 2 10-bit DACs
  - SPI accessible
- **Proprietary Application Specific Power Drivers**
  - 3 160V (180V Bootstrap) high-side gate drivers with 2A gate driving capability
  - 3 low-side gate drivers with 2A gate driving capability
  - Configurable propagation delay and fault protection
  - PWM control interface

6 ABSOLUTE MAXIMUM RATINGS

The table below shows the absolute maximum ratings for this device.

To prevent damage to the device, do not exceed these limits. Exposure to the absolute maximum rating conditions for long periods of time may affect device reliability.

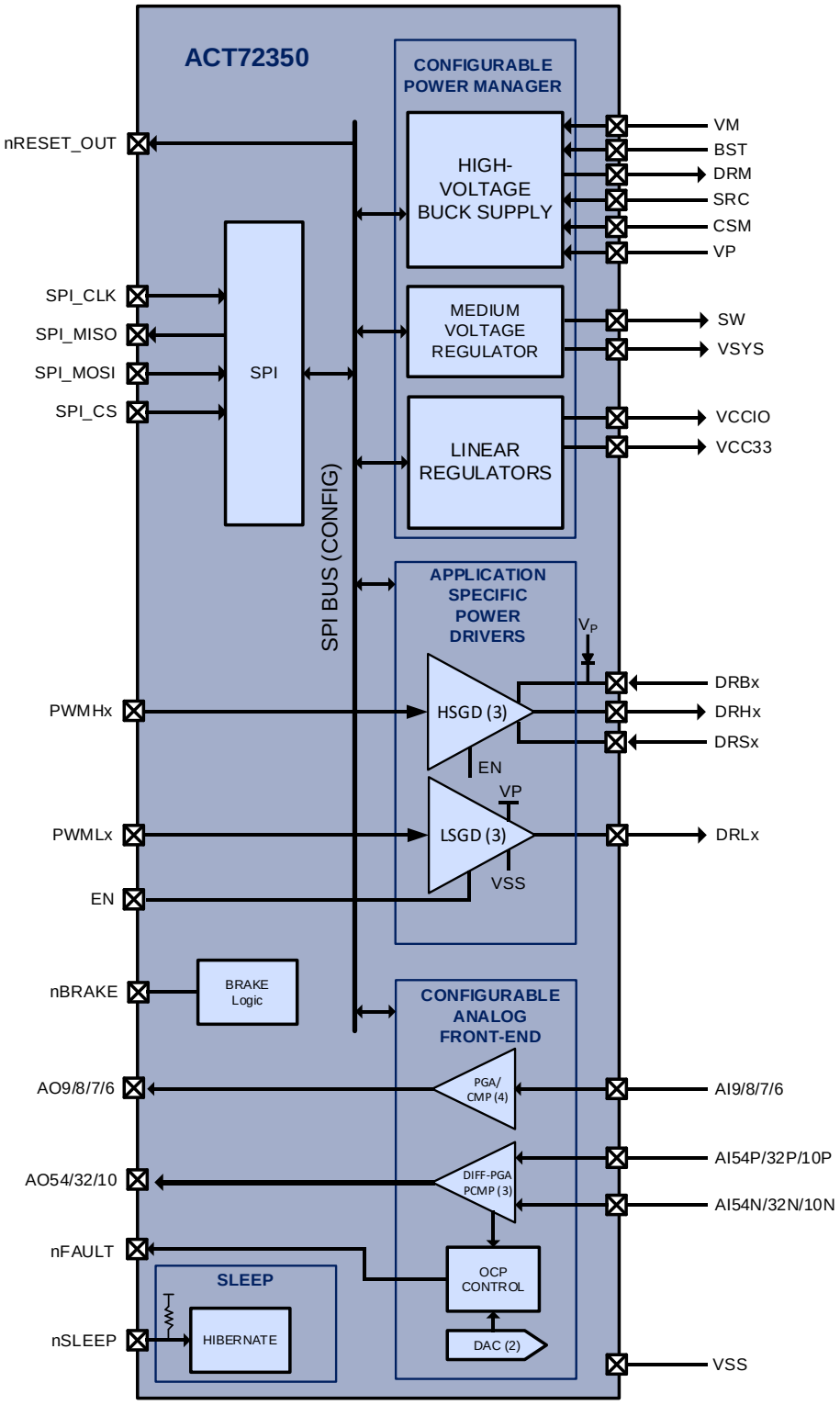
The device is not guaranteed to function properly outside of the operating conditions.

Table 6-1 Absolute Maximum Ratings

PARAMETER		VALUE	UNIT
VM to VSS		-0.3 to 160	V
BST to VSS		-0.3 to 180	V
BST to SRC		-0.3 to 20	V
SRC to VSS		-10 to VM + 15	V
DRM to SRC		-0.3 to 20	V
VP to VSS		-0.3 to 20	V
SW to VSS		-0.3 to V_P + 0.3	V
CSM to VP		-0.3 to 0.3	V
VSYS, AI6 to VSS, AO6 to VSS		-0.3 to 6	V
AI<9:7>, AI<5:0> to VSS		-0.3 to V_{SYS} + 0.3	V
AO<9:7>, AO<5:0> to VSS		-0.3 to V_{SYS} + 0.3	V
EN, nBRAKE to VSS		-0.3 to V_{SYS} + 0.3	V
ADC_REF to VSS		-0.3 to V_{SYS} + 0.3	V
nSLEEP to VSS		-0.3 to 6	V
CLK_OUT, PWMHx, PWMLx, SPI_CLK, SPIMOSI, SPIMISO, SPI_CS to VSS		-0.3 to V_{CCIO} + 0.3	V
VCC33, VCCIO to VSS		-0.1 to V_{SYS} + 0.3	V
DRL0, DRL1, DRL2 to VSS		-0.3 to V_P + 0.3	V
DRB3, DRB4, DRB5 to VSS		-0.3 to 180	V
DRS3, DRS4, DRS5 to VSS		-10 to 160	V
DRB3 to DRS3, DRB4 to DRS4, DRB5 to DRS5		-0.3 to 20	V
DRH3 to DRS3, DRH4 to DRS4, DRH5 to DRS5		-0.3 to V_{DRBx} + 0.3	V
VSS RMS Current		0.2	A_{RMS}
Operating ambient temperature range (T_A)		-40 to 125	°C
Electrostatic Discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV

7 ARCHITECTURAL BLOCK DIAGRAM

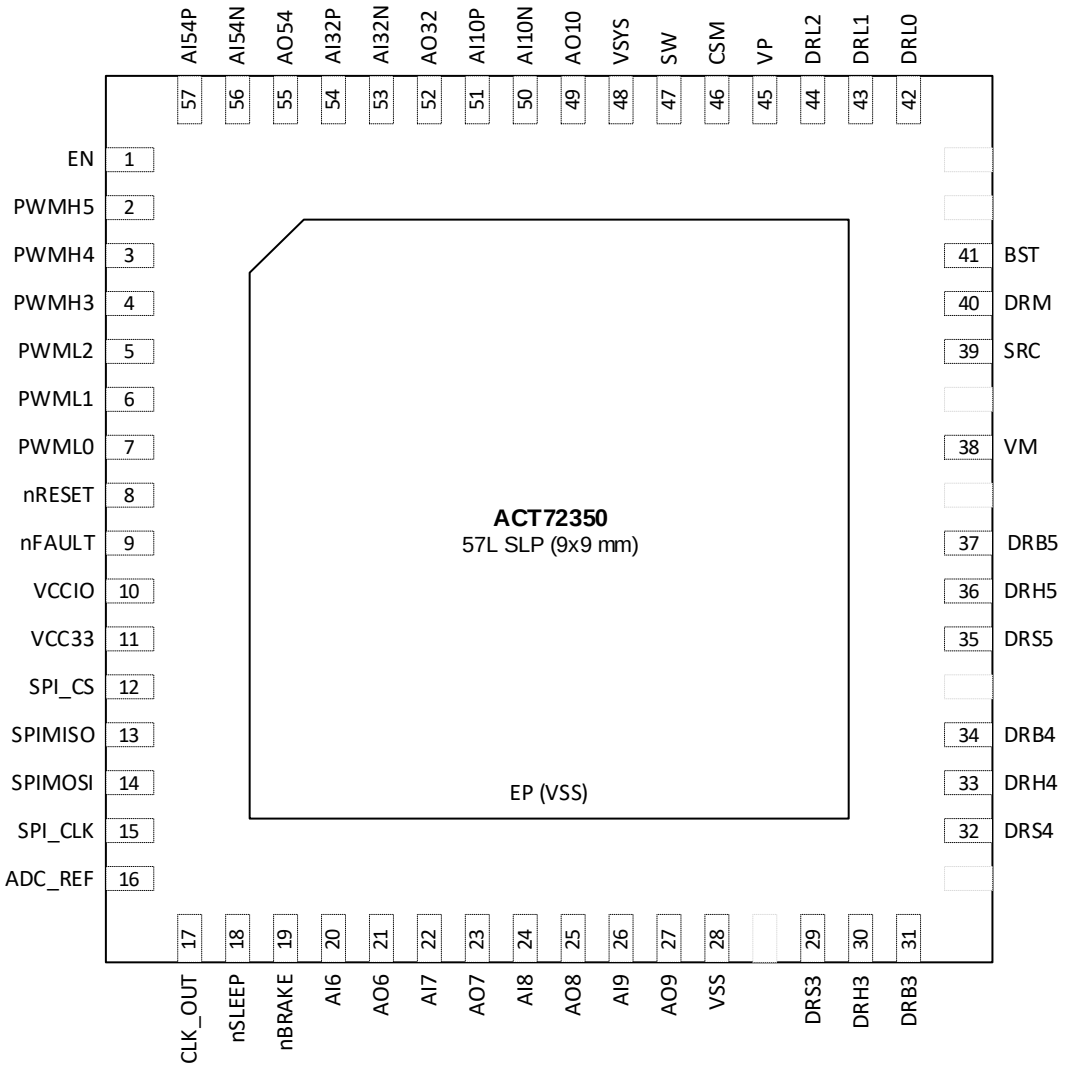
Figure 7-1 Architectural Block Diagram



8 PIN CONFIGURATION

8.1 ACT72350

Figure 8-1 ACT72350 Pin Diagram



9 PIN DESCRIPTION

9.1 Power and Ground Pin Description

Table 9-1 Power and Ground Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCCIO	10	Power	Internally generated digital I/O 3.3V power supply. Connect a 2.2μF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
VCC33	11	Power	Internally generated 3.3V power supply. Connect to a 2.2μF or higher value ceramic capacitor from V_{CC33} to V_{SSA}.
VSS	28	Power	Ground.
VM	38	Power	High-Voltage Buck Regulator supply controller input. Connect a 1μF or higher value ceramic capacitor, or a 0.1μF ceramic capacitor in parallel with a 10μF or higher electrolytic capacitor from VM to VSS. This pin requires good capacitive bypass to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
SRC	39	Power	High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator.
DRM	40	Power	High-Voltage Buck Regulator Switching supply driver output. Connect to the base or gate of the external N-channel MOSFET.
BST	41	Power	High-Voltage Buck Regulator bootstrap input. Connect a 2.2μF or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin.
VP	45	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10μF ceramic capacitor in parallel with a 100μF aluminum capacitor from V_P to V_{SS} for voltage loop stabilization. If the switching frequency of the HV-BUCK is >= 200kHz, then the 100μF aluminum capacitor can be replaced with 47μF, but the efficiency will be worse. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
CSM	46	Power	High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor.
SW	47	Power	Switch node for the medium-voltage buck regulator.
VSYS	48	Power	5V System power supply. Connect to a 22μF/10V (20%) or higher ceramic capacitor from V_{SYS} to V_{SS}.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

9.2 Signal Manager Pin Description

Table 9-2 Signal Manager Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
A010	49	DA10 OUT	Analog	Differential PGA 10 analog output
AI10N	50	DA10N IN	Analog	Differential PGA 10 negative input.
AI10P	51	DA10P IN	Analog	Differential PGA 10 positive input.
A032	52	DA32 OUT	Analog	Differential PGA 32 analog output
AI32N	53	DA32N IN	Analog	Differential PGA 32 negative input.
AI32P	54	DA32P IN	Analog	Differential PGA 32 positive input.
A054	55	DA54 OUT	Analog	Differential PGA 54 analog output
AI54N	56	DA54N IN	Analog	Differential PGA 54 negative input.
AI54P	57	DA54P IN	Analog	Differential PGA 54 positive input.
AI6	20	AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AO6	21		Analog	Analog 6 Output
AI7	22	AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AO7	23		Analog	Analog 7 Output
AI8	24	AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AO8	25		Analog	Analog 8 Output
AI9	26	AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.
AO9	27	AMP9/CMP9/PHC9	Analog	Analog 9 Output

9.3 Driver Manager Pin Description

Table 9-3 Driver Manager Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRS3	29	Analog	High-side gate driver source 3.
DRH3	30	Analog	High-side gate driver 3.
DRB3	31	Analog	High-side gate driver bootstrap 3.
DRS4	32	Analog	High-side gate driver source 4.
DRH4	33	Analog	High-side gate driver 4.
DRB4	34	Analog	High-side gate driver bootstrap 4.
DRS5	35	Analog	High-side gate driver source 5.
DRH5	36	Analog	High-side gate driver 5.
DRB5	37	Analog	High-side gate driver bootstrap 5.
DRL0	42	Analog	Low-side gate driver 0.
DRL1	43	Analog	Low-side gate driver 1.
DRL2	44	Analog	Low-side gate driver 2.

9.4 PWM Input Pin Description

Table 9-4 Tri Phase Inverter PWM inputs

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
EN	1	Digital	Tri Phase Inverter Enable
PWMH5	2	Digital	High Side Gate Driver 5 (Half H Bridge 52) PWM Input
PWMH4	3	Digital	High Side Gate Driver 4 (Half H Bridge 41) PWM Input
PWMH3	4	Digital	High Side Gate Driver 3 (Half H Bridge 30) PWM Input
PWML2	5	Digital	Low Side Gate Driver 2 (Half H Bridge 52) PWM Input
PWML1	6	Digital	Low Side Gate Driver 1 (Half H Bridge 41) PWM Input
PWML0	7	Digital	Low Side Gate Driver 0 (Half H Bridge 30) PWM Input

9.5 SPI Input Pin Description

Table 9-5 SPI Communication Port inputs

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SPI_CS	12	Digital	SPI Communications Port Chip Select
SPI_MISO	13	Digital	SPI Communications Port Master Input Slave Output
SPI_MOSI	14	Digital	SPI Communications Port Master Output Slave Input
SPI_CLK	15	Digital	SPI Communications Port Clock

9.6 Miscellaneous Pin Description

Table 9-6 Other Inputs and Outputs

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
nRESET	8	Digital	Reset for external microcontroller reset functionality.
nFAULT	9	Digital	Open Drain fault output
ADC_REF	16	Analog	2.5V or 3.0V ADC reference output
CLK_OUT	17	Digital	Open Drain 125KHz to 1 MHz Clock Output
nSLEEP	18	Digital	Enter Hibernate mode input (asserted low)
nBRAKE	19	Digital	Enter Brake mode (asserted low)

10 Serial Peripheral Interface

The ACT72350 device contains a series of programmable blocks fully configurable through a conventional SPI port. Operating as a Slave SPI peripheral, the ACT72350 SPI port allows the external microcontroller to read and write the internal analog sub system registers.

A typical SPI transaction consists of 16 bits. The first byte forms the seven bit address, with single bit read/write command, and the second byte is the data. Each bit is sampled during the SPI_CLK rising edge.

Figure 10-1 Typical SPI Packet Communication

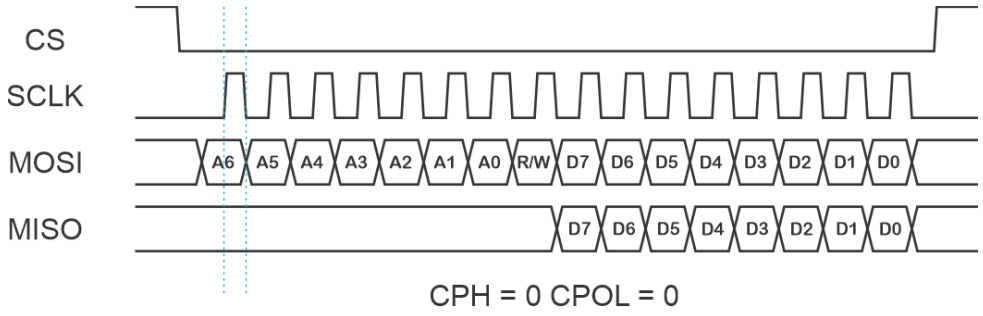
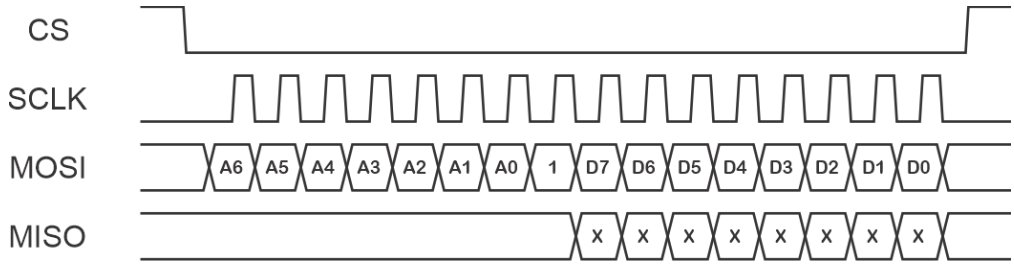
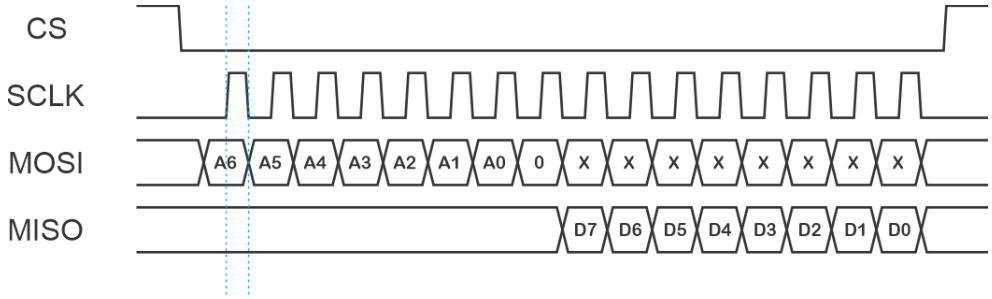


Figure 10-2 SPI Write Command



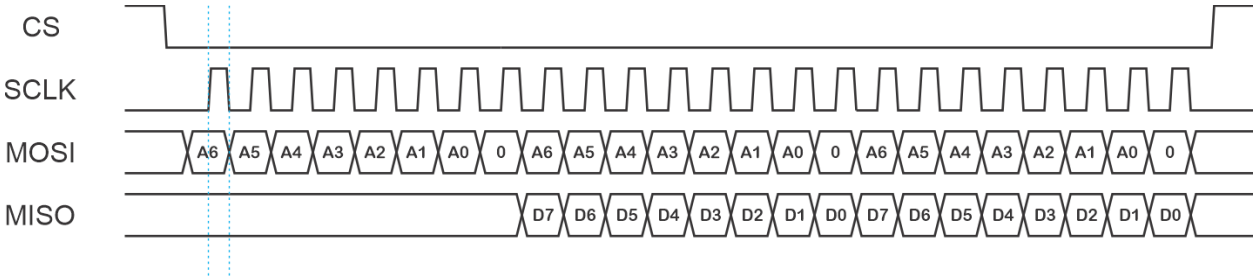
A typical write packet consists of 16 bits of SPI transfer where the first byte contains the 7 bit address shifted one space, followed by the LSB equal to 1 (write command). The second byte then contains the 8 bit data to be written into the addressed register.

Figure 10-3 SPI Read Command



A typical read packet consists of 16 bits of SPI transfer where the first byte contains the 7 bit address shifted one space, followed by the LSB equal to 0 (Read command). The second byte is of no importance as the data will be sent by the slave through the MISO and into the master processor.

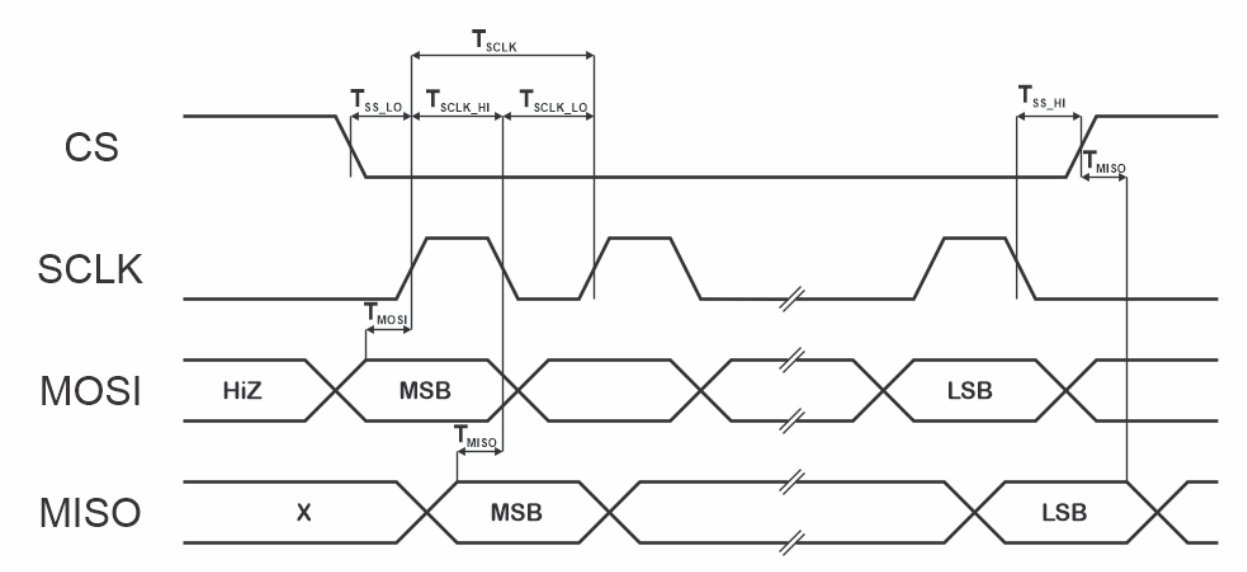
Figure 10-4 SPI Contiguous Packets



In multi byte transactions, the second MOSI byte will contain the subsequent read/write operation and simply consists of nested read/write operations as depicted above.

10.1 Electrical Characteristics

Table 10-1 Serial Peripheral Interface Electrical Characteristics



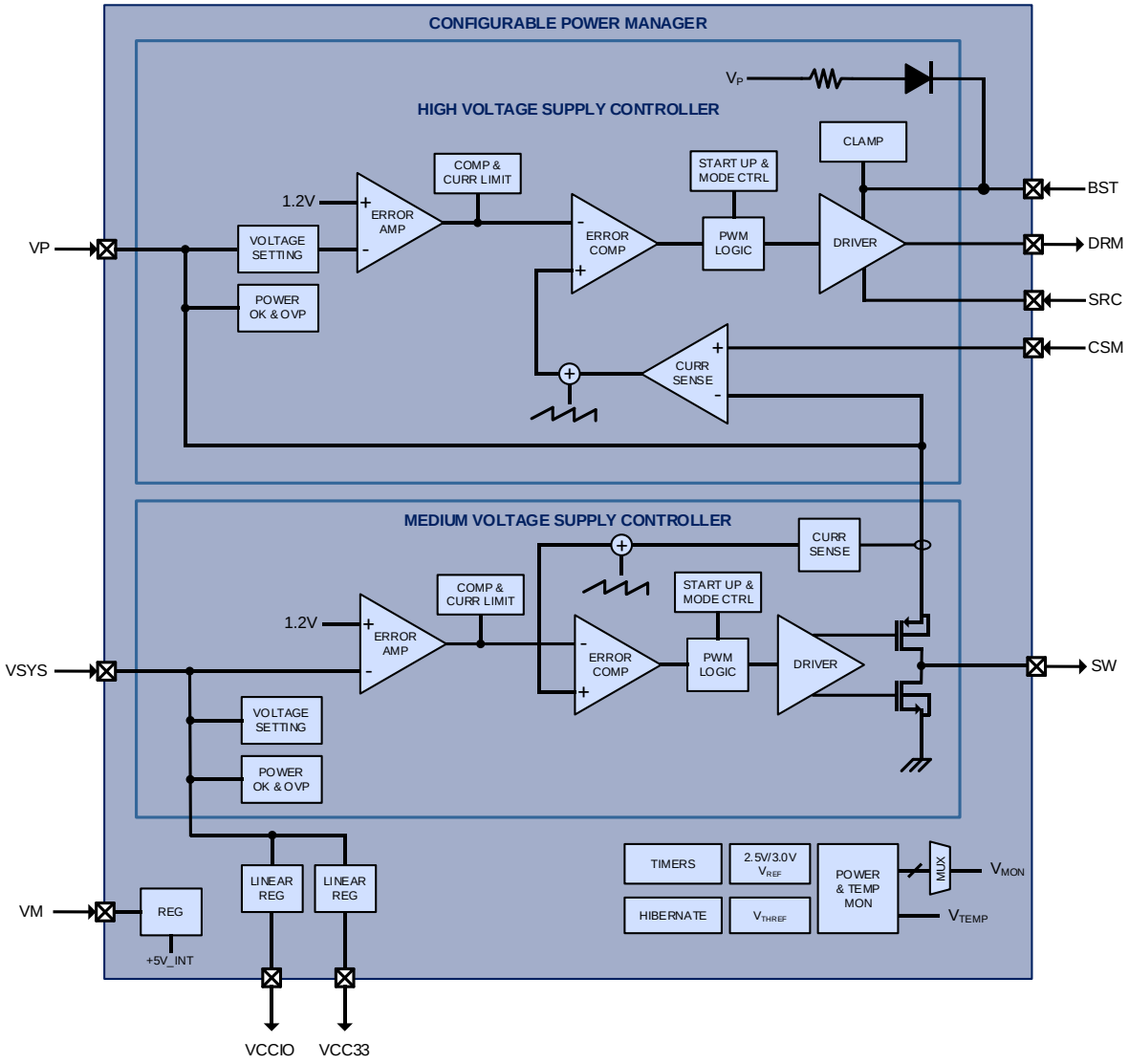
Parameter	Description	Min	Max	Units
T_{SS_LO}	Time between Slave Select falling edge and SCLK rising edge	20		ns
T_{SCLK}	SCLK Period	40		ns
T_{SCLK_HI}	SCLK Signal High Level Time	20		ns
T_{SCLK_LO}	SCLK Signal Low Level Time	20		ns
T_{MISO}	Master Input Slave Output data valid to SCLK falling edge		15	ns
T_{MOSI}	Master Output Slave Input data valid to SCLK rising edge	15		ns
T_{SS_HI}	Time between the last SCLK falling edge and Slave Select rising edge	20		ns

11 CONFIGURABLE POWER MANAGER (CPM)

11.1 Features

- 160V Buck DC/DC Controller (HV Buck)
  - 25V – 160V input
- 5V Switching Regulator (MV Buck)
- 3 linear regulators with power and hibernate management, including V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

Figure 11-1 CPM Block Diagram



11.2 Functional Description

The Configurable Power Manager is optimized to efficiently provide “all-in-one” power management required by the ACT72350 and associated application circuitry. It incorporates a high-voltage power supply controller that is used to convert power from a DC input source to generate a main supply output V_P. There is also an integrated medium-voltage buck DC/DC regulator to generate V_{SYS}.

Two other linear regulators provide V_{CCIO} and V_{CC33} supplies for 3.3V I/O and 3.3V mixed signal. The power manager also handles system functions including internal reference generation, wakeup timer, hibernate mode management, and power and temperature monitoring.

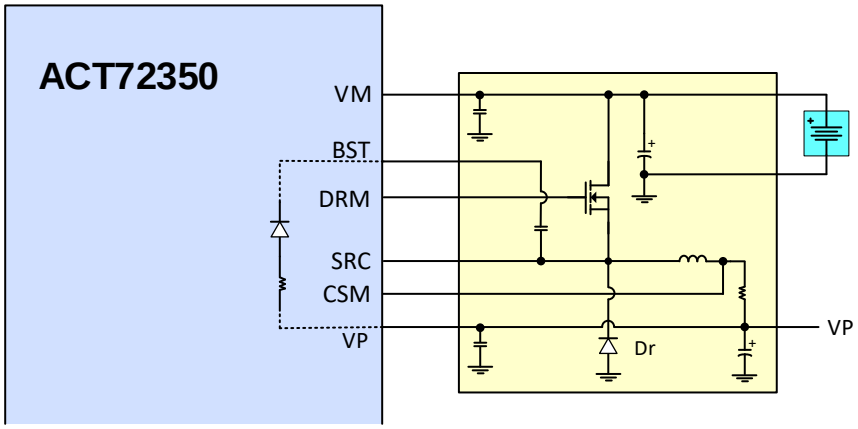
11.3 High-Voltage Supply Controller (HV-BUCK)

The ACT72350 contains a High-Voltage Supply Controller for a Buck DC/DC. This power supply is used to supply the various regulators in the ACT72350, as generating the V_P gate drive voltage for the Application Specific Driver Manager (ASPD).

The HV-BUCK controller drives an external power MOSFET for pulse-width modulation switching of an inductor or transformer for power conversion. The VM is the HV-BUCK supply controller input. The DRM output drives the gate of the N-CH MOSFET between the V_M on state and V_{SS} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The gate of the high-side power MOSFET is connected to the DRM pin and the source of the high-side power MOSFET is connected to SRC.

The V_P regulation voltage is initially set to 15V during start up, and can be reconfigured to be 12V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.2V.

Figure 11-2 HV-BUCK Example



The switching frequency and output voltage of the HV-BUCK can be reconfigured by the application MCU through the SPI port. The switching frequency can be configured to be between 50kHz and 400kHz and

the gate drive output voltage can be configured to either 12V or 15V to work for a range of MOSFET or IGBT based inverters.

The Rectifier Diode (Dr) must be a low QRR diode.

11.3.1 HV-BUCK Configuration

To configure the HV-BUCK's output voltage to either 12V or 15V, write to the **SOC.SYSCONF.VPSET**. To set the HV-BUCK's frequency write to the **SOC.SYSCONF.HVBK_FREQ.**

11.3.2 HV-BUCK Re-start Handling

The HV-BUCK has a safety re-start mechanism that protects the device and external components in case of a DC/DC failure. This mechanism samples VM and VP when the MV-BUCK is re-started and may insert a delay before it allows the power supply to be re-started, in case of some type of short or damage with the power supply components on the PCB.

The re-start handling operates as described below.

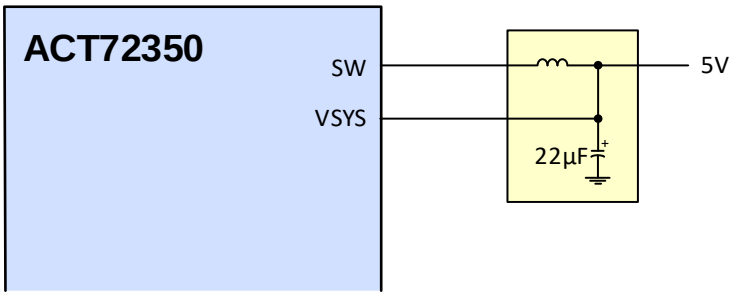
In ACT72350, if the DC/DC has been disabled due to VM falling below $V_{UVLOF;VM}$, VM is sampled and as soon as VM > $V_{UVLOR;VM}$, then the DC/DC will re-start. If VM is > VM UVLO falling ($V_{UVLOF;VM}$) but VP < VP UVLO falling ($V_{UVLOF;VP}$) then the DC/DC is disabled and a 350ms delay is inserted. After this delay, the DC/DC is re-started.

11.4 Medium-Voltage Buck Regulator (MV-BUCK)

The ACT72350 contains a Medium-Voltage Buck Switching Regulator that generates a 5V, 200mA supply for the device, as well as PCB functions.

The SW pin is the switch node of the Buck regulator. The Power MOSFET is integrated, so connect this pin to VSYS through an external inductor. The VSYS pin is the 5V regulator output, which should be bypassed to ground.

Figure 11-3 MV-BUCK Switching Regulator Example

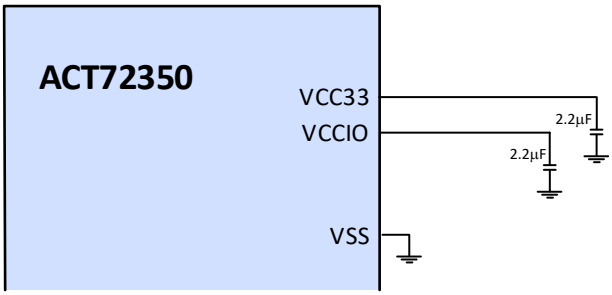


The output of VSYS is fixed at 5V and the switching frequency is 1.33MHz. This regulator supplies at least 200mA. This buck regulator offers better thermal and efficiency performance.

11.5 Linear Regulators

The CPM includes two additional linear regulators, supplied by the VSYS medium voltage regulator. Once VSYS is above 4.5V, the linear regulators for VCCIO and VCC33 supplies, sequentially power up.

Figure 11-4 Linear Regulators Example

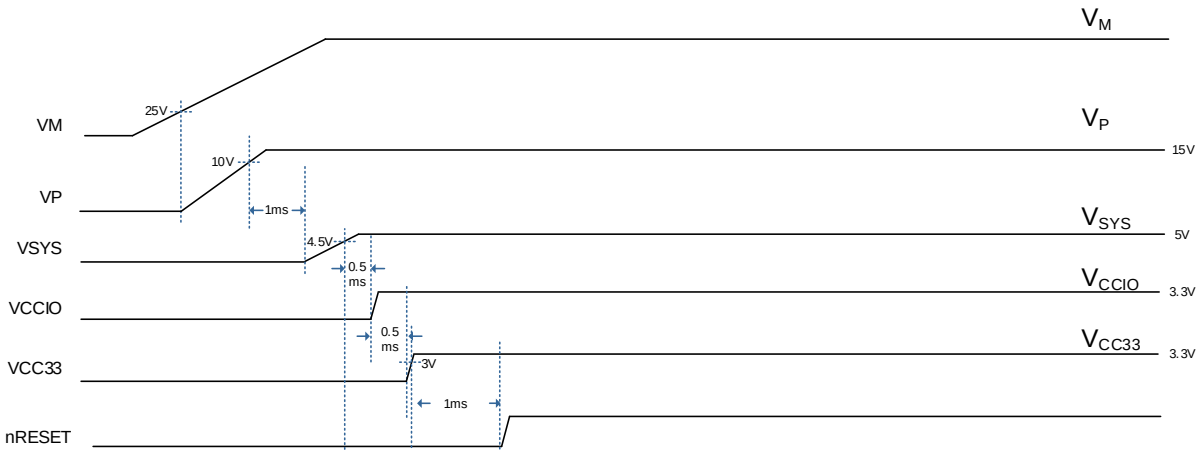


The figure above shows typical circuit connections for the linear regulators. The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 regulator generates 3.3V. When VSYS and the LDOs above are all above their respective power good thresholds, and the configurable power on reset duration has expired, the nRESET signal is released from reset state.

11.6 Power-up Sequence

The CPM follows a typical power up sequence as shown in Figure 11-5 below.

Figure 11-5 Power-Up Sequence



A typical sequence begins with motor power supply (VM) being applied and rising to 25V. When VM rises to 25V, the HV-BUCK controller is started and VP starts to rise. When VP rises over the UVLO rising threshold, then there is a 1ms delay and then the MV-BUCK is enabled. When VSYS rises to 4.5V, then there is a 0.5ms delay and the VCCIO LDO is enabled. Then there is a 0.5ms delay and the VCC33 LDO is enabled.

There is then a 0.5ms delay and the power good threshold of all LDOs is checked. If all are OK, then there is an additional 1ms delay, then the POR signal is asserted, and the nRESET signal is released so the application MCU can begin executing firmware.

During the firmware initialization process, the application MCU may change the VP output voltage setting from the default value of 15V to 12V.

11.7 Hibernate Mode

The IC can go into an ultra-low power hibernate mode by asserting the nSLEEP signal. In hibernate mode, only a minimal amount (typically 19µA at 56V) of current is used by V_M, and the CPM controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the application microcontroller can be reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

To enable the push button feature, write to the **SOC.MISC.PBEN** bit.

11.8 Standby Mode

The IC can go into an intermediary low power mode by writing to the STBY bit to allow the system to preserve power, while remaining powered, allowing the application to exit sleep mode much faster than what can be achieved with the Hibernade mode. In Stand By mode, the DC/DC converter and VSYS are allowed to remain oeprating, while the VCCIO and VCC33 regulators are disabled. The system exits Stand By mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the Stand By mode, the power manager goes through the start up cycle for the two disabled LDO's and the application microcontroller can be reinitialized. All internal registers content is retained during Stand By mode.

To enter Stand By mode, write to the **SOC.WATCHDOG.STDBY** bit.

11.9 Power and Temperature Monitor

Whenever any of the V_P, V_{SYS}, V_{CCIO} or V_{CC33} power supplies falls below their respective power good threshold voltage, a fault event is detected and the nRESET signal is asserted (application microcontroller is reset). The application microcontroller stays in the reset state until V_{SYS}, V_{CCIO} and V_{CC33} supply rails are all good again and the POR time has expired. Faults are logged within the SOC.FAULT register and can be sampled as follows:

- V_P FAULT: Read **SOC.FAULT.VPFLT** bit
- V_{SYS} FAULT: Read **SOC.FAULT.VSYSFLT** bit
- V_{CCIO} FAULT: Read **SOC.FAULT.VCCIOFLT** bit
- V_{CC33} FAULT: Read **SOC.FAULT.VCC33PFLT** bit

An nRESET assertion can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 165°C. The fault status bits are persistent during reset, and can be read by the

microcontroller upon re-initialization to determine the cause of previous reset. This information is stored within the **SOC.FAULT.TMPFLT** bit

A power monitoring signal V_{MON} is provided onto the AIO6 buffered output for monitoring various internal power supplies. V_{MON} can be set to be one of the following monitored supplies: 0.4•V_{CC33}, 0.4•V_{CCIO}, 0.4•V_{SYS}, VPTAT[1] or 0.1•V_P.

For power and temperature warning, an IC temperature warning event at 140°C are provided as a maskable interrupt source into the application microcontroller, through the nFAULT output. This warning could be employed to instruct the microcontroller to safely power down the system.

To allow Temperature Warning assertions on the nFAULT open drain output, write to the **SOC.FAULTENABLE.nTMPWARN** bit. Alternatively, the external microcontroller can obtain the real time status temperature warning bit by reading the **SOC.FAULT.TMPWARN** bit. If the Temperature Warning fault issues a fault message, the state of this fault is latched within the **SOC.FAULT.TMPWARN_LATCH**.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal is provided onto the AIO6 buffered output as an analog signal, which the application microcontroller can choose to capture using its ADC resource, as a means to measure internal die temperature.

11.10 Voltage Reference

The reference block includes a 1.2V high-precision reference voltage used internally and for all the LDOs. There is also a high-accuracy 2.5V/3.0V programmable reference for the ADC V_{REF}. There is also a 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V) .

[1] VPTAT is voltage proportional with absolute temperature from the temperature sensing circuit. The VPTAT voltage can be sampled by the external microcontroller's ADC through the voltage monitoring MUX at AO6, while AIO6 is in Output Buffer Mode.

11.11 Electrical Characteristics

Table 11-1 High-Voltage Buck Controller Electrical Characteristics

(V_M = 30V, V_P = 12V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{HIB;VM}$	V_M hibernate mode supply current	Hibernate mode, VM = 56V		19	26	μA
		Hibernate mode, VM = 80V		22.5		μA
$V_{UVLOR;VM}$	V_M UVLO rising		23	25	27	V
$V_{UVLOF;VM}$	V_M UVLO hysteresis			8		V
$V_{REF;VP}$	V_P output regulation voltage	Set to 15V (default)	-5%	12	-5%	V
$k_{POKR;VP}$	V_P power OK threshold	V_P rising		91		%
$k_{POKF;VP}$		V_P falling		87		%
$k_{OVPR;VP}$	V_P OV protection threshold	V_P rising, blanking = 10□s		130		%
$t_{ONMIN;DRM}$	DRM minimum on time		90	200	300	ns
$t_{OFFMIN;DRM}$	DRM minimum off time		390	600	1150	ns
$V_{UVLOR;VP}$	V_P UVLO rising			10		V
$V_{UVLOF;VP}$	V_P UVLO falling			8		V
$V_{CSM;ILIM}$	CSM current limit threshold		-12%	0.2	12%	V
$F_{S;DRM}$	Switching frequency	Frequency setting: 50kHz, 100kHz, 200kHz (default), 400kHz	-5		5	%
$I_{SOURCE;DRM}$	DRM output high source current			200		mA
$I_{SINK;DRM}$	DRM output low sink current			500		mA
	HV-BUCK inductor value			100		□H
I_{DSG}	Discharge current			10		mA
V_{VM}	Motor voltage range		0		160	V
$V_{SRC;VM}$	SRC to VM range				10	V
$V_{BST;VSS}$	BST to ground range				175	V

Table 11-2 Medium-Voltage Buck Controller Electrical Characteristics

(V_M = 30V, V_P = 12V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSYS}	V_{SYS} output voltage accuracy		-3%	5	3%	V
F_{SW}	Switching frequency		-5%	1.33	5%	MHz
$I_{VSYS;LIM}$	V_{SYS} peak current limit, cycle by cycle	L = 10 uH	465	550	710	mA
I_{VSYS}	V_{SYS} output current	V_{SYS} > 3V	200			mA
		V_{SYS} < 2.5V	100			mA
$V_{POK;VSYS}$	V_{SYS} power OK threshold	Rising	4.25	4.5	4.75	V
		Falling		4.2		V
	V_{SYS} power OK blanking delay			10		µs
	MV-BUCK inductor value	Current rating of at least 750mA	6.8 – 20%		10 + 20%	µH
$V_{UVLO;VSYS}$	V_{SYS} UVLO	Rising		4.5		V
		Falling		4.2		V
$V_{OVP;VSYS}$	V_{SYS} OVP	Rising		5.5		V
		Falling		5.2		V

Table 11-3 Linear Regulators Electrical Characteristics

(V_P = 12V and T_A = -40°C to 125°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCIO}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CC33}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
$I_{LIM;VCCIO}$	V_{CCIO} current limit		140	160		mA
$I_{LIM;VCC33}$	V_{CC33} current limit		40	65		mA
$I_{LIM;FOLDBACK}$	LDO current fold back	V_{CCIO}, V_{CC33}		50		%
$t_{POK;BLANK}$	Power OK blanking delay[2]	V_{CCIO}, V_{CC33}		10		µs
R_{DISCH}	Output discharge resistance	LDO off		300		Ohm
C_{VCCIO}	VCCIO stable output capacitance		1		4.7	µF
C_{VCC33}	VCC33 stable output capacitance		1		4.7	µF
$V_{LDO;POK}$	LDO power OK rising threshold	Hysteresis = 10%	85	90	95	%
$V_{LDO;OV}$	LDO Over voltage protection rising threshold	Hysteresis = 6%[1]	112	115	118	%

[1] Guaranteed by Design (ATE)

[2] Guaranteed by Design

Table 11-4 ADC REF Output (ADC_REF) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	Ta = 25°C	-0.5%	2.5	0.5%	V
		Ta = −40°C to Ta = 125°C	-0.9%	2.5	0.9%	V
$VREF_{C\_LOAD}$	Capacitive Load				10	pf

11.12 Typical Performance Characteristics

(T_A = 25ºC unless otherwise specified)

Figure 11-6 VDDIO LDO Voltage vs. Current

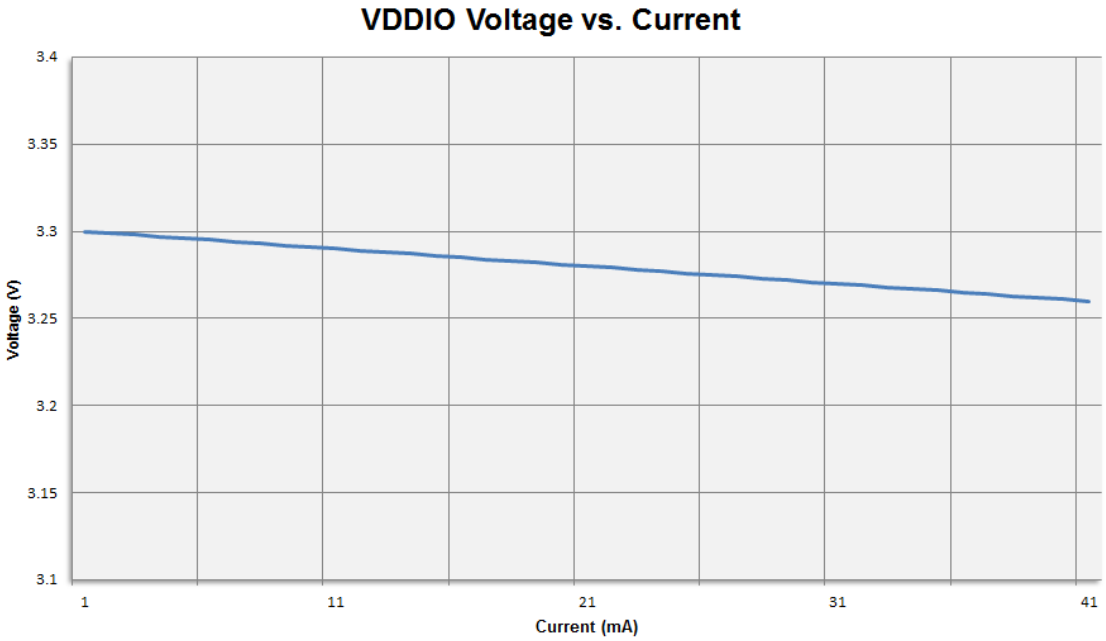
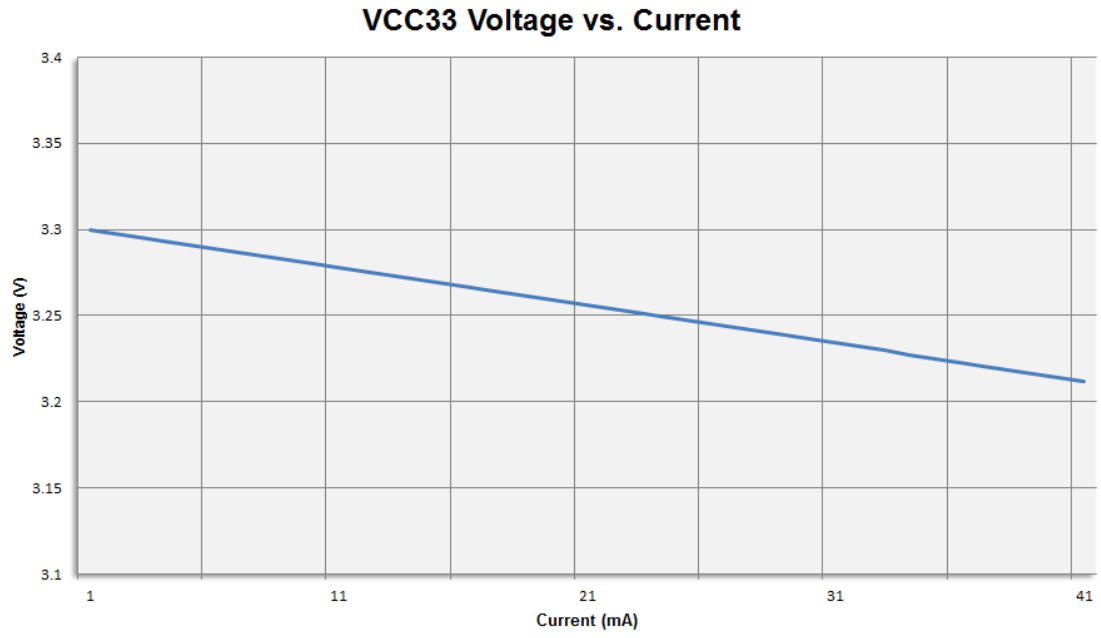


Figure 11-7 VCC33 LDO Voltage vs. Current



11.13 Register Summary

Table 11-5 CPM Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
00h	**SOC.FAULT**	Fault condition indication register	00h
01h	**SOC.STATUS**	Hardware status condition register	00h
02h	**SOC.MISC**	Miscellaneous features register	00h
03h	**SOC.PWRCTL**	Power control register	00h
04h	**SOC.FAULTENABLE**	Power Manager fault mask register	00h
05h	**SOC.WATCHDOG**	SOC Watchdog configuration register	00h
2Bh	**SOC.SYSCONF**	Power Manager system configuration register	0Ch
7Eh	**SOC.WDTPASS**	SOC Watchdog Timer Password	00h

11.14 Register Detail

11.14.1 SOC.FAULT

Register 11-1 SOC.FAULT (Fault Condition, 00h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**TMPWARN_RTS**	R	0x0	Real-time temperature warning status. When the temperature is greater than the warning threshold, this bit is set to 1b. When the temperature less than the warning threshold, this bit is set to 0b. 0b: No temperature warning 1b: Temperature warning
6	**TMPWARN_LATCH**	R	0x0	Latched temperature warning status. If the temperature reaches the warning threshold and the **SOC.FAULTENABLE.nTMPWARN** is not masked, this bit is set and nIRQ1 is asserted. Write 1b to clear when not masked. 0b: No temperature warning 1b: Temperature warning
5	**TMPFLT**	R	0x0	Temperature fault status. If the temperature reaches the fault threshold, this bit is set to 1b. Write 1b to clear. 0b: No temperature fault 1b: Temperature fault
4	**VPFLT**	R	0x0	DC/DC fault when VP is below UVLO or over-voltage. Set on fault, and cleared when written to 1b. 0b: No VP fault 1b: VP fault
3	**VSYSFLT**	R	0x0	VSYS fault when VSYS is below UVLO or over-voltage. Set on fault, and cleared when written to 1b. 0b: No VSYS fault 1b: VSYS fault
2	**VCCIOFLT**	R	0x0	VCCIO fault. Set on fault, and cleared when written to 1b. 0b: No VCCIO fault 1b: VCCIO fault
1	**VCC33FLT**	R	0x0	VCC33 fault. Set on fault, and cleared when written to 1b. 0b: No VCC33 fault 1b: VCC33 fault
0	**RFU**	R	0x0	Reserved, write as 0.

11.14.2 SOC.STATUS

Register 11-2 SOC.STATUS (System Status, 01h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HWRSTAT**	R	0x0	Hardware Reset Status. Bit is set on hardware reset and is cleared when written to 1b. 0b: No hardware reset 1b: Hardware reset
6	**SRSTSTAT**	R	0x0	Soft Reset Event. Bit is set on software reset event and is cleared when written to 1b. 0b: No software reset 1b: Software reset
5	**WDTRSTAT**	R	0x0	Watchdog Timer Reset Status. When enabled, this bit is set on Watchdog Timer Reset and cleared when written to 1b. 0b: No WDT reset 1b: WDT Reset
4	**VM24LOW_LATCH**	R	0x0	VM Low Status. Bit is set on hardware reset and is cleared when written to 1b. 0b: No VM low 1b: VM low
3	**VPLOW_RTS**	R	0x0	Real-time VP Low Status. 0b: No VP low 1b: VP low
2	**VPLOW_LATCH**	R	0x0	Latched VP Low Status. During VP low condition, this bit is set and the nIRQ signal is asserted. To clear this bit, write to 1b. 0b: No latched VP low 1b: Latched VP low
1	**PBSTAT_RTS**	R	0x0	Real-time Push-button Status. 0b: Push-button not active 1b: push-button active
0	**PBSTAT_LATCH**	R	0x0	Latched Push-button Status. This bit is set in normal operation as long as the push button is enabled and on for more than the deglitch time, if not masked. When this bit is set, it will assert the nIRQ signal. 0b: Latched push-button not active 1b: Latched push-button active

11.14.3 SOC.MISC

Register 11-3 SOC.MISC (SOC Miscellaneous Configuration, 02h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R/W	0x0	Reserved, write as 0.
6	**PBEN**	R/W	0x0	AIO6 Push-button Enable. 0b: Push-button not enabled 1b: Push-button enabled
5	**VREFSET**	R/W	0x0	ADC Reference Voltage Setting. 0b: 2.5V 1b: 3.3V
4	**CLKOUTEN**	R/W	0x0	Clock Output (CLK_OUT) enable. 0b: Not enabled 1b: Enabled
3	**MCUALIVE**	R/W	0x0	MCU Alive. Set by the MCU to indicate that it is alive. Before this bit is set, ignore all MCU commands (EMUX, gate driver) except SPI register commands. This bit will automatically be cleared when the reset signal to the MCU is asserted. 0b: MCU not alive 1b: MCU alive
2	**TPBD**	R/W	0x0	Push-button deglitch time: 0b: 32ms 1b: 1ms
1	**RFU**	R	0x0	Reserved, write as 0.
0	**SMEN**	R/W	0x0	Signal Manager Enable. This bit is automatically cleared when the reset signal to the MCU is asserted. 0b: Not enabled 1b: Enabled

11.14.4 SOC.PWRCTL

Register 11-4 SOC.PWRCTL (Power Control, 03h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**CLKOUTFREQ**	R/W	0x0	Low-Speed Clock Output Frequency Setting (CLKOUT). 00b: 125kHz 01b: 250kHz 10b: 500KHz 11b: 1 MHz
5	**STDBY**	R/W	0x0	Stand By Mode Enable. This bit is self clearing. 0b: No Stand By Mode (normal LDO operation) ..1b: Enter Stand By Mode (Disables LDO's)
4	**VMSNSEN**	R/W	0x0	VM Sense Enable. 0b: VM Sense Disabled ..1b: VM Sense Enabled
4:0	**WUTIMER**	R/W	0x0	Wake Up Timer Interval: 0000b = infinite 0001b = 1ms 0010b = 5ms 0011b = 10ms 0100b = 25ms 0101b = 50ms 0110b = 100ms 0111b = 125ms 1000b = 250m 1001b = 500ms 1010b = 750ms 1011b = 1s 1100b = 2s 1101b = 4s 1110b = 6s 1111b = 8s

11.14.5 SOC.FAULTENABLE

Register 11-5 SOC.FAULTENABLE (Fault enable, 04h)

BIT	NAME	ACCESS[2]	RESET	DESCRIPTION
7	**nVM24FLTEN**	R/W	0x0	VM Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)
6	**nTMPWARNEN**	R/W	0x0	Temperature Warning Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)
5	**nVPFLTEN**	R/W	0x0	VP Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)
4	**nVSYSFLTEN**	R/W	0x0	VSYS Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)
3	**RFU**	R/W	0x0	Reserved, write as 0.
2	**nLDOFLTEN**	R/W	0x0	LDO Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)
1	**nPBINTEN**	R/W	0x0	Push-button Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)
0	**nVPINTEN**	R/W	0x0	VP Low Fault Enable 0b: Disabled 1b: Fault Enabled (Asserts nFAULT)

[2] This byte is unlocked for writing when **UNLOCK** = 1b.

11.14.6 SOC.WATCHDOG

Register 11-6 SOC.WATCHDOG (SOC Watchdog Configuration, 05h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**SRST**	R/W	0x0	Soft Reset. This bit can be set to issue a system soft reset. This bit is always read as 0b. When set, the STATUS.SRST bit will be latched to a 1b so the MCU knows the system is being started after a soft reset. 0b: Do not issue soft reset 1b: Issue soft reset
6:4	**RFU**	R	0x0	Reserved, write as 0.
3	**WDTEN**	R/W	0x0	Watchdog Timer Enable. Cleared during hard reset. 0b: disabled 1b: enabled
2:0	**TWD**	R/W	0x0	Watch-dog Timer. 000b: 62.5ms 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

11.14.7 SOC.SYSCONF

Register 11-7 SOC.SYSCONF (System Configuration, 2Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**RFU**	R	0x0	Reserved, write as 0.
3	**VPSET**	R/W	0x1	VP Setting. 0b: 12V 1b: 15V
2:1	**HVBK_FREQ**	R/W	0x2	High-Voltage Buck Switching Frequency Setting. 00b: 50kHz 01b: 100kHz 10b: 200kHz 11b: 400kHz
0	**DIS_PD**	R/W	0x01	Disable VP Pull Down 0b: Enable VP Pull Down 1b: Disable VP Pull Down

11.14.8 SOC.WDTPASS

Register 11-8 SOC.WDTPASS (WDT Password, 7Eh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**WDTPASS**	RW	0000 0000b	To reset the SOC Watchdog Timer, write this field to ACh.

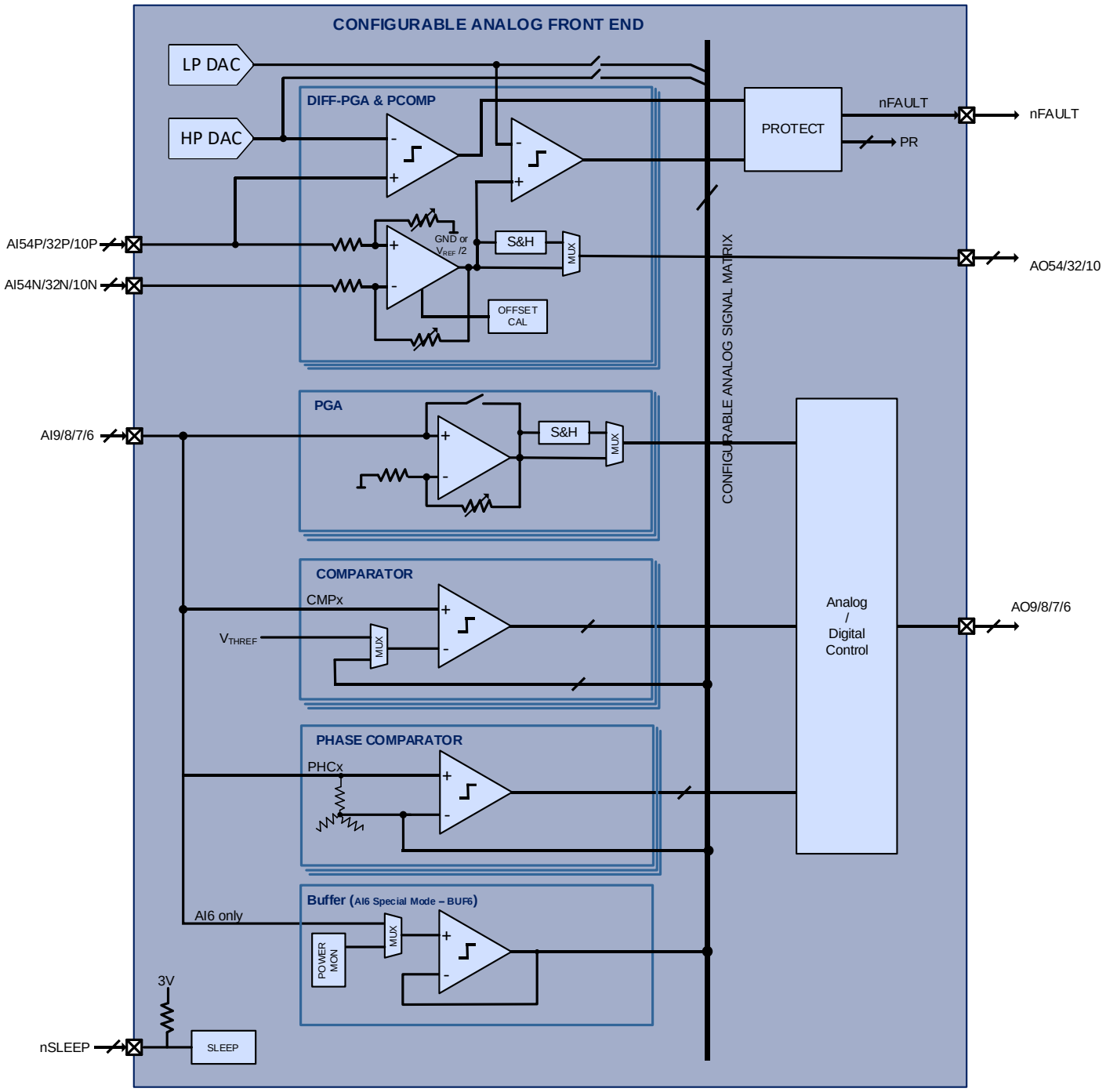
12 CONFIGURABLE ANALOG FRONT END (CAFE)

12.1 Features

- 10 Configurable Analog I/O signals
  - Gain mode, comparator mode, special mode
- 3 High-Performance, Configurable Differential Amplifiers
- 4 High-Performance, Configurable Single-Ended Amplifiers
- Two high-speed comparators with protection functions
- Phase to phase, phase to center-tap modes
- Bi-directional, asymmetric configurable comparator hysteresis
- Push-button input for exiting hibernate mode

12.2 Block Diagram

Figure 12-1 Configurable Analog Front End



12.3 Introduction

The device includes a Configurable Analog Front End (CAFE, Figure 12-1) accessible through 10 analog input and 7 analog output pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, and one buffer output. A push button function is provided for optional push button on Hibernate and Stand By modes.

12.4 Differential Programmable Gain Amplifier (DA)

The DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly as a live analog output, or through a sample-and-hold circuit synchronized with the external ADC sampling engine. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 13.5k / (13.5k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

12.5 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SS}. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed into its independent output for easy access into the application's microcontroller analog inputs.

12.6 General Purpose Comparator (CMP)

The general purpose comparator takes the CMPx input and compares it to the programmable threshold voltage (V_{THREF}). The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed into its respective output.

12.7 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (V_{THREF}) or a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection.

The phase comparator signals can also be configured to the other two phase comparators (between AIO7, AIO8 and AIO9), to perform phase to phase comparisons.

The comparator blanking time is configurable. The blanking time configuration supports bi-directional and asymmetric configurations, which enables hysteresis for rising and falling signals.

The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

12.8 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The HP comparator compares the amplifier output to the 10-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to assert the nFAULT output. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR. These two protection events can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

12.9 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the BUF6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

12.10 Analog Front End I/O (AIO)

The ACT72350 has 10 AIx pins and 7 AOx pins that are available as digital IO resource. In the analog front end I/O mode, the aforementioned pins can be configured to be a digital input (AIx pins) or digital open-drain output (AOx pins).

The AIx inputs signal logical state can be sampled from the SOC.DINSIG0 and DINSIG1 registers. Input changes (rising edge or falling edge) on AI[9:6] can be logged within the SOC.SIGINTF register. Rising or falling edge logging can be selected on a per digital input on AI[9:6] at the SOC.SIGINTM register.

The digital output signal logical state can be set to active high (default) or active low, with pull up to VSYS supply rail. Digital output state can be set within the SOC.DOUTSIG register.

12.11 Push Button (PBTN)

The push button PBTN, when enabled, can be used by the MCU to detect a user active-low push button event and to put the system into an ultra-low-power hibernate mode. Once the system is in hibernate mode, PBTN can be used to wake up the system.

In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 8s during normal operation. The PBTN input is active low and has a 55kΩ pull-up resistor to 3V.

12.12 HP DAC and LP DAC

The 10-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators, or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators, or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

12.13 Cycle-by-cycle Current Limit

The ACT72350 contains hardware support for cycle by cycle current limit. The user may configure this feature to use the LPCOMP DAC as the current threshold. The CAFE will automatically perform duty cycle truncation to lower current at any time the associated phase current is greater than the setting of the LPCOMP DAC.

12.14 Temperature Protection

The ACT72350 contains an internal temperature sensor that detects temperature warnings and faults.

When the device temperature reaches the temperature warning threshold (140ºC), the device sets an over-temperature warning condition. The user may configure a mask-able interrupt the MCU for this condition, through the nFAULT output.

When the device temperature reaches the temperature fault threshold (165 ºC), the device is shut down. This condition will always assert the nFAULT output.

For more details on the register settings for over-temperature protection see the ACT72350 User Guide and related application notes.

12.15 Electrical Characteristics

Table 12-1 Differential Programmable Gain Amplifier (DA) Electrical Characteristics (AIO<5:0>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;DA}$	Input common mode range		-0.3		2.5	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	V
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150		µA
$V_{OS;DA}$	Input offset voltage	Gain = 8x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio		50	80		dB
	Slew rate	Gain = 8x, V_{DAxP} – V_{DAxN} = 0V to 0.2V, T_A = 25 °C		7		V/µs
$R_{INDIF;DA}$	Differential input impedance			27		kΩ
$t_{ST;DA}$	Settling time	To 1% of final value		500		ns
C_{OUT}	Maximum Output Capacitance	External capacitance			30	pF
I_{max}	Maximum load current	V_{OUT}=1V, T_A = 25°C		1		mA
$A_{VZI;DA}$	Differential amplifier gain (zero ohm source impedance)	Gain = 1x	-2	1	2	%
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{DAxP}-V_{DAxN}=125mV, T_A = 25°C		8		
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		

Table 12-2 Single-Ended Programmable Gain Amplifier (AMP) Electrical Characteristics (AIO<9:6>)

(V_{SYS} = 5V, V_{CCIO} = 3.3V and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;AMP}$	Input common mode range		0		V_{SYS}	V
$V_{OLR;AMP}$	Output linear range		0.1		V_{SYS} – 0.1	V
$I_{CC;AMP}$	Operating supply current	Each enabled amplifier		80	120	µA
$V_{OS;AMP}$	Input offset voltage	Gain = 8x	-10		10	mV
	Slew rate	Gain = 1x		10		V/µs
$t_{ST;AMP}$	Settling time	To 1% of final value		400		ns
C_{OUT}	Maximum Output Capacitance	External capacitance			30	pF
I_{max}	Maximum load curent	V_{OUT}=1V, T_A = 25°C		1		mA
$A_{V;AMP}$	Amplifier gain	Gain = 1x	-2	1	2	%
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{AMPx}=125mV, T_A = 25°C		8		
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		

Table 12-3 General Purpose Comparator (CMP) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;CMP}$	Input common mode range		0		V_{SYS}	V
$I_{CC;CMP}$	Operating supply current	Each enabled comparator		35		µA
$V_{OS;CMP}$	Input offset voltage[2]		-10		10	mV
$V_{HYS;CMP}$	Hysteresis			22		mV
$t_{DEL;CMP}$	Comparator delay				1	µs
$t_{DELMODE;CMP}$	Mode change blanking delay[2]			5		µs

Table 12-4 Phase Comparator (PHC) Electrical Characteristics (AIO<9:6>)

(V_{SYS} = 5V, V_{CC33} = 3.3V and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;PHC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;PHC}$	Operating supply current[3]	Each enabled comparator		35		µA
$V_{OS;PHC}$	Input offset voltage[3]		-10		10	mV
$V_{HYS;PHC}$	Comparator Hysteresis, HYSMODE = 0	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (6mV)	4	6	8	mV
		AIO<9:7>HYS = 10b (12mV)	9	12	15	mV
		AIO<9:7>HYS = 11b (24mV)	18	24	30	mV
	Comparator Hysteresis, HYSMODE = 1	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (24mV)	18	24	30	mV
		AIO<9:7>HYS = 10b (48mV)	36	48	60	mV
		AIO<9:7>HYS = 11b (96mV)	72	96	120	mV
$t_{DEL;PHC}$	Comparator delay	10mV difference input			1	µs

Table 12-5 Special Mode Electrical Characteristics (AIO<9:7>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC}$	Operating supply current[4]	Each enabled comparator		35		µA
$V_{HSYS;SPEC}$	Comparator Hysteresis, HYSMODE = 0	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (6mV)	4	6	8	mV
		AIO<9:7>HYS = 10b (12mV)	9	12	15	mV
		AIO<9:7>HYS = 11b (24mV)	18	24	30	mV
	Comparator Hysteresis, HYSMODE = 1	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (24mV)	18	24	30	mV
		AIO<9:7>HYS = 10b (48mV)	36	48	60	mV
		AIO<9:7>HYS = 11b (96mV)	72	96	120	mV

Table 12-6 Special Mode Electrical Characteristics (AIO6)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		3.6	V
$I_{CC;SPEC6}$	Operating supply current			60		µA
$V_{INOFF;SPEC6}$	Input offset voltage		-20		20	mV
$I_{OUT;SPEC6}$	Output current			2		mA

Table 12-7 Analog Front End (AI/AO) Electrical Characteristics (AI/AO<9:0>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage		2.2			V
$V_{IL;AIO}$	Low-level input voltage				0.8	V
$R_{PD;AIO}$	Pull-down resistance	Input mode		1		MΩ
$V_{OL;AIO}$	Low-level output voltage	I_{AIOx}=7mA, open-drain output mode			0.3	V
$I_{OL;AIO}$	Low-level output sink current	V_{AIOx} = 0.4V, open-drain output mode	6	14		mA
$I_{LK;AIO}$	High-level output leakage current	V_{AIOx} = 5V, open-drain output mode		0	10	µA

Table 12-8 Push Button (PBTN) Electrical Characteristics (AIO6)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2.2			V
$V_{IL;PBTN}$	Low-level input voltage				0.8	V
$R_{PU;PBTN}$	Pull-up resistance	To 3V, push-button input mode		50		kΩ

Table 12-9 nSLEEP Input (nSLEEP) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{nSLEEP}	nSLEEP pin voltage range		0		5	V
V_{IH_nSLEEP}	High-Level input voltage		2.3			V
V_{IL_nSLEEP}	Low-level input voltage				0.8	V
R_{PU_nSLEEP}	nSLEEP pull up resistance			50		KOhms

Table 12-10 HP DAC and LP DAC Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DACREF}	DAC reference voltage	TA = 25°C	-0.5%	2.5	0.5%	V
		TA = -40°C to 125°C	-0.9%	2.5	0.9%	
	HP 10-bit DAC INL		-2.5		2.5	LSB
	HP 10-bit DAC DNL		-2.5		2.5	LSB
	LP 10-bit DAC INL		-2.5		2.5	LSB
	LP 10-bit DAC DNL		-2.5		2.5	LSB

Table 12-11 Temperature Protection

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{WARN}	Temperature warning threshold			140		°C
$T_{WARN;HYS}$	Temperature warning hysteresis			15		°C
$T_{WARN;BLANK}$	Temperature warning blanking			50		µs
T_{FAULT}	Temperature fault threshold			165		°C
$T_{FAULT;HYS}$	Temperature fault hysteresis			15		°C
$T_{FAULT;BLANK}$	Temperature fault blanking			50		µs

12.16 Register Summary

Table 12-12 CAFE Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
0x06	**SOC.CFGAIO0**	AIO0 Configuration	0x00
0x07	**SOC.CFGAIO1**	AIO1 Configuration	0x00
0x08	**SOC.CFGAIO2**	AIO2 Configuration	0x00
0x09	**SOC.CFGAIO3**	AIO3 Configuration	0x00
0x0A	**SOC.CFGAIO4**	AIO4 Configuration	0x00
0x0B	**SOC.CFGAIO5**	AIO5 Configuration	0x00
0x0C	**SOC.CFGAIO6**	AIO6 Configuration	0x00
0x0D	**SOC.CFGAIO7**	AIO7 Configuration	0x00
0x0E	**SOC.CFGAIO8**	AIO8 Configuration	0x00
0x0F	**SOC.CFGAIO9**	AIO9 Configuration	0x00
0x10	**SOC.SIGSET**	Signal manager Configuration	0x00
0x11	**SOC.HPDACH**	High Protection Threshold	0x00
0x12	**SOC.HPDACL**	High Protection Threshold	0x00
0x13	**SOC.LPDACH**	Low Protection Threshold	0x00
0x14	**SOC.LPDACL**	Low Protection Threshold	0x00
0x15	**SOC.SHEN**	Sample and Hold Enable	0x00
0x16	**SOC.SHCNTRL**	Sample and Hold Control	0x00
0x17	**SOC.PROTINTEN**	Driver Protection Interrupt Enable	0x00
0x18	**SOC.PROTSTAT**	Driver Protection Interrupt Status	0x00
0x19	**SOC.DOUTSIG**	AIO Data Output	0x00
0x1A	**SOC.USER**	USER Register	0x00
0x1B	**SOC.DINSIG0**	AIO Data Input 0	0x00
0x1C	**SOC.DINSIG1**	AIO Data Input 1	0x00
0x1D	**SOC.CFGIO**	AIO10-AIO13 Configuration	0x00
0x1F	**SOC.SIGINTM**	AIO Interrupt Mask Configuration	0x00
0x20	**SOC.SIGINTF**	AIO Interrupt Flag Status	0x00
0x21	**SOC.BLANKING**	BEMF Comparator Blanking Configuration	0x00
0x22	**SOC.SPECCFG0**	AIO7 Hysteresis Configuration	0x00
0x23	**SOC.SPECCFG1**	AIO8/AIO9 Hysteresis Configuration	0x00
0x24	**SOC.SPECCFG2**	AIO7/AIO8 Comparator Input MUX Configuration	0x00
0x25	**SOC.SPECCFG3**	AIO9 Comparator Input MUX Configuration	0x00

12.17 Register Detail

12.17.1 SOC.CFGAIO0

Register 12-1 SOC.CFGAIO0 (AIO0 Configuration, 06h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE10**	RW	00b	00b	01b
5:4	**OPT0**	RW	00b	**OPT0**: AI0/AO10 Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN10:** Differential amplifier gain setting: 000b: 1x 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
3	**POL0**	RW	0b	**POL0**: AI0/AO10 Polarity If **CFGAIO0.OPT0** = 00b, AI0 input polarity setting. If **CFGAIO0.OPT0** = 10b, AO10 output polarity setting: 0b: active high 1b: active low	
2	**MUX0**	RW	0b	**MUX0**: AO10 Digital MUX setting: 000b: DOUT0 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0.
1:0		RW	00b		**LP10EN:** LP10 Comparator option: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

12.17.2 SOC.CFGAIO1

Register 12-2 SOC.CFGAIO1 (AIO1 Configuration, 07h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	R	00b	Reserved, write as 0.	Reserved, write as 0.
5:4	**OPT1**	RW	0b	**OPT1**: AI1 IO Option (input only): 00b: Input 01b: Hi-Z 10b: Hi-Z 11b: Hi-Z	**HP10PREN:** HPROT10 PR Protection enable: 0b: HP10 output to PR disabled 1b: HP10 output to PR enabled
		RW	0b		**LP10PREN:** LPROT10 PR Protection enable: 0b: LP10 output to PR disabled 1b: LP10 output to PR enabled
3	**POL1**	RW	0b	If **CFGAIO1.OPT1** = 00b, AI1 input polarity setting. 0b: active high 1b: active low	**OS10EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX1**	RW	0b	Reserved, write as 0.	**CAL10EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP10EN:** HP10 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

12.17.3 SOC.CFGAIO2

Register 12-3 SOC.CFGAIO2 (AIO2 Configuration, 08h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE32**	RW	00b	00b	01b
5:4	**OPT2**	RW	0b	**OPT2**: AI2 /AO32 Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN32:** Differential amplifier gain setting: 000b: 1x 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
3	**POL2**	RW	0b	If **CFGAIO2.OPT2** = 00b, AI2 input polarity setting. If **CFGAIO2.OPT2** = 10b, AO32 output polarity setting: 0b: active high 1b: active low	
2	**MUX2**	RW	0b	**MUX2**: AO32 Digital MUX setting: 000b: DOUT2 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0.
1:0		RW	0b		**LP32EN:** LP32 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

12.17.4 SOC.CFGAIO3

Register 12-4 SOC.CFGAIO3 (AIO3 Configuration, 09h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	RW	0b	Reserved, write as 0.	Reserved, write as 0.
5	**OPT3**	RW	0b	**OPT3**: AIO3 IO Option: 00b: Input 01b: Hi-Z 10b: Hi-Z 11b: Hi-Z	**HP32PREN:** HPROT32 PR Protection enable: 0b: HP32 output to PR disabled 1b: HP32 output to PR enabled
4		RW	0b		**LP32PREN:** LPROT32 PR Protection enable: 0b: LP32 output to PR disabled 1b: LP32 output to PR enabled
3	**POL3**	RW	0b	If **CFGAIO3.OPT3** = 00b, AI3 input polarity setting 0b: active high 1b: active low	**OS32EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX3**	RW	0b	Reserved, write as 0.	**CAL32EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP32EN:** HP32 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

12.17.5 SOC.CFGAIO4

Register 12-5 SOC.CFGAIO4 (AIO4 Configuration, 0Ah)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE54**	RW	00b	00b	01b
5:4	**OPT4**	RW	0b	**OPT4**: AI4/AO54 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN54:** Differential amplifier gain setting: 000b: 1x 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
3	**POL4**	RW	0b	If **CFGAIO4.OPT4** = 00b, AI4 input polarity setting. If **CFGAIO4.OPT4** = 10b, AO54 output polarity setting: 0b: active high 1b: active low	
2	**MUX4**	RW	0b	**MUX4**: AO54 Digital MUX: 000b: DOUT4 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0.
		RW	00b		**LP54EN:** LP54 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

12.17.6 SOC.CFGAIO5

Register 12-6 SOC.CFGAIO5 (AIO5 Configuration, 0Bh)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	RW	0b	Reserved, write as 0.	Reserved, write as 0.
5	**OPT5**	RW	0b	**OPT5**: AIO5 IO Option: 00b: Input 01b: Hi-Z 10b: Hi-Z 11b: Hi-Z	**HP54PREN:** HPROT54 PR Protection enable: 0b: HP54 output to PR disabled 1b: HP54 output to PR enabled
4		RW	0b		**LP54PREN:** LPROT54 PR Protection enable: 0b: LP54 output to PR disabled 1b: LP54 output to PR enabled
3	**POL5**	RW	0b	If **CFGAIO5.OPT5** = 00b, AI5 input polarity setting. 0b: active high 1b: active low	**OS54EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX5**	RW	0b	Reserved, write as 0.	**CAL54EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP54EN:** HP54 Comparator setting: 00b: disabled 01b: 1µs blanking time 10b: 2µs blanking time 11b: 4µs blanking time

12.17.7 SOC.CFGAIO6

Register 12-7 SOC.CFGAIO6 (AIO6 Configuration, 0Ch)

BIT	IO MODE	GAIN MODE (PGA)	COMPARATOR MODE	SPECIAL MODE (BUF6)
7:6	**MODE6:** 00b	**MODE6:** 01b	**MODE6:** 10b	**MODE6:** 11b
5	**OPT6:** AI6 / AO6 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN6:** AIO6 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT6:** AI6 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write as 0.
4				**SWAP:** Buffer Swap: 0b: Do not swap buffer offset 1b: Swap buffer offset
3	**POL6:** AI6/AO7 Polarity Setting: If **CFGAIO6.OPT6** = 00b, AI6 input polarity setting. If **CFGAIO6.OPT6** = 10b, AO6 output polarity setting: 00b: active-high 01b: active-low		**POL6:** AO6 Comparator output polarity setting: 0b: active-high 1b: active-low	**MUX6:** Analog MUX Setting: 0000b = AI6 0001b = VMSENSE 0010b = VCC33x4/10 0011b = VDDIOx4/10 0100b = VSYSx4/10 0101b = ISENSE 0110b = VPTAT 0111b = VPx1/10 1000b=AB6 1000b: AB6 1001b: AB1 1010b: AB2 1011b: AB3 1100b: AB4 1101b: AB5 1110b: AB6 1111b: AB7
2:0	**MUX6:** AO6 Digital MUX Setting: 000b: DOUT6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0.	**MUX6:** AO6 Digital MUX Setting: 000b: DOUT6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	

12.17.8 SOC.CFGAIO7

Register 12-8 SOC.CFGAIO7 (AIO7 Configuration, 0Dh)

BIT	IO MODE	GAIN MODE (PGA)	COMPARATOR MODE	SPECIAL MODE (PHC)
7:6	**MODE7:** 00b	**MODE7:** 01b	**MODE7:** 10b	**MODE7:** 11b
5	**OPT7:** AI7/AO7 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN7:** AIO7 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT7:** AI7 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write as 0b
4				Reserved, write as 0b
3	**POL7**: AIO7 Polarity Setting: If **CFGAIO7.OPT7** = 00b, AI7 input polarity setting. If **CFGAIO7.OPT7** = 10b, AO7 output polarity setting: 00b: active-high 01b: active-low		**POL7:** AO7 Comparator polarity setting: 0b: active-high 1b: active-low	**POL7:** AO7 Comparator polarity setting: 0b: active-high 1b: active-low
2:0	**MUX7:** AO7 Digital MUX: 000b: DOUT7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX7:** AO7 Analog MUX Setting: 000b: AB7 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX7:** AO7 Digital MUX: 000b: DOUT7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 000b

12.17.9 SOC.CFGAIO8

Register 12-9 SOC.CFGAIO8 (AIO8 Configuration, 0Eh)

BIT	IO MODE	GAIN MODE (PGA)	COMPARATOR MODE	SPECIAL MODE (PHC)
7:6	**MODE8:** 00b	**MODE8:** 01b	**MODE8:** 10b	Reserved, write to 0b.
5	**OPT8:** AI8/AO8 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN8:** AIO8 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT8:** AI8 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write to 0b.
4				Reserved, write to 0b.
3	**POL8:** AI8/AO8 Polarity Setting: 00b: active-high 01b: active-low		**POL8:** AO8 Comparator polarity setting: 0b: active-high 1b: active-low	**POL8:** AO8 Comparator polarity setting: 0b: active-high 1b: active-low
2:0	**MUX8:** AI8 Digital MUX: 000b: DOUT8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX8:** AO8 Analog MUX: 000b: AB8 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX8:** AO8 Digital MUX: 000b: DOUT8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 000b.

12.17.10 SOC.CFGAIO9

Register 12-10 SOC.CFGAIO9 (AIO9 Configuration, 0Fh)

BIT	IO MODE	GAIN MODE (PGA)	COMPARATOR MODE	SPECIAL MODE (PHC)
7	**MODE9:** 00b	**MODE9:** 01b	**MODE9:** 10b	**MODE9[1]:** Switch (4/10)*AIO7/8/9 to AB7/8/9
6				**MODE9[0]:** Switch AIO7/8/9 to CT resistors to generate CT at AB1
5	**OPT9:** AI9/AO9 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN9:** AIO9 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT9:** AI9 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write to 00b.
4				
3	**POL9:** AI9/AO9 Polarity Setting: 00b: active-high 01b: active-low		**POL9:** AO9 Comparator polarity setting: 0b: active-high 1b: active-low	**POL9:** AO9 Comparator polarity setting: 0b: active-high 1b: active-low
2:1	**MUX9:** AO9 Digital MUX: 000b: DOUT9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX9**: AO9 Analog MUX Setting: 000b: AB9 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX9:** AO9 Digital MUX: 000b: DOUT9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write to 00b.
0				Reserved, write to 0b.

12.17.11 SOC.SIGSET

Register 12-11 SOC.SIGSET (Signal Manager Configuration, 10h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**RFU**	R	0b	Reserved, write to 000b
3	**HPROTHYS**	RW	0b	HPx Hysteresis: 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
2	**LPROTHYS**	RW	0b	LPx Hysteresis: 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
1	**LPDACAB3**	RW	0b	Connect LPDAC output to AB3: 1b: LPDAC output connected to AB3 0b: LPDAC output not connected to AB3
0	**HPDACAB2**	RW	0b	Connect HPDAC output to AB2: 1b: HPDAC output connected to AB2 0b: HPDAC output not connected to AB2

12.17.12 SOC.HPDACH

Register 12-12 SOC.HPDACH (HPDAC High Setting, 11h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**HPDAC[9:2]**	RW	0	HPDAC MSB setting bits 9:2

12.17.13 SOC.HPDACL

Register 12-13 SOC.HPDACL (HPDAC Low Setting, 12h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**RFU**	R	0	Reserved, write to 0
1:0	**HPDAC[1:0]**	RW	0	HPDAC MSB setting bits 1:0

12.17.14 SOC.LPDACH

Register 12-14 SOC.LPDACH (LPDAC High Setting, 13h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**LPDAC[9:2]**	RW	0	LPDAC MSB setting bits 9:2

12.17.15 SOC.LPDACL

Register 12-15 SOC.LPDAC1 (LPDAC Low Setting, 14h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**Reserved**	R	0b	Reserved, write to 0.
1:0	**LPDAC[1:0]**	RW	0b	LPDAC Setting bits 1:0

12.17.16 SOC.SHEN

Register 12-16 SOC.SHEN (Sample and Hold Enable, 15h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	000b	Reserved, write to 0
6	**AIO9SHEN**	RW	0b	AIO9 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
5	**AIO8SHEN**	RW	0b	AIO8 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
4	**AIO7SHEN**	RW	0b	AIO7 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
3	**AIO6SHEN**	RW	0b	AIO6 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
2	**DAO54SHEN**	RW	0b	DAO54 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
1	**DAO32SHEN**	RW	0b	DAO32 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H
0	**DAO10SHEN**	RW	0b	DAO10 Sample and Hold buffer enable: 1b: enable S/H 0b: disable and bypass S/H

12.17.17 SOC.SHCNTRL

Register 12-17 SOC.SHCNTRL (Sample and Hold Control, 16h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	RFU	R	000b	Reserved, write to 0
6	**AIO9_HOLD**	RW	0b	AIO9 Sample and Hold Output: 0b: Sample 1b: Hold
5	**AIO8_HOLD**	RW	0b	AIO8 Sample and Hold Output: 0b: Sample 1b: Hold
4	**AIO7_HOLD**	RW	0b	AIO7 Sample and Hold Output: 0b: Sample 1b: Hold
3	**AIO6_HOLD**	RW	0b	AIO6 Sample and Hold Output: 0b: Sample 1b: Hold
2	**DAO54_HOLD**	RW	0b	DAO54 Sample and Hold Output: 0b: Sample 1b: Hold
1	**DAO32_HOLD**	RW	0b	DAO32 Sample and Hold Output: 0b: Sample 1b: Hold
0	**DAO10_HOLD**	RW	0b	DAO10 Sample and Hold Output: 0b: Sample 1b: Hold

12.17.18 SOC.PROTINTEN

Register 12-18 SOC.PROTINTEN (Protection Interrupt Enable, 17h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6	**HP54INTEN**	RW	0b	HPROT54 Interrupt enable: 1b: enable 0b: disabled
5	**HP32INTEN**	RW	0b	HPROT32 Interrupt enable: 1b: enable 0b: disabled
4	**HP10INTEN**	RW	0b	HPROT10 Interrupt enable: 1b: enable 0b: disabled
3	**RFU**	R	0b	Reserved, write to 0.
2	**LP54INTEN**	RW	0b	LPROT54 Interrupt enable: 1b: enable 0b: disabled
1	**LP32INTEN**	RW	0b	LPROT32 Interrupt enable: 1b: enable 0b: disabled
0	**LP10INTEN**	RW	0b	LPROT10 Interrupt enable: 1b: enable 0b: disabled

12.17.19 SOC.PROTSTAT

Register 12-19 SOC.PROTSTAT (Protection Interrupt Status, 18h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HP54STAT**	R	0b	HPROT54 Real-time status: 0b: Comparator output low 1b: Comparator output high
6	**HP54INT**	RW	0b	HPROT54 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
5	**HP32INT**	RW	0b	HPROT32 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
4	**HP10INT**	RW	0b	HPROT10 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
3	**LP54STAT**	R	0b	LPROT54 Real-time status: 0b: Comparator output low 1b: Comparator output high
2	**LP54INT**	RW	0b	LPROT54 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
1	**LP32INT**	RW	0b	LPROT32 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
0	**LP10INT**	RW	0b	LPROT10 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear

12.17.20 SOC.DOUTSIG0

Register 12-20 SOC.DOUTSIG0 (Digital Output 0, 19h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6	**DOUT9**	RW	0b	Data output to AO9.
5	**DOUT8**	RW	0b	Data output to AO8.
4	**DOUT7**	RW	0b	Data output to AO7.
3	**DOUT6**	RW	0b	Data output to AO6.
2	**DOUT4**	RW	0b	Data output to AO54.
1	**DOUT2**	RW	0b	Data output to AO32.
0	**DOUT0**	RW	0b	Data output to AO10.

12.17.21 SOC.USER

Register 12-21 SOC.USER (User Register ,1Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**USER**	RW	0b	USER Register. Data preserved during reset

12.17.22 SOC.DINSIG0

Register 12-22 SOC.DINSIG0 (Digital Input 0, 1Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**RFU**	RW	00b	Reserved, write to 0.
5	**DIN5**	R	0b	Data input from AIO5.
4	**DIN4**	R	0b	Data input from AIO4.
3	**DIN3**	R	0b	Data input from AIO3.
2	**DIN2**	R	0b	Data input from AIO2.
1	**DIN1**	R	0b	Data input from AIO1.
0	**DIN0**	R	0b	Data input from AIO0.

12.17.23 SOC.DINSIG1

Register 12-23 SOC.DINSIG1 (Digital Input 1, 1Ch)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**RFU**	R	000b	Reserved, write to 0.
3	**DIN9**	R	0b	Data input from AIO9.
2	**DIN8**	R	0b	Data input from AIO8.
1	**DIN7**	R	0b	Data input from AIO7.
0	**DIN6**	R	0b	Data input from AIO6.

12.17.24 SOC.CFGIO1

Register 12-24 SOC.CFGIO1 (AIO10-AIO13 Configuration 1, 1Dh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	000b	Reserved, write as 0.
4	**EN_AIO6_OCP**	RW	0b	Enable AIO6 comparator output to disable gate driver on OC event.
3	**VREFBP**	RW	0b	Switch VREF signal to AB5 so that it can be buffered out on AIO6.
2	**RFU**	R	0 0000b	Reserved, write as 0.
1:0	**VTHREF**	RW	00b	Threshold voltage for comparators in AIO<9:6>: 00b: 0.1V 01b: 0.2V 10b: 0.5V 11b: 1.25V

12.17.25 SOC.SIGINTM

Register 12-25 SOC.SIGINTM (AIO Interrupt Mask, 1Fh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**AI9REINTEN**	RW	0b	AI9 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
6	**AI8REINTEN**	RW	0b	AI8 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
5	**AI7REINTEN**	RW	0b	AI7 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
4	**AI6REINTEN**	RW	0b	AI6 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
3	**AI9FEINTEN**	RW	0b	AI9 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
2	**AI8FEINTEN**	RW	0b	AI8 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
1	**AI7FEINTEN**	RW	0b	AI7 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
0	**AI6FEINTEN**	RW	0b	AI6 digital input falling edge interrupt enable. 0b: disabled 1b: enabled

12.17.26 SOC.SIGINTF

Register 12-26 SOC.SIGINTF (AIO Interrupt Flag, 20h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HP32STAT**	R	0b	HPROT32 Real-time status: 0b: Comparator output low 1b: Comparator output high
6	**LP32STAT**	R	0b	LPROT32 Real-time status: 0b: Comparator output low 1b: Comparator output high
5	**HP10STAT**	R	0b	HPROT10 Real-time status: 0b: Comparator output low 1b: Comparator output high
4	**LP10STAT**	R	0b	LPROT10 Real-time status: 0b: Comparator output low 1b: Comparator output high
3	**AI9INTF**	RW	0b	AI9 Interrupt Flag: 0b: No Interrupt 1b: Interrupt. Write 1b to clear.
2	**AI8INTF**	RW	0b	AI8 Interrupt Flag: 0b: No Interrupt 1b: Interrupt. Write 1b to clear.
1	**AI7INTF**	RW	0b	AI7 Interrupt Flag: 0b: No Interrupt 1b: Interrupt. Write 1b to clear.
0	**AI6INTF**	RW	0b	AI6 Interrupt Flag: 0b: No Interrupt 1b: Interrupt. Write 1b to clear.

12.17.27 SOC.BLANKING

Register 12-27 SOC.BLANKING (Comparator Blanking Configuration, 21h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**BLANKTIME**	RW	0000b	Blanking time for BEMF Comparator: 1111b: 6000ns 1110b: 5500ns 1101b: 5000ns 1100b: 4500ns 1011b: 4000ns 1010b: 3500ns 1001b: 3000ns 1000b: 2500ns 0111b: 2000ns 0110b: 1500ns 0101b: 1250ns 0100b: 1000ns 0011b: 750ns 0010b: 500ns 0001b: 250ns 0000b: 100ns
3:2	**RFU**	R	00b	Reserved, write as 0.
1:0	**BLANKMODE**	R/W	00b	BEMF Comparator Blanking Mode: 11b: Leading and trailing edge blanking 10b: Trailing edge blanking 01b: Leading edge blanking 00b: Disabled

12.17.29 SOC.SPECCFG0

Register 12-28 SOC.SPECCFG0 (AIO7 Comparator Hysteresis Configuration, 22h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HYSMODE**	RW	0x0	AIO7 Special Mode Comparator Hysteresis Mode: 1b: Hysteresis = 0/24/48/96 mV 0b: Hysteresis = 0/6/12/24 mV
6:4	**RFU**	R	0x0	Reserved
3:0	**AIO7HYS**	R/W	0x0	AIO7 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 1111b: Rising = 24mV, Falling = 24mV 1110b: Rising = 24mV, Falling = 12mV 1101b: Rising = 24mV, Falling = 6mV 1100b: Rising = 24mV, Falling = 0mV 1011b: Rising = 12mV, Falling = 24mV 1010b: Rising = 12mV, Falling = 12mV 1001b: Rising = 12mV, Falling = 6mV 1000b: Rising = 12mV, Falling = 0mV 0111b: Rising = 6mV, Falling = 24mV 0110b: Rising = 6mV, Falling = 12mV 0101b: Rising = 6mV, Falling = 6mV 0100b: Rising = 6mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 24mV 0010b: Rising = 0mV, Falling = 12mV 0001b: Rising = 0mV, Falling = 6mV 0000b: Rising = 0mV, Falling = 0mV AIO7 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 1111b: Rising = 96mV, Falling = 96mV 1110b: Rising = 96mV, Falling = 48mV 1101b: Rising = 96mV, Falling = 24mV 1100b: Rising = 96mV, Falling = 0mV 1011b: Rising = 48mV, Falling = 96mV 1010b: Rising = 48mV, Falling = 48mV 1001b: Rising = 48mV, Falling = 24mV 1000b: Rising = 48mV, Falling = 0mV 0111b: Rising = 24mV, Falling = 96mV 0110b: Rising = 24mV, Falling = 48mV 0101b: Rising = 24mV, Falling = 24mV 0100b: Rising = 24mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 96mV 0010b: Rising = 0mV, Falling = 48mV 0001b: Rising = 0mV, Falling = 24mV 0000b: Rising = 0mV, Falling = 0mV

12.17.30 SOC.SPECCFG1

Register 12-29 SOC.SPECCFG1 (AIO8/9 Comparator Hysteresis Configuration, 23h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**AIO8HYS**	R/W	0x0	AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 1111b: Rising = 24mV, Falling = 24mV 1110b: Rising = 24mV, Falling = 12mV 1101b: Rising = 24mV, Falling = 6mV 1100b: Rising = 24mV, Falling = 0mV 1011b: Rising = 12mV, Falling = 24mV 1010b: Rising = 12mV, Falling = 12mV 1001b: Rising = 12mV, Falling = 6mV 1000b: Rising = 12mV, Falling = 0mV 0111b: Rising = 6mV, Falling = 24mV 0110b: Rising = 6mV, Falling = 12mV 0101b: Rising = 6mV, Falling = 6mV 0100b: Rising = 6mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 24mV 0010b: Rising = 0mV, Falling = 12mV 0001b: Rising = 0mV, Falling = 6mV 0000b: Rising = 0mV, Falling = 0mV AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 1111b: Rising = 96mV, Falling = 96mV 1110b: Rising = 96mV, Falling = 48mV 1101b: Rising = 96mV, Falling = 24mV 1100b: Rising = 96mV, Falling = 0mV 1011b: Rising = 48mV, Falling = 96mV 1010b: Rising = 48mV, Falling = 48mV 1001b: Rising = 48mV, Falling = 24mV 1000b: Rising = 48mV, Falling = 0mV 0111b: Rising = 24mV, Falling = 96mV 0110b: Rising = 24mV, Falling = 48mV 0101b: Rising = 24mV, Falling = 24mV 0100b: Rising = 24mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 96mV 0010b: Rising = 0mV, Falling = 48mV 0001b: Rising = 0mV, Falling = 24mV 0000b: Rising = 0mV, Falling = 0mV
3:0	**AIO9HYS**	R/W	0x0	AIO9 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 1111b: Rising = 24mV, Falling = 24mV 1110b: Rising = 24mV, Falling = 12mV 1101b: Rising = 24mV, Falling = 6mV 1100b: Rising = 24mV, Falling = 0mV 1011b: Rising = 12mV, Falling = 24mV 1010b: Rising = 12mV, Falling = 12mV 1001b: Rising = 12mV, Falling = 6mV 1000b: Rising = 12mV, Falling = 0mV 0111b: Rising = 6mV, Falling = 24mV 0110b: Rising = 6mV, Falling = 12mV 0101b: Rising = 6mV, Falling = 6mV 0100b: Rising = 6mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 24mV 0010b: Rising = 0mV, Falling = 12mV 0001b: Rising = 0mV, Falling = 6mV

				0000b: Rising = 0mV, Falling = 0mV AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 1111b: Rising = 96mV, Falling = 96mV 1110b: Rising = 96mV, Falling = 48mV 1101b: Rising = 96mV, Falling = 24mV 1100b: Rising = 96mV, Falling = 0mV 1011b: Rising = 48mV, Falling = 96mV 1010b: Rising = 48mV, Falling = 48mV 1001b: Rising = 48mV, Falling = 24mV 1000b: Rising = 48mV, Falling = 0mV 0111b: Rising = 24mV, Falling = 96mV 0110b: Rising = 24mV, Falling = 48mV 0101b: Rising = 24mV, Falling = 24mV 0100b: Rising = 24mV, Falling = 0mV 0011b: Rising = 0mV, Falling = 96mV 0010b: Rising = 0mV, Falling = 48mV 0001b: Rising = 0mV, Falling = 24mV 0000b: Rising = 0mV, Falling = 0mV

12.17.31 SOC.SPECCFG2

Register 12-30 SOC.SPECCFG2 (AIO7/8 Comparator MUX Input Configuration, 24h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6:4	**SMUXAIO7**	RW	000b	Special Mode Comparator Input MUX Selection for AIO7: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO8 (phase to phase compare) 101b: AIO9 (phase to phase compare) 110b: RFU 111b: RFU
3	**RFU**	R	0b	Reserved, write to 0.
2:0	**SMUXAIO8**	RW	000b	Special Mode Comparator Input MUX Selection for AIO8: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (phase to phase compare) 101b: AIO9 (phase to phase compare) 110b: RFU 111b: RFU

12.17.32 SOC.SPECCFG3

Register 12-31 SOC.SPECCFG3 (AIO9 Comparator MUX Input Configuration, 25h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6:4	**SMUXAIO9**	RW	000b	Special Mode Comparator Input MUX Selection for AIO7: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (phase to phase compare) 101b: AIO8 (phase to phase compare) 110b: RFU 111b: RFU
3:0	**RFU**	R	000b	Reserved, write to 0.

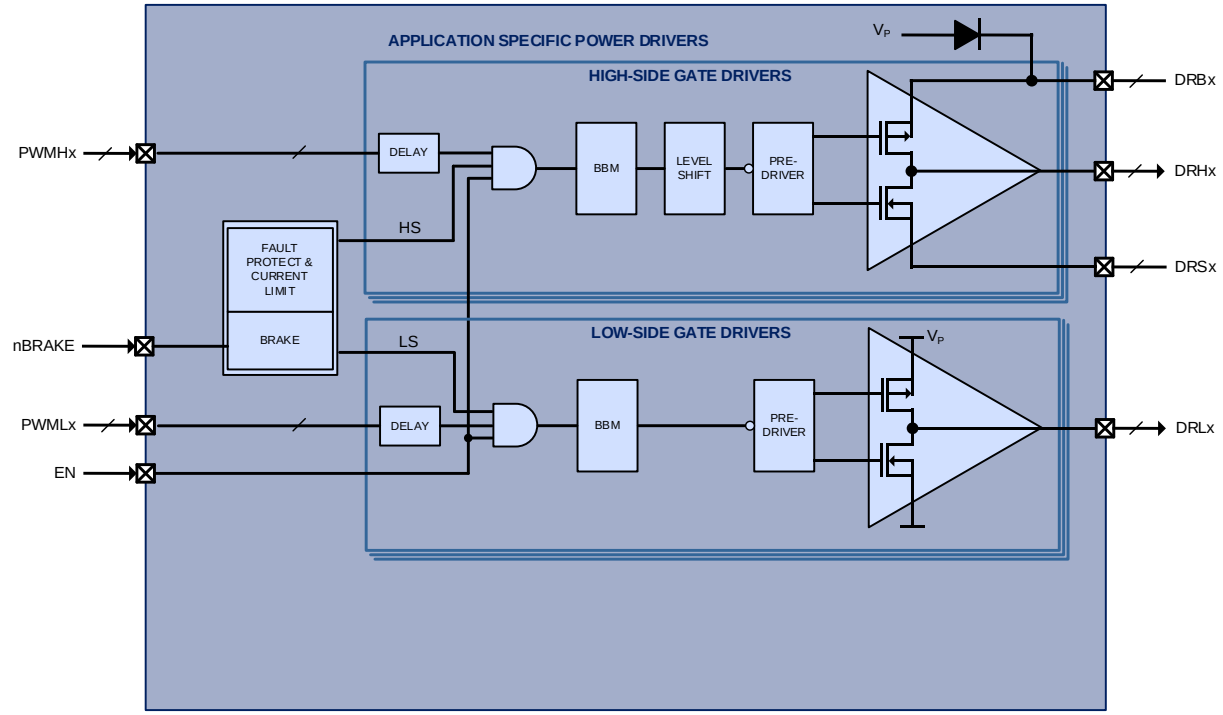
13 APPLICATION SPECIFIC POWER DRIVERS (ASPD)

13.1 Features

- 3 low-side and 3 high-side gate drivers
- 2A sink/source gate driving capability
- Configurable propagation delays
- Fast fault protection
- Cycle-by-cycle current limit function
- Configurable driver break-before-make (BBM) safety function

13.2 Block Diagram

Figure 13-1 Application Specific Power Drivers



13.3 Functional Description

The Application Specific Power Drivers (ASPD, Figure 13-1) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 13-2 below shows typical gate driver connections and Table 13-1 shows the ASPD available resources. The ASPD gate drivers support up to a 160V source supply.

Figure 13-2 Typical Gate Driver Connections

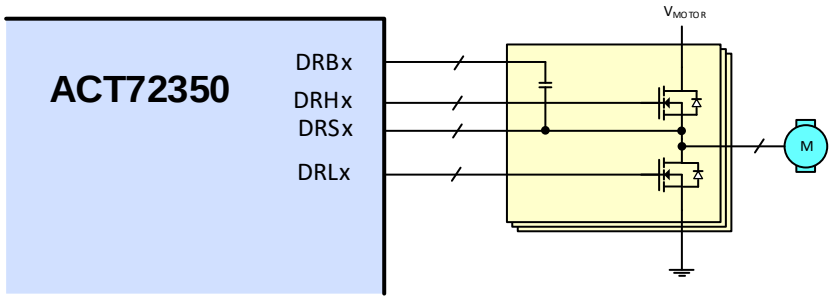


Table 13-1 Power Driver Resources by Part Numbers

PART NUMBER	LOW-SIDE GATE DRIVER		HIGH-SIDE GATE DRIVER		
	DRLx	SOURCE/SINK CURRENT	DRHx	SOURCE/BOOTSTRAP SUPPLY	SOURCE/SINK CURRENT
ACT72350	3	2A/2A	3	160V/180V	2A/2A

The ASPD includes built-in configurable fault protection for the internal gate drivers.

13.4 Low-Side Gate Driver

The DRLx low-side gate driver drives the gate of an external MOSFET or IGBT switch between the low-level power ground rail and high-level V_P supply rail. The DRLx output pin has sink and source output current capability of 2A. Each low-side gate driver is controlled by a PWM port input signal.

13.5 High-Side Gate Driver

The DRHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DRSx driver source rail and its high-level DRBx bootstrap rail. The DRSx pin can go up to 160V steady state (VM + 15V maximum). The DRHx output pin has sink and source output current capability of 2A.

The DRBx bootstrap pin can have a maximum operating voltage of 15V relative to the DRSx pin, and up to 175V steady state. The DRSx pin can have a maximum operating voltage of 10V relative to the VM pin. The DRSx pin is designed to tolerate momentary switching negative spikes down to -10V without affecting the DRHx output state. Each high-side gate driver is controlled by a PWM port signal.

For bootstrapped high-side operation, connect an appropriate capacitor between DRBx and DRSx. Each high side driver includes its own internal bootstrap diode with respective current limiting resistor. To operate the DRHx output as a low-side gate driver, connect its DRBx pin to V_P and its DRSx pin to V_{SS}.

13.6 Power Drivers Control

The ASPD is controlled via the EN signal. When the EN signal is high, the ASPD module is enabled and the DRx outputs follow their respective PWMx input. When the EN signal is low, the ASPD module is disabled and all gate driver outputs are disabled.

nBRAKE	EN	PWMHx	PHMLx	DRHx	DRLx
0	0	X	X	HiZ	200K Pull Down
0	1	X	X	LO	HI
1	0	X	X	HiZ	200K Pull Down
1	1	0	0	LO	LO
		0	1	LO	HI
		1	0	HI	LO
		1	1	LO	LO

13.7 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR) signal. The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DRH3/DRH4/DRH5 gate drivers are designated as high-side group 1. The PR signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR mask bit settings. If the ASPD has unmasked the high-side PR protection (**CFGDRV1.nHSPRM** = 1b) then the high-side gate drivers will be disabled. If the ASPD has unmasked the low-side PR protection (**CFGDRV1.nLSPRM** = 1b), then the low-side gate drivers will be disabled.

Alternatively, faults on any of the driven switches can be programmed to drive the nFAULT output signal, in the event of a protection mechanism triggering.

Once the gate drivers have been disabled through an over current event, the MCU must reset the ASPD by toggling the EN line for at least 50 us in order to re-enable the ASPD module.

13.8 Break Before Make (BBM)

The ASPD supports a Break Before Make (BBM) configuration option for hardware protection against current shoot-through.

There are two types of BBM support:

- Single-driver BBM
- Half-bridge BBM

Single-driver BBM is always enabled and guarantees that the internal PMOS and NMOS FETs for a single gate driver are not on at the same time.

Half-bridge BBM can be enabled by setting **CFGDRV1.ENBBM** to 1b. When enabled, the half-bridge BBM function inserts 100ns of dead-time between in each of the half-bridge drivers (DRH3/DRL0, DRH4/DRL1, DRH5/DRL2).

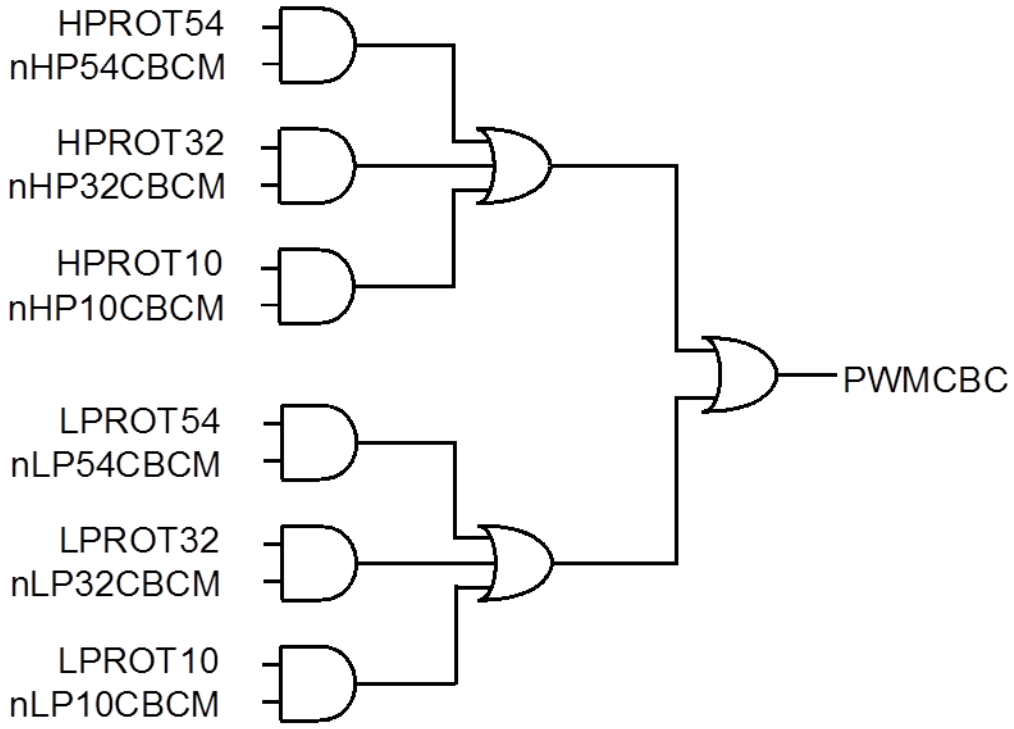
13.9 Cycle by Cycle Current Limit

To provide hardware assist for current limit, the ASPD may be configured to temporarily disable the gate drivers, when the current is over a configured threshold.

During these events, the ASPD may turn off all the high-side, low-side or high-side and low-side gate drivers based on the state of the Signal Manager HPCOMP/LPCOMP comparators. This can allow applications to have cycle by cycle current limit, without intervention of the MCU.

The diagram below shows how the protection comparators can be used to generate an event signal PWMCBC, which can be used to control this operation.

Figure 13-3 Cycle by Cycle Current Limit



The mask signal (**CFGDRV2.nDRVxyDISM**) is used to select which half-bridge to enable cycle-by-cycle current limit on, while **CFGDRV2.LPCBCHS** and **CFGDRV2.LPCBCLS** are used to select the high-side or low-side gate driver for the half-bridge to disable.

The real-time status of which half-bridge is in cycle-by-cycle current limit operation is available in **STATDRV.DRVxyDISSTAT**. The latched status is available in **STATDRV.DRVxyDIS**.

During operation, if the PWMCBC signal is high, then the output to the configured gate drivers is temporarily disabled, until the PWMCBC becomes available again. The following shows which drivers are disabled during this condition:

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV52DISM** = 1b, disable DRH5
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV52DISM** = 1b, disable DRL2

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV41DISM** = 1b, disable DRH4
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV41DISM** = 1b, disable DRL1

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV30DISM** = 1b, disable DRH3
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV30DISM** = 1b, disable DRL0

13.10 nBRAKE Actuation

The ASPD includes a braking source through the nBRAKE pin. An external microcontroller, or in some cases a redundant safety microcontroller, can assert the nBRAKE signal low in order to invoke the Braking mode. To enter braking mode, the nBRAKE signal must be made low for 50 us. Once in Braking mode, all of the high side gate drivers will disable their respective switches, while the low side gate drivers will follow the brake command. When nBRAKE is low, all low side gate drivers are enabling their respective switch and the braking force is applied as the motor winding is shorted. When nBRAKE is high, all low side gate drivers disable their switches and the phase output is Hi-Z. During Braking mode, the six PWM inputs are ignored.

To exit Braking mode, the nBRAKE signal must be made high and the EN signal low. When re-enabled, the tri phase inverter will operate normally.

Figure 13-4 Entering and Exiting Braking Mode

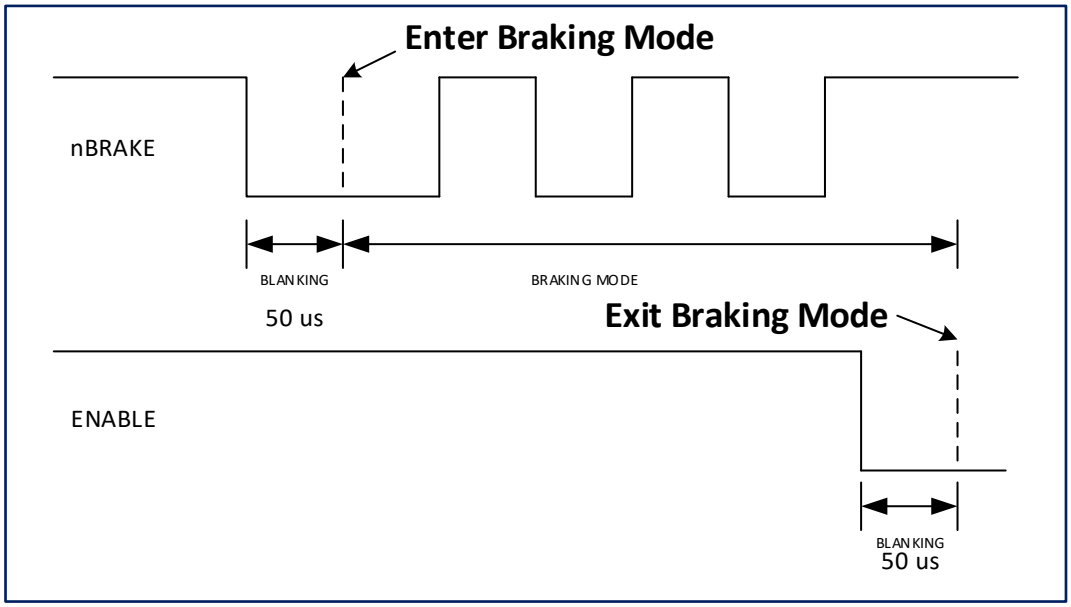
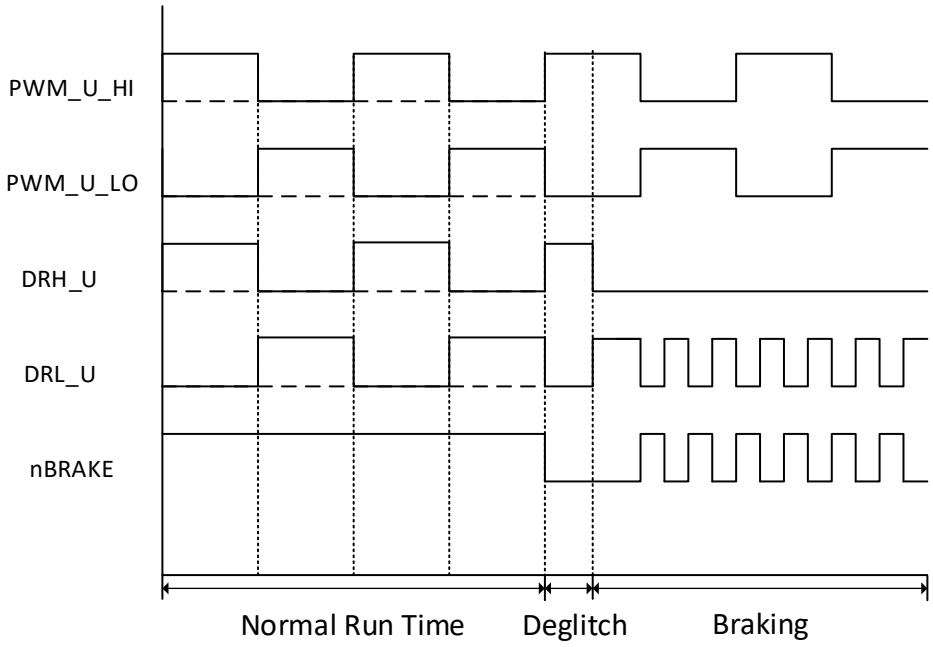


Figure 13-5 Braking Mode Operation



13.11 Electrical Characteristics

Table 13-2 Gate Driver Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Low-Side Gate Drivers (DRLx pins)						
$V_{OH;DRL}$	High-level output voltage	I_{DRLx} = -50mA	V_P-0.3			V
$V_{OL;DRL}$	Low-level output voltage	I_{DRLx} = 50mA			0.3	V
$I_{OHPK;DRL}$	Output high source current	10µs pulse		2		A
$I_{OLPK;DRL}$	Output low sink current	10µs pulse		2		A
High-Side Gate Drivers (DRHx, DRBx and DRSx pins)						
V_{DRS}	Level-shift driver source voltage range		-10		VM + 10	V
V_{DRB}	Bootstrap pin voltage range	Relative to V_{DRS}	10		20	V
		Relative to VSS			175	V
$V_{UVLO;DRB}$	Bootstrap UVLO threshold	V_{DRBx} rising	8.5			V
		Hysteresis		2		V
$I_{BS;DRB}$	Bootstrap supply current	Current from DRBx to DRSx		28		µA
$I_{OS;DRB}$	Offset supply current	Current from DRBx to ground		10		µA
$V_{OH;DRH}$	High-Level output voltage	I_{DRHx} = -50mA	V_{DRBx}-0.3			V
$V_{OL;DRH}$	Low-level output voltage	I_{DRHx} = 50mA			V_{DRSx}+0.3	V
$I_{OHPK;DRH}$	Output high source current	10µs pulse		2		A
$I_{OLPK;DRL}$	Output low sink current	10µs pulse		2		A

Table 13-3 Driver Enable (EN) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{EN}	EN pin voltage range		0		5	V
V_{IH_EN}	High-Level input voltage		2.3			V
V_{IL_EN}	Low-level input voltage				0.8	V
R_{PD_EN}	EN pull down resistance			1		MOhms
$EN_{DEGLITCH}$	Deglitch			50		µs

Table 13-4 PWMH Inputs (PWMHx) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{PWMH}	PWMH pin voltage range	VSYS = VCCIO = 5V	0		5	V
V_{IH_PWMH}	High-Level input voltage	VCCIO = 3.3V	1.7			V
		VCCIO = VSYS (5V)	2.3			V
V_{IL_PWMH}	Low-level input voltage	VCCIO = 3.3V			0.4	V
		VCCIO = VSYS (5V)			0.8	V
R_{PD_PWMH}	PWMH pull down resistance			50		KOhms

Table 13-5 PWML Inputs (PWMLx) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{PWML}	PWML pin voltage range	VSYS = VCCIO = 5V	0		5	V
V_{IH_PWML}	High-Level input voltage	VCCIO = 3.3V	1.7			V
		VCCIO = VSYS (5V)	2.3			V
V_{IL_PWML}	Low-level input voltage	VCCIO = 3.3V			0.4	V
		VCCIO = VSYS (5V)			0.8	V
R_{PD_PWML}	PWML pull down resistance			50		KOhms

Table 13-6 nBRAKE Input (nBRAKE) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{nBRAKE}	nBRAKE pin voltage range		0		5	V
V_{IH_nBRAKE}	High-Level input voltage		2.3			V
V_{IL_nBRAKE}	Low-level input voltage				0.8	V

13.12 Register Summary

Table 13-6 ASPD Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
27h	**SOC.CFGDRV1**	Driver Configuration 1	00h
28h	**SOC.CFGDRV2**	Driver Configuration 2	00h
29h	**SOC.CFGDRV3**	Driver Configuration 3	00h
2Ah	**SOC.STATDRV**	Driver Status	00h

13.13 Register Detail

13.13.1 SOC.CFGDRV1

Register 13-1 SOC.CFGDRV1 (Driver Configuration 1, 27h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**BBMSEL**	RW	000b	Break Before Make Delay Select: 000b: 250ns 001b: 500ns 010b: 750ns 011b: 1000ns 100b: 1250ns 101b: 1500ns 110b: 1750ns 111b: 2000ns
4	**BSTPREN**	RW	0b	Bootstrap Protection Enable: 0b: BSTPR disabled 1b: BSTPR enabled
3	**HSPREN**	RW	0b	High side PR protection enable: 0b: PR1 disabled 1b: PR1 enabled
2	**LSPREN**	RW	0b	Low side PR protection enable: 0b: PR1 disabled 1b: PR1 enabled
1	**DRSFLTPREN**	RW	0b	Phase Detection Fault Protection: 0b: DRSFLTPR Enabled 1b: DRSFLTPR Disabled
0	**ENBBM**	RW	0b	Enable Break-before-make. When enabled, inserts 100ns dead-time between the high and low-side PWM signal of each pair of half-bridges (DRH3/DRL0, DRH4/DRL1, DRH5/DRL2): 0b: disabled 1b: enabled

13.13.2 SOC.CFGDRV2

Register 13-2 SOC.CFGDRV2 (Driver Configuration 2, 28h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	RW	0b	Reserved, write as 0.
4	**nDRV52DISM**	R/W	0b	Mask signal for DRH5/DRL2 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
3	**nDRV41DISM**	R/W	0b	Mask signal for DRH4/DRL1 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
2	**nDRV30DISM**	R/W	0b	Mask signal for DRH3/DRL0 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
1	**LPCBCLS**	R/W	0b	Control signal for low-side gate drivers disable. Used for PWM pulse cycle-by-cycle current limit: 0b: Do not disable 1b: Disable when commanded
0	**LPCBCHS**	R/W	0b	Control signal for high-side gate drivers disable. Used for PWM pulse cycle-by-cycle current limit: 0b: Do not disable 1b: Disable when commanded

13.13.3 SOC.CFGDRV3

Register 13-3 SOC.CFGDRV3 (Driver Configuration 3, 29h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**nHP54CBCM**	R/W	0b	Mask signal for HPROT54 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
6	**nLP54CBCM**	R/W	0b	Mask signal for LPROT54 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
5	**nHP32CBCM**	R/W	0b	Mask signal for HPROT32 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
4	**nLP54CBCM**	R/W	0b	Mask signal for LPROT32 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
3	**nHP10CBCM**	R/W	0b	Mask signal for HPROT10 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
2	**nLP10CBCM**	R/W	0b	Mask signal for LPROT10 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
1	**PEXTDIS**	RW	0b	PWM Pulse Extension Disable: 0b: Pulse Extension Enabled 1b: Pulse Extension Disabled
0	**DRVFLT_BLK_SET**	RW	0b	Reserved, write as 0.

13.13.4 SOC.STATDRV

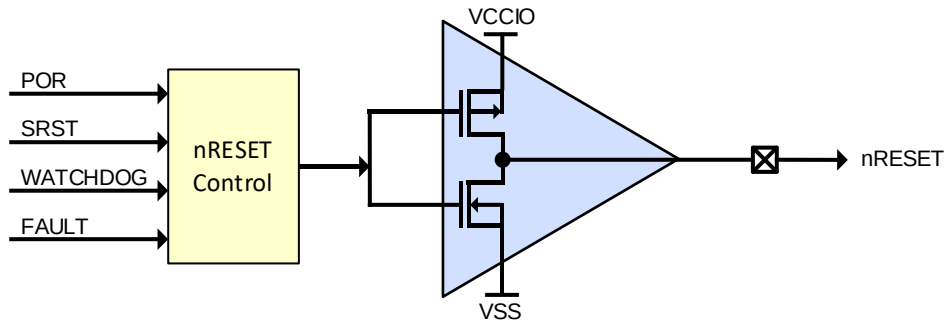
Register 13-4 SOC.STATDRV (Driver Status, 2Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	0b	Reserved, write as 0.
4	**BST_LOW_RTS**	R	0b	Real-time status of BSTLOW signal: 0b: No bootstrap low voltage condition 1b: Bootstrap low voltage present
3	**DRSFLT_RTS**	R	0b	Real-time status of DRSFLT signal: 0b: No DRSFLT present 1b: DRSFLT present
2	**RFU**	R	0b	Reserved, write as 0.
1	**BST_LOW**	R	0b	Latched status of BSTLOW signal. To clear, write this bit to a 1b: 0b: No bootstrap low event occurred 1b: Bootstrap voltage low event occurred
0	**DRS_FLT**	R	0b	Latched status of DRSFLT signal. To clear, write this bit to a 1b: 0b: No phase detection fault 1b: Phase detection fault occurred

14 nRESET Generator

14.1 Block Diagram

Figure 14-1 nRESET Push/Pull Output



14.2 Functional Description

The ACT72350 provides a configurable nRESET output signal the application can use to generate external microcontroller reset events. During power up, while all internal power rails are initializing, the nRESET signal is held low to ensure the external microcontroller is kept under reset until all power structures are stable. During normal operation, the nRESET is kept logic HI. If programmed, the nRESET signal will be pulled low during certain faults. The external microcontroller can also issue a software based nRESET by writing a 1 to the **WATCHDOG.SRST** register. When the watchdog is enabled, and if the watchdog counter is not cleared on time, the nRESET is asserted.

Table 14-1 nRESET Input (nRESET) Electrical Characteristics

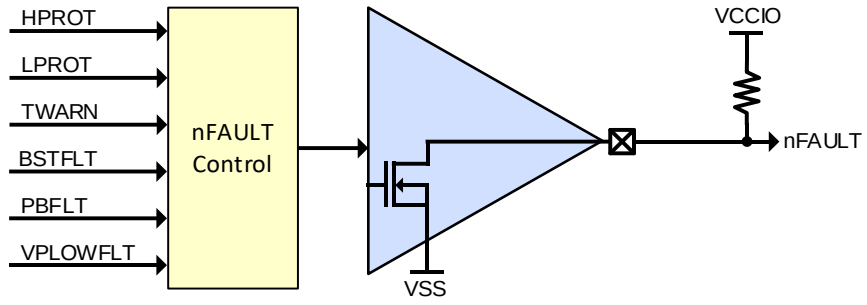
(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{nRESET}	nRESET pin voltage range	VCCIO=VSYS	0		5	V
V_{IH_nRESET}	High-Level input voltage	VCCIO = 3.3V, 1.5mA load	VCCIO-0.6			V
		VCCIO = VSYS (5V), 1.5mA load	VCCIO-0.6			V
V_{IL_nRESET}	Low-level input voltage	VCCIO = 3.3V, 1.5mA sink			0.9	V
		VCCIO = VSYS (5V), 1.5mA sink			0.9	V
I_{OH_NRESET}	nRESET output source current	10us pulse		10		mA
I_{OL_NRESET}	nRESET output sink current	10us pulse		10		mA

15 nFAULT Generator

15.1 Block Diagram

Figure 15-1 nFAULT Open Drain Output



15.2 Functional Description

The open drain output nFAULT can be used by the external microcontroller to learn of when an internal fault or event has occurred within the ACT72350 device. Fault generation is programmable with every nFAULT generating source being maskable. Faults and events asserting the nFAULT output are:

- HPROT: Used for Over Current Event (OCP) with the HPROT comparator and HPDAC reference.
- LPROT: Used for Over Current Event (OCP) with the LPROT comparator and LPDAC reference.
- TWARN: Over temperature warning (die temperature exceeds 145 degrees C).
- BSTFLT: Bootstrap voltage is below its UVLO.
- PBFLT: Push Button has been pressed.
- VPLOWFLT: VP DC/DC switching controller output voltage is below its UVLO.

Table 15-1 nFAULT Open Drain Output (nFault) Electrical Characteristics

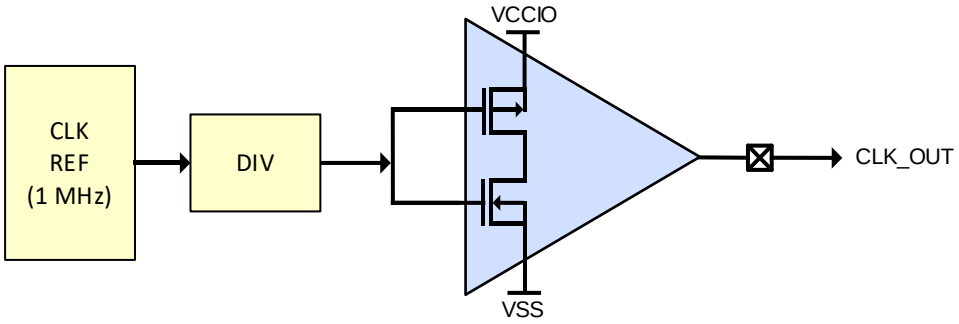
(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{nFAULT}	nFAULT pin voltage range		0		5	V
V_{OL_nFAULT}	Low-level output voltage	I_{nFAULT}=7 mA			0.3	V
I_{OH_NFAULT}	nFAULT output sink current	V_{nFAULT}=0.3V	10	20		mA

16 CLK_OUT

16.1 Block Diagram

Figure 16-1 CLK_OUT Push Pull Output



16.2 Functional Description

The ACT72350 device contains a 1 MHz internal oscillator with an output at the CLK_OUT terminal. The purpose for this clock signal output is to allow external microcontrollers a known time base which can be used to discriminate against faulty internal timing functions. By comparing the amount of time in between pulses, microcontroller timer functions can be determined to be operating within normal useful range or faulty conditions.

Enabling the CLK_OUT function is accomplished by writing a 1 to the **SOC.MISC.CLKOUTEN** register bit. Default frequency is 125 KHz but by configuring the **SOC.PWRCTL.CLKOUTFREQ** registers bits different divided down frequencies can be obtained.

Table 16-1 CLK_OUT Output (CLK_OUT) Electrical Characteristics

(V_P = 12V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CLKOUT}	CLK_OUT pin voltage range	VSYS = VCCIO	0		5	V
$FREQ_{CLOCK\_OUT}$	Clock Out Frequency	Ta = 25°C	-1%	1	1%	MHz
		Ta = −40°C to Ta = 125°C	-2.5%	1	2.5%	MHz
V_{OH_CLKOUT}	High-Level output voltage	VCCIO = 3.3V, 3mA load	VCCIO-0.6			V
		VCCIO = VSYS (5V), 3mA load	VCCIO-0.6			V
V_{OL_CLKOUT}	Low-level output voltage	VCCIO = 3.3V, 3mA sink			0.6	V
		VCCIO = VSYS (5V), 3mA sink			0.6	V
$I_{OH\_CLK\_OUT}$	CLK_OUT output source current	10us pulse		20		mA
$I_{OL\_CLK\_OUT}$	CLK_OUT output sink current	10us pulse		20		mA

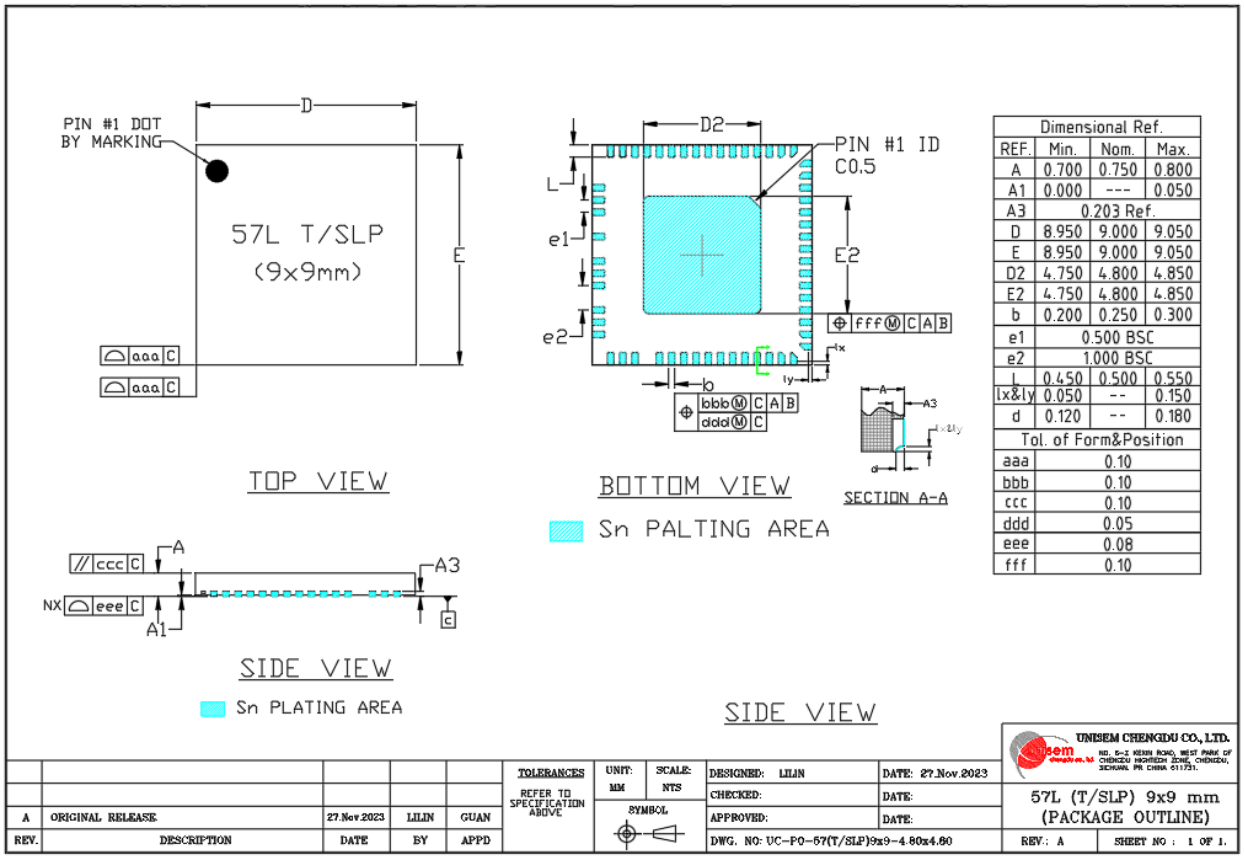
17 THERMAL CHARACTERISTICS

Table 17-1 Thermal Characteristics

PARAMETER	VALUE	UNIT
Operating ambient temperature range	-40 to 125	°C
Operating junction temperature range	-40 to 150	°C
Storage temperature range	-55 to 150	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Junction-to-case thermal resistance (Θ_{JC})	2.897	°C/W
Junction-to-ambient thermal resistance (Θ_{JA})	23.36	°C/W

18 PACKAGE OUTLINE AND DIMENSIONS

18.1 57L T/SLP 9mm x 9mm Package Outline and Dimensions



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	---	0.050
A3	0.203 Ref.		
D	8.950	9.000	9.050
E	8.950	9.000	9.050
D2	4.750	4.800	4.850
E2	4.750	4.800	4.850
b	0.200	0.250	0.300
e1	0.500 BSC		
e2	1.000 BSC		
L	0.450	0.500	0.550
lx&ly	0.050	--	0.150
d	0.120	--	0.180
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

REV.	DESCRIPTION	DATE	BY	APPD
A	ORIGINAL RELEASE	27.Nov.2023	LILIN	GUAN

TOLERANCES: REFER TO SPECIFICATION ABOVE
UNIT: MM SCALE: NTS
SYMBOL
DESIGNED: LILIN DATE: 27.Nov.2023
CHECKED: DATE:
APPROVED: DATE:
DWG. NO: UC-PO-57(T/SLP)9x9-4.80x4.60

UNISEM CHENGDU CO., LTD.
NO. 6-2 KEXIN ROAD, WEST PARK OF CHENGDU HIGHTECH ZONE, CHENGDU, SICHUAN PR CHINA 611731.

57L (T/SLP) 9x9 mm
(PACKAGE OUTLINE)

REV.: A SHEET NO : 1 OF 1.

Notes:

1. All dimensions are in millimeters
2. Dimensioning and Tolerancing per JEDEC MD-220
3. Contact plating: Sn

19 Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 1A	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

20 Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating -Matte Sn

21 Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- PFOS Free
- SVHC Free

22 Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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