PAC52411EVK1

PAC52411EVK1 Evaluation Module User's Guide

Overview

Qorvo's PAC52411EVK1 development platform is a complete hardware solution enabling users not only to evaluate the PAC52411 device, but also develop power applications revolving around this powerful and versatile ARM® Cortex®-M0 based microcontroller. The module contains a PAC52411 Power Application Controller® (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development the PAC52411EVK1 offers access to each and every one of the PAC52411 device's signals by means of a series of male header connectors.

The PAC52411EVK1 also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC52411's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control particular application features.

Finally, the PAC52411EVK1 module gives access to the PAC52411's SWD port allowing users to both program the application into the device's FLASH memory, as well as debug the application in real time. The provided 4 pin connector is compatible with a decent variety of SWD based debugger/programmer modules, widely available.

Qorvo's PAC52411EVK1 evaluation kit consists of the following:

- PAC52411EVK1 module
- ET-UARTSWD module with all cable assemblies
- PAC52411EVK1 User's Guide
- Schematics, BOM and Layout Drawings

Note: External SWD debugger/programming module required and to be provided by user.

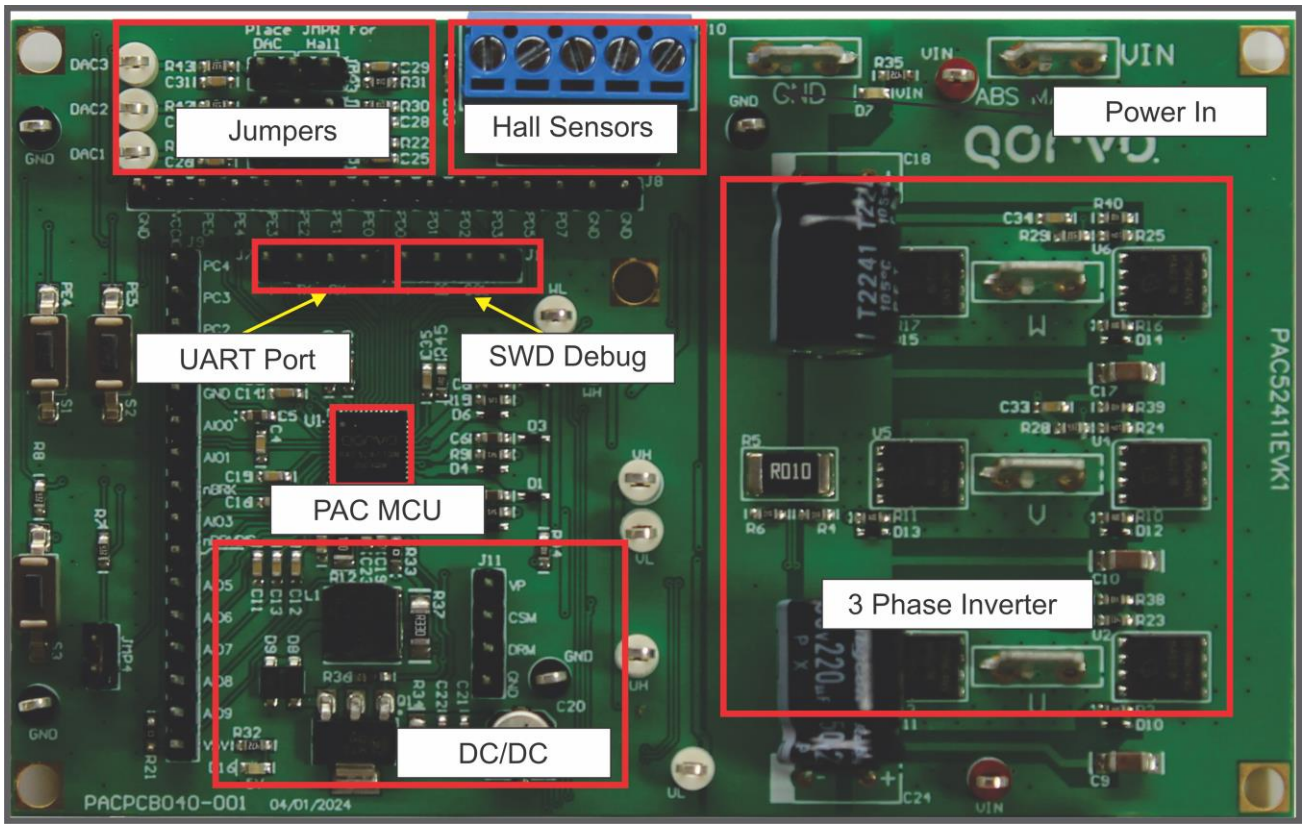


Figure 1: PAC52411EVK1 Block Diagram

Solution Benefits:

- Ideal for high voltage (up to 40V Abs Max) general purpose power applications and controllers
- Single-IC PAC52411 with configurable PWM outputs, ADC inputs, I2C, UART, SPI communication ports and GPIO.
- Gate driving for up to three half H Bridge (tri phase) inverter.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Qorvo's PAC52411EVK1 turnkey solution.

PAC52411EVK1 Resources

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC52411EVK1 evaluation module, as seen from above:

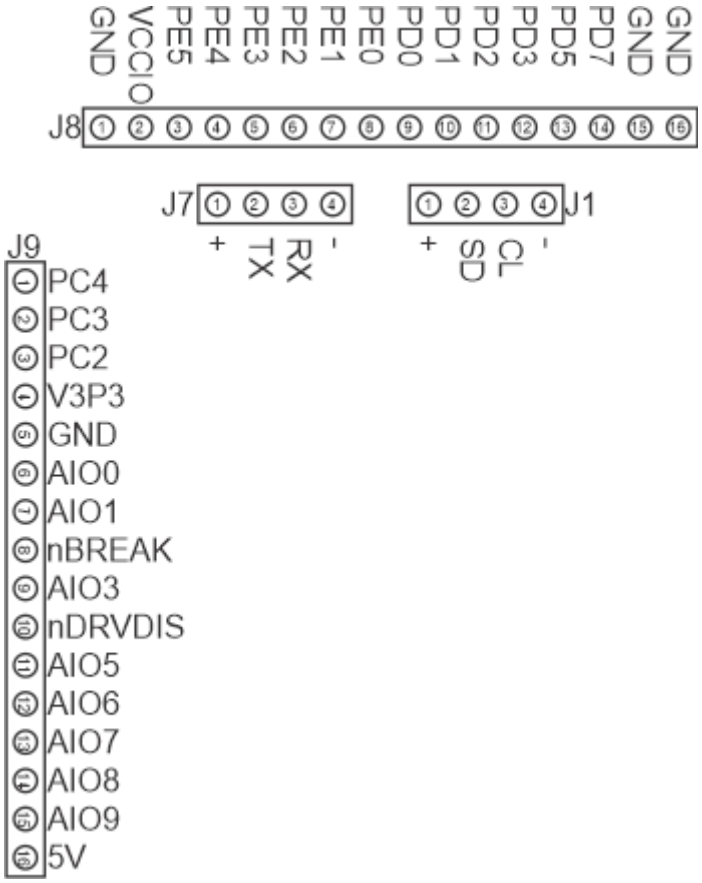


Figure 2 PAC52411EVK1 Headers and Test Stakes Pinout

Power Input

Power to the PAC52411EVK1 evaluation module can be applied to the VIN and GND spade connectors. Power to the PAC52411EVK1 evaluation module should not exceed 40V (Abs Max).

The PAC52411EVK1 is optimized to operate with voltages ranging from 14V to 24V Nominal (40V Abs Max). When the VIN input voltage goes above 8V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D16 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.2V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D16	VSYS (5V). Light up when the PAC52411 device is successfully powered up by VIN.
D7	VIN. Lights up as VIN voltage is applied.

SWD Debugging

Connector J1 offers access to the PAC52411 SWD port lines.

J1 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	SD	SWD Serial Data (PD0)
3	CL	SWD Serial Clock (PD1)
4	-	GND (System Ground)

Serial Communications

Connector J7 offers access to the PAC52411 UART port lines.

J7 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	TX	MCU Transmit Line (PE1)
3	RX	MCU Receive Line (PE2)
4	-	GND (System Ground)

Hall Sensor / DAC Interface

Terminal Block J10 offers access to the PAC52411 resources on PORTD utilized for hall sensor based commutation. These resources can be alternatively utilized as PWM DAC outputs for real time debugging. Jumpers JMP1/2/3 are used to select the preferred function.

NOTE: 2 pin shunts must be placed on the JMP1/2/3 in order for the respective PORTD resources to be made available.

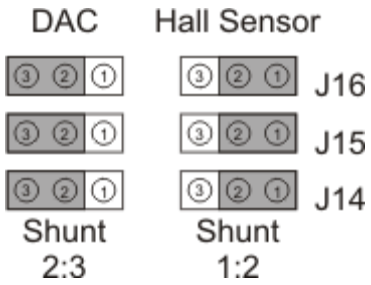


Figure 3 DAC / Hall Sensor Jumper Selection

Jumper JMP1/2/31	Description
1:2	Hall Sensor Functionality
2:3	DAC Functionality

NOTE: J10 and J12 functionality is only available when jumpers JMP1/2/3 have been shunted on the Hall Sensor respective position.

J10/J12 Pin	Terminal	Description
1	+	VCCIO (default is 5V)
2	Hall Sensor U	PORTD2
3	Hall Sensor V	PORTD3
4	Hall Sensor W	PORTD7
5	GND	GND (System Ground)

NOTE: Test stakes DAC1/2/3 are only available when jumpers JMP1/2/3 have been shunted on the DAC respective position

Test Stake	Description
DAC 1	PORTD2
DAC 2	PORTD3
DAC 3	PORTD7

PAC52411EVK1 Setup

The setup for the PAC52411EVK1 evaluation module requires up to four simple connections.

1. Connect the VIN power source via spade tab connectors VIN and GND. As VIN power is applied, the LED D7 will light up. Once VIN voltage goes above 8V, the PAC52411's Multi Mode Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D16 lighting up.
2. Connect the 3 Phase BLDC/PMSM motor via space tab connectors PHASE U, PHASE V and PHASE W.
3. If Serial Communications are desired, connect the USB to UART module 4 pin connection to J7.
4. For debugging/programming, connect a suitable USB SWD module to J1 by using a standard 4 wire cable.

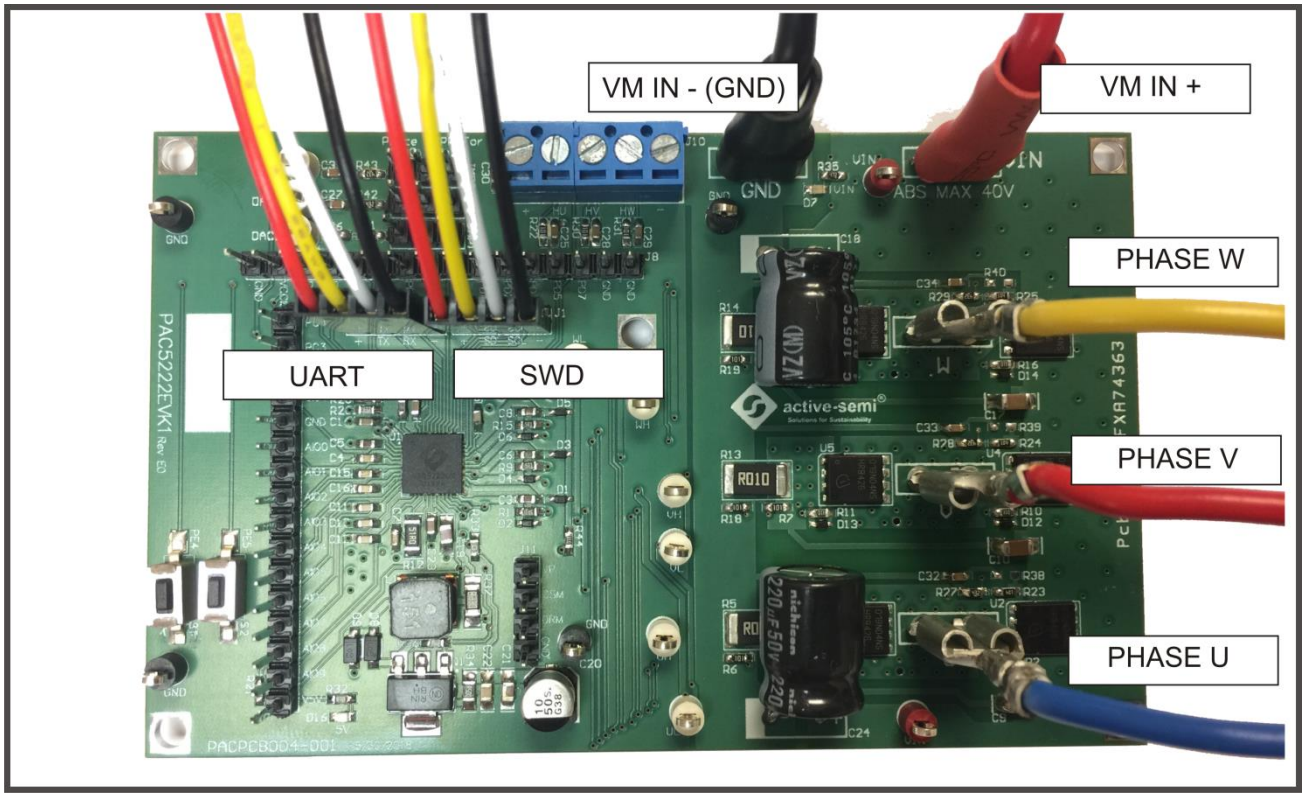
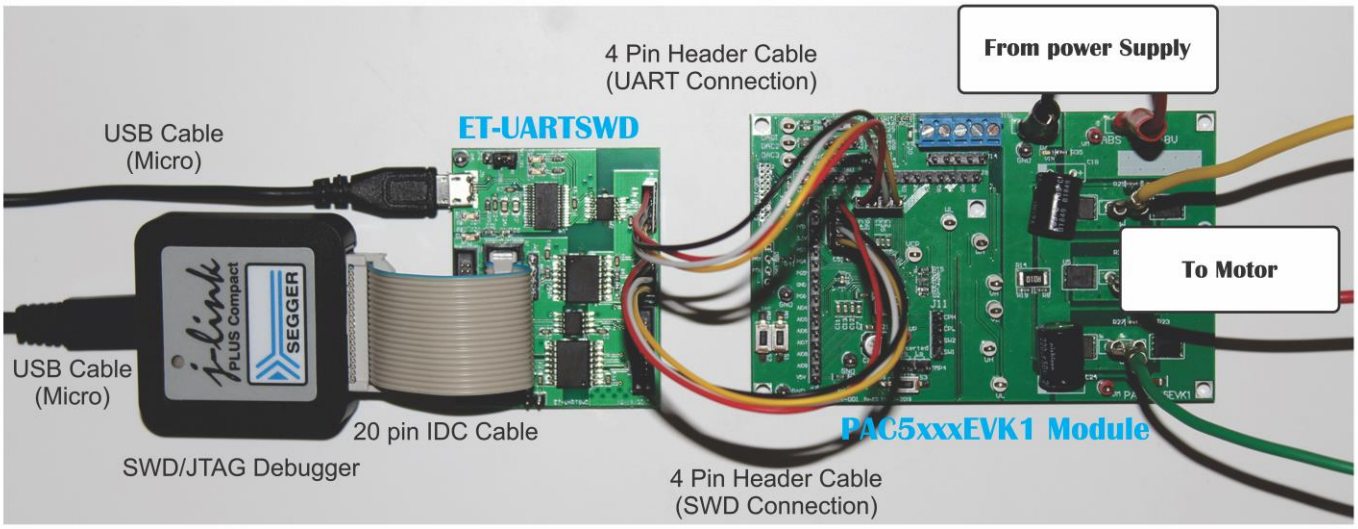
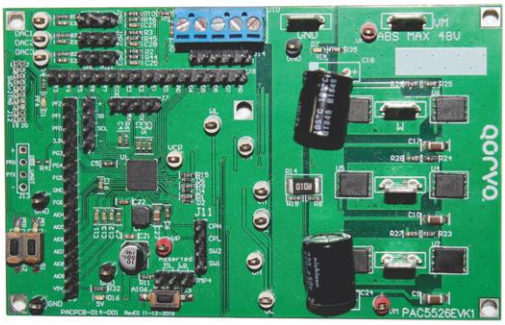


Figure 4: PAC52411EVK1 Evaluation Module Connections

TYPICAL PAC5XXXXEVK1 SETUP



PAC5XXXXEVK1 INCLUDED COMPONENTS



X1

PAC5xxxEVK1 Module

X1

ET-UARTSWD Module

X2

4 pin header cable

X1

USB Cable

REVISION HISTORY

Revision	Description
Rev 1.0	Initial draft

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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