JFET TOLL Demo Board User Guide

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Scope

This document explains the design and use of the demo board containing Qorvo® SiC JFETs in a TOLL package intended for semiconductor circuit protection and relay applications.

Caution

This document is provided as a user guide to install and operate the JFET TOLL demo board for characterization of JFET devices in TOLL package. The hardware system including the Graphic User Interface (GUI) and all accessories are designed for evaluating Qorvo JFET devices and for use in a lab environment by qualified power electronics technicians or engineers. Touching the demo board with high voltage applied can cause serious injury or even death. The hardware system is not designed to meet any specific safety standards nor production assembly qualification. The user should read the entire manual before using the demo board and exercise appropriate caution during its use.

Overview

The purpose of JFET TOLL demo board is to help semiconductor and relay manufacturers who are new to SiC JFETs to easily evaluate both the conduction and switching performance. The configuration is two parallel sets of a SiC JFET in series with a separate 30 V silicon MOSFET, driven by a single gate driver, as indicated in the block diagram of Figure 1. There are four total SiC JFET + Si MOSFET connected common source and in parallel. This is a bidirectional blocking circuit breaker or relay configuration, suitable for both AC and DC applications.

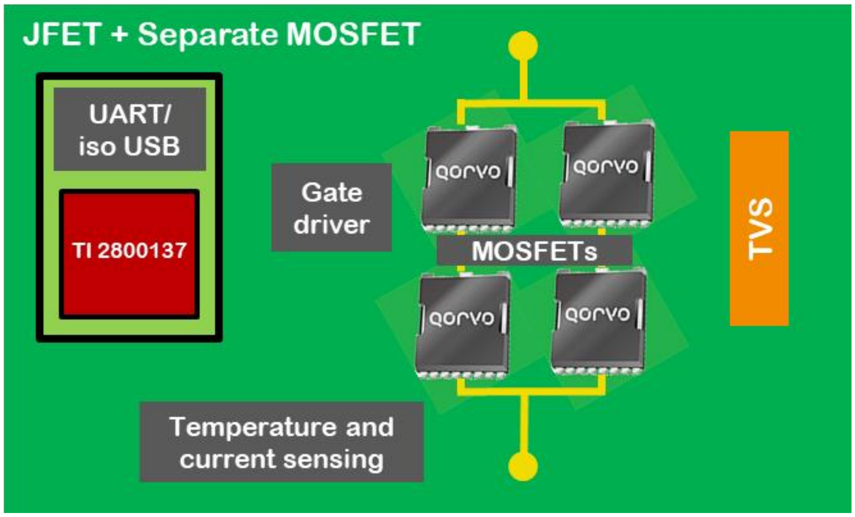


Figure 1 Four UJ4N075004L8S SiC JFET + Si MOSFET connected common source, two sets in parallel, with quasi-cascode drive

All the SiC JFETs and Si MOSFETs are driven by a single off-the-shelf gate driver. The control signal to the gate driver is from a Texas Instruments TMS320F2800137 control card. Alternatively, the control card can be left uninstalled, and an externally generated control signal brought in through test points. Total current and JFET temperature sense are provided by onboard circuitry. Finally, there is a transient voltage suppression block that contains RC snubbers and metal oxide varistors (MOVs) across the two power terminals. A 15 V DC power connection supplies power for the onboard electronics. The control card connects to a host computer by USB cable. A graphic user interface (GUI) provides an easy way to control and monitor the board functions. Each of these functions is described in more detail in this user guide.

Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
RMS Voltage	$V_{AC,rms}$			275	V_{rms}	Limited by MOVs
DC Voltage	V_{DC}			400	V	Limited by MOVs
RMS current	$I_{AC,rms}$			282	A_{rms}	Limited by current sensor
DC current	I_{DC}			±400	A	Amplitude limited by current sensor, duration limited by JFET and MOSFET temperature rise
Peak current	I_{peak}			±940	A	Limited by SiC JFETs
Operating temperature	T_{op}	-40		85	°C	Limited by switching regulator M1
Supply voltage	V_{supply}	13.5	15	16.5	V	Limited by isolated DC-DC M2
Control signal voltage range	$V_{control}$	-0.5		3.8	V	Limited by gate driver
Gate drive positive supply	V_{DD}		15		V	
Gate drive negative supply	V_{EE}		-5		V	
Analog voltages	V_{analog}	0		3.3	V	Measurement range of control card ADC

Table 1 Specifications for the JFET TOLL demo board

Power Circuit

Figure 2 shows the power circuit, or the circuit that switches on or off to allow current to flow freely or to block its flow regardless of the voltage polarity across the power terminals. The gate driver is a Texas Instruments UCC5304 single-channel isolated driver. Other gate drivers from various manufacturers would also work. The RC filter and pulldown resistor at the input of the gate driver are optional but a recommended best practice. The gate driver and its power supply are isolated, but the common source point is used as ground for the control card and all other circuitry.

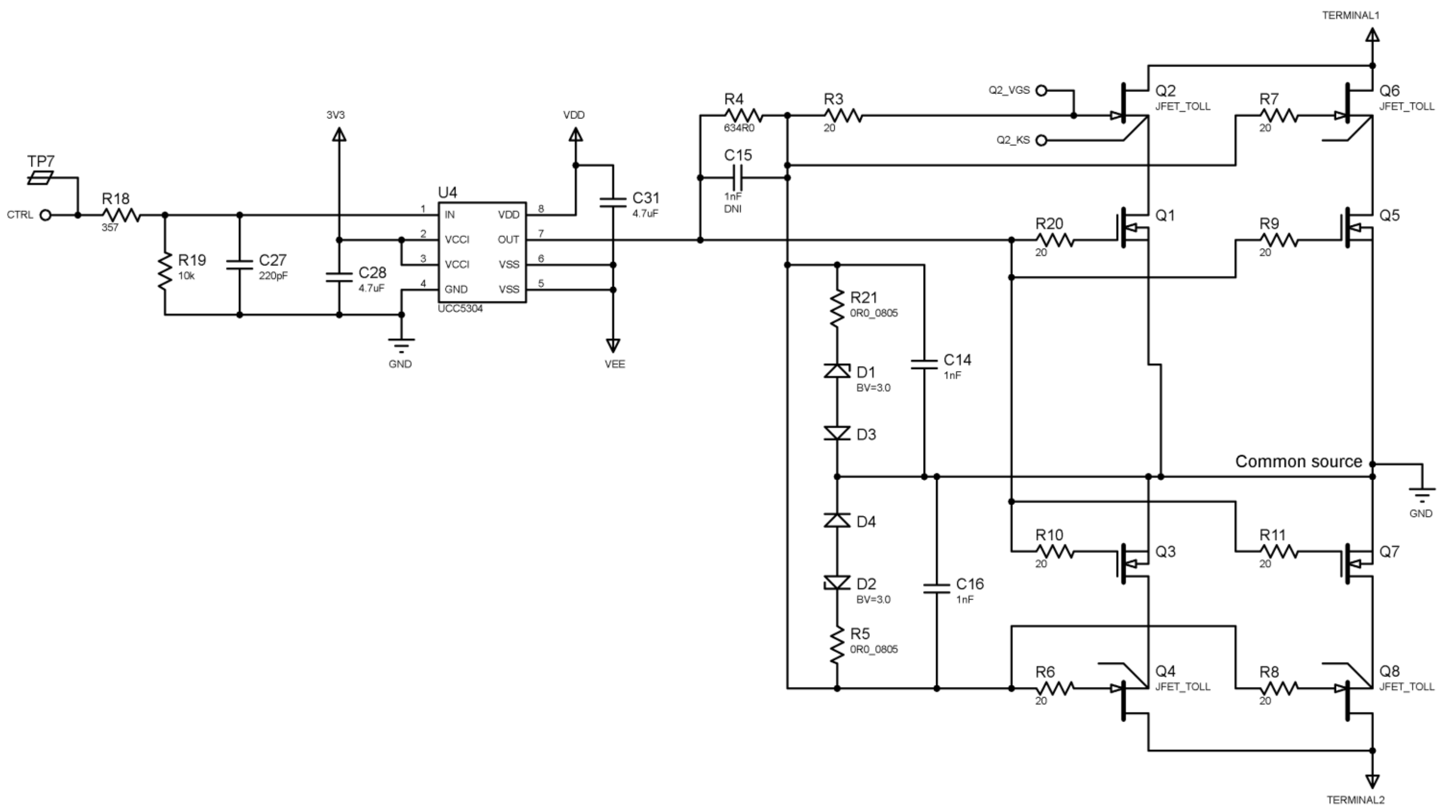


Figure 2 Four UJ4N075004L8S SiC JFET + Si MOSFET connected common source, two sets in parallel, with quasi-cascode drive

The resistor R4 is the “overdrive resistor”, labeled R_ODV in the JFET User Guide. The gate driver’s power supply voltages are +15/-5 V. With +15 V on-state voltage from the gate driver, and V_{GS} of each JFET at about 2.3 V, there is about 1.7 V across R4, and the current into each JFET is close to 5 mA. This is a good compromise between gate drive power consumption and temperature sense noise immunity. Note that R4, the overdrive resistor, is only in line with the JFET gates, and not with the Si MOSFET gates.

The speedup capacitor C15 is unnecessary and therefore not installed.

There is a 20 Ω resistor at the gate of each JFET and MOSFET. This value yields reasonable switching speed for a circuit breaker or relay. For faster or slower switching, you can decrease or increase the JFET gate resistance, respectively. Take caution however to avoid switching too fast, which creates high dV/dt transients that are challenging to absorb, or switching too slowly, which can put too much energy from line inductance into the JFETs or MOSFETs.

The damping resistors R21 and R5 are unnecessary and therefore populated with 0 Ω resistors.

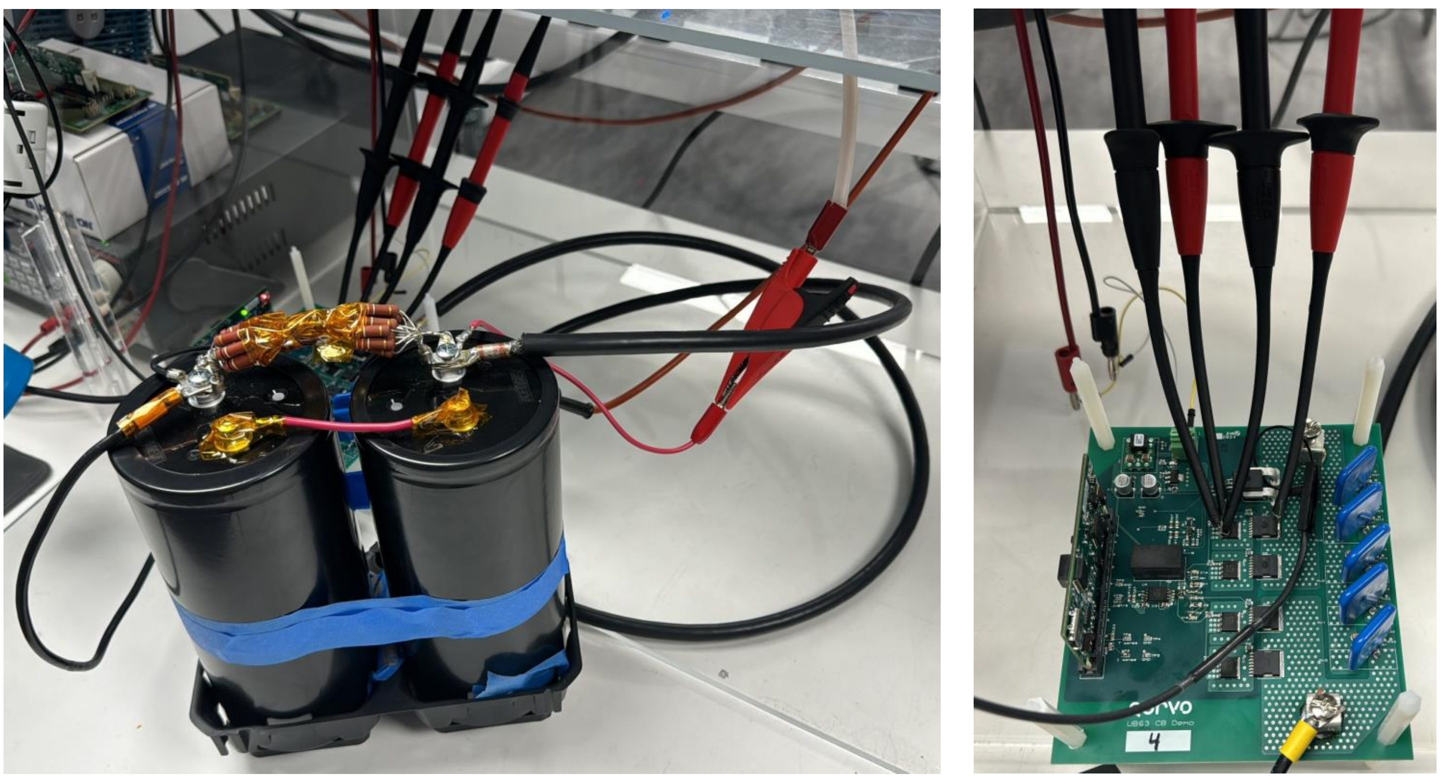
Zener diodes D1 and D2 enable both overdriving the JFET gates and cascode switching of the JFETs. When switching off, the Zener diodes avalanche at about 3 V, allowing JFET gate discharging current to flow to the common source. As the MOSFET V_{DS} exceeds the JFET threshold voltage magnitude plus the Zener BV, then the JFET switches off. This is similar to cascode operation, hence the name quasi-cascode. There is no need to worry about JFET versus MOSFET switch timing. The JFET automatically switches with the MOSFET. When off, diodes D3 and D4 prevent current from flowing from common source into the gate driver and wasting gate drive power. When switching on, D3 and D4 force the gate charging current to flow through R4, which has high resistance. Therefore, turnon is slow, as is usually desirable in circuit breakers and relays. For faster switch-on, simply short D3 and D4. In this case, JFET gate charging current during switch-on flows forward through the Zener diodes as in cascode mode. Also, adding a diode in series with R4 prevents any current into the gate driver from wasting gate drive power.

The gate ringing suppression capacitors C14 and C16 are optional but recommended.

The silicon MOSFETs Q1, Q3, Q5, and Q7 are 30 V rated, part number SQJQ130EL-T1_GE3 from Vishay. Other 20 to 30 V rated MOSFETs will also work fine. Note however that switching off current with sufficient voltage developing across the power terminals will cause the MOSFETs to avalanche. The avalanche duration depends on energy stored in line inductances and on the JFET gate resistance value, with higher gate resistance resulting in longer avalanche duration. Switching at AC zero crossings always minimizes stress on both the JFETs and MOSFETs, but during an emergency, it may be impractical to wait for a zero crossing before switching off. Therefore, the MOSFET must have good avalanche energy capability.

Switching Tests

Switching tests were made on a JFET TOLL demo board. The test setup is shown in Figure 3, with a large capacitance bank supplying the switching energy in (a), and in (b) a differential probe measuring a MOSFET V_{GS} and another measuring a JFET drain to common source voltage. Pins were soldered to the MOSFET gate, MOSFET source (common source point), and JFET drain to attach the differential probes to. Current sensing is by a Rogowski probe.



(a) (b)

Figure 3 UJ4N075004L8S demo board test setup (a) capacitor bank, (b) probes on demo board

Current was ramped up to 1176 A through a demo board by applying 70 V across an 8 AWG wire-180 cm long with about 2.5 µH inductance. This is effectively an unclamped inductive switching (UIS) setup. The resulting waveforms are shown below in Figure 4.

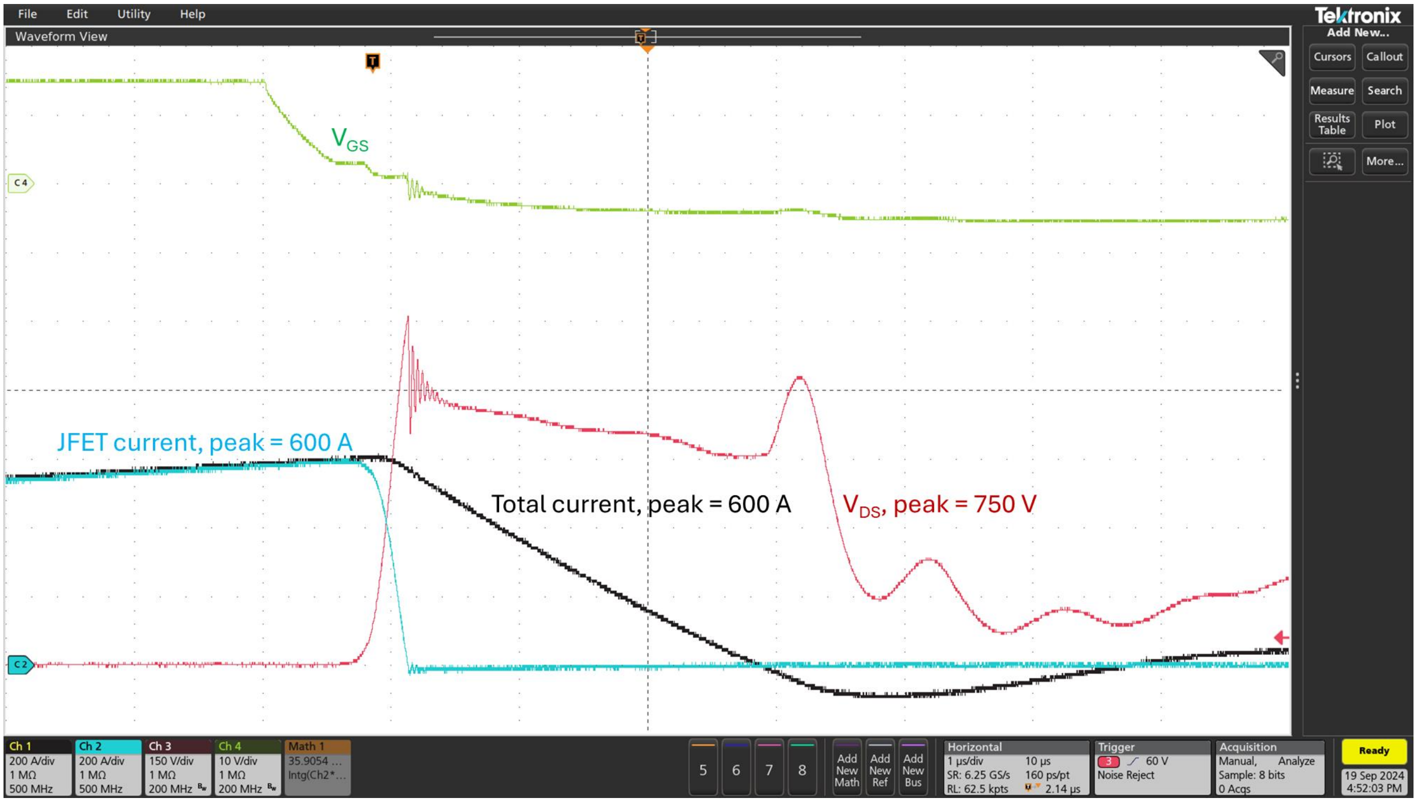


Figure 4 Switching waveforms for the JFET TOLL demo board

The top waveform, Ch 4, is the gate-source waveform of a forward-conducting MOSFET, driven from -5 to 15 V. The Ch 2 (light blue) waveform shows current flowing through the JFETs and MOSFETs, excluding current through the MOVs and snubbers. Ch 1 (black) waveform is the total current into the board, so JFET and MOSFET plus MOVs and snubbers. Ch 3 (red) is the JFET drain to MOSFET source (common source point). During switching off, JFET current and the total current decrease smoothly, while simultaneously the JFET drain to common source voltage rises to a peak of 750 V. At that time the JFETs are off, and the JFET drain voltage settles with some ringing, as expected, especially with differential probes. The MOVs absorb energy from the cable inductance until the total current is nearly zero, after which there is normal ringing between the cable inductance and test system capacitances.

Temperature Sense Circuit

The temperature sense circuit is a simple differential amplifier connected to the gate and Kelvin-source terminals of one of the JFETs, Q2. It has unity gain and an output voltage range of 1.84 to 2.62 V corresponding to a temperature range of 175 down to -55 °C with I_G = 5 mA for the UJ4N075004L8S JFET. The voltage swing is 0.78 V over the entire temperature range. With a 100 °C change in temperature, the voltage at the analog to digital converter (ADC) changes 0.34 V. The ADC has an input voltage range of 3.3 V. Using such a small portion of the ADC input voltage range causes noise susceptibility, so the control card digitally filters the V_{GS} measurement.

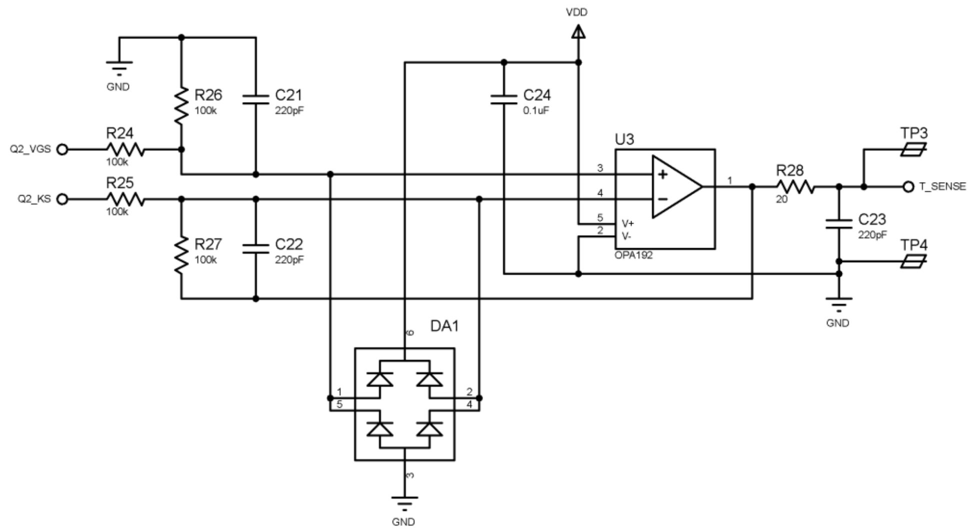
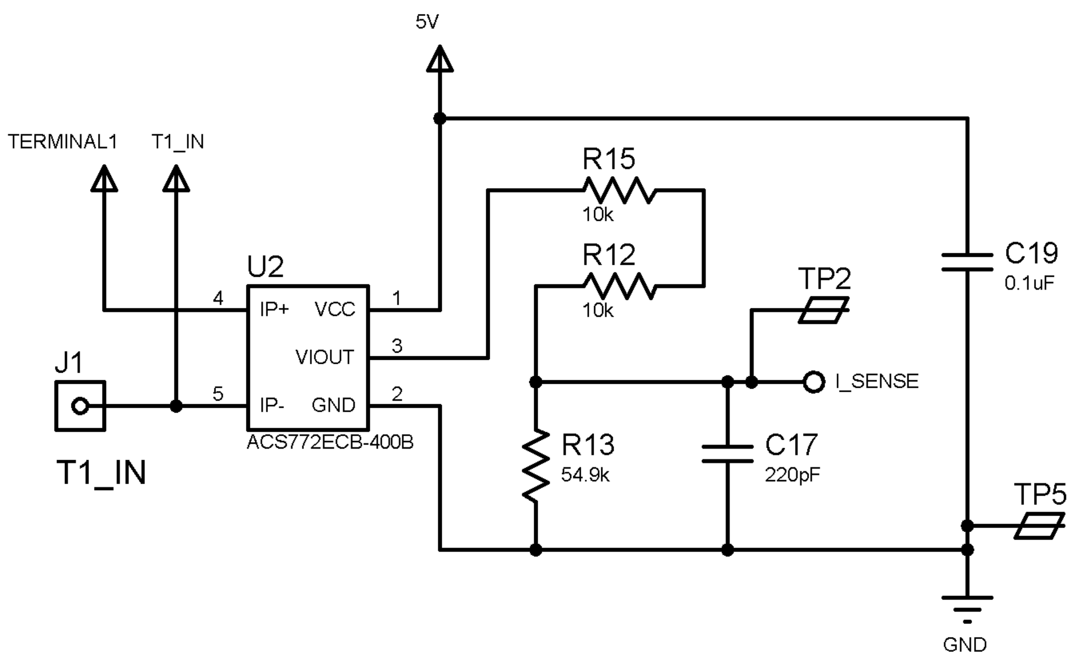


Figure 4 JFET on-chip temperature sense circuit

The op-amp U3 is a precision op-amp from Texas Instruments, part number OPA192. Other precision op-amps will also work fine. The diode array DA1 clamps the op-amp input signals to its power supply rails. C23 is needed by the ADC in the control card and must be placed close to the ADC input.

Current Sense Circuit



3.2984V = 400A, 0.3665V = -400A, 1.8324V = 0A

Figure 5 current sense circuit

The current sense circuit includes a Hall-effect sensor from Allegro, part number ACS772ECB-400B-PFF-T. It has a current sense range of ±400 A. With such a wide current sense range, accurately sensing currents below about 10 A is challenging. Response to a step change is typically 2.5 µs, which is slow. This current sensor is included on the demo board for convenience only. It is not used for overcurrent or short circuit detection with automatic switch-off of the JFETs.

An arguably better current sensor type is a current sense resistor combined with a precision differential amplifier. Even better is to use the JFET itself as the current sensor, as explained in the JFET User Guide. This approach was developed after this demo board was designed.

Operating Instructions

Board Connections

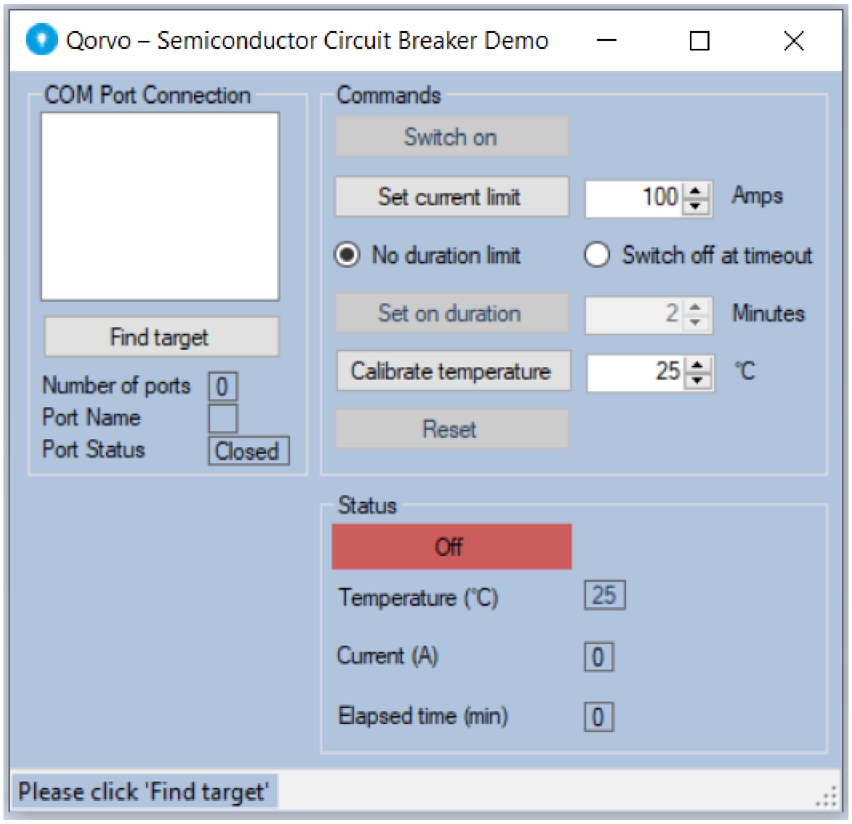
Figure 5 current sense circuit

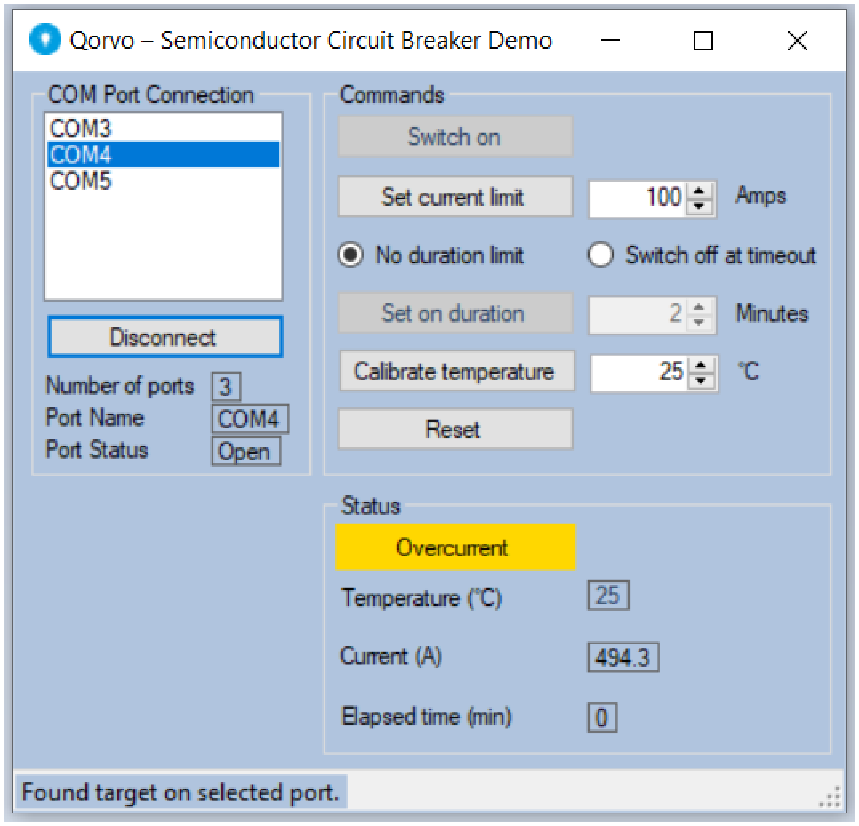
1. If using the Texas Instruments TMS320F2800137 control card, insert it into its connector and push in the latches to lock it into place. Otherwise, connect your controller to the board using the test point labelled CTRL and a GND test point.
2. Connect a benchtop power supply to the spring terminal block, as shown in Figure 5. Set the power supply to 15 V. You can set the current limit to 0.5 A. Current consumption is typically less than 0.1 A.
3. Connect your test load to the power terminals with SAE #10 machine screws or 5 mm bolts.

GUI Instructions

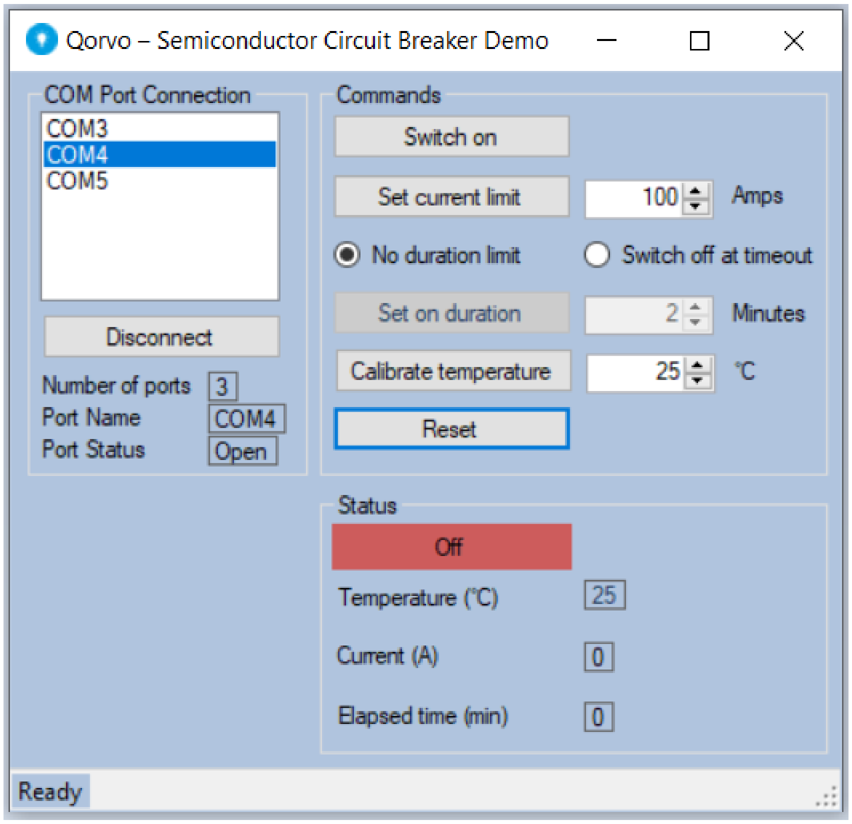
The GUI requires Microsoft .NET 4.8 or higher framework installed to run. Most PCs have this installed by default. The operation of the GUI is explained by the following stepwise instructions.

1. Connect a USB-C cable between the Texas Instruments control card and you computer.
2. Apply 15 V power to the demo board. This powers the gate drive and other circuitry.
3. Run the GUI and click the 'Find target' button.

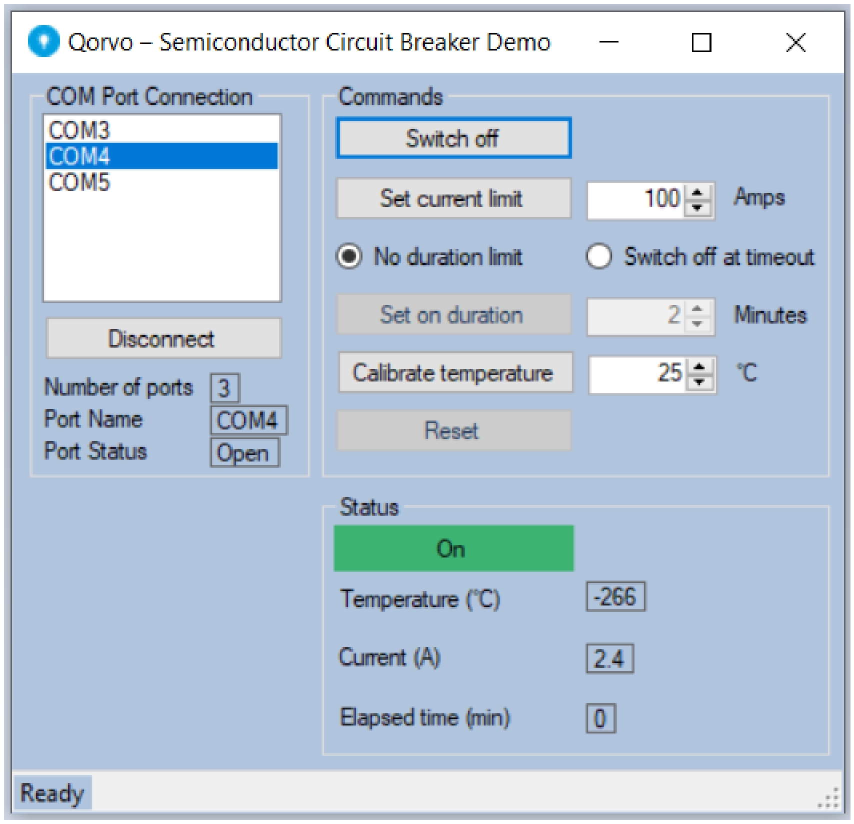




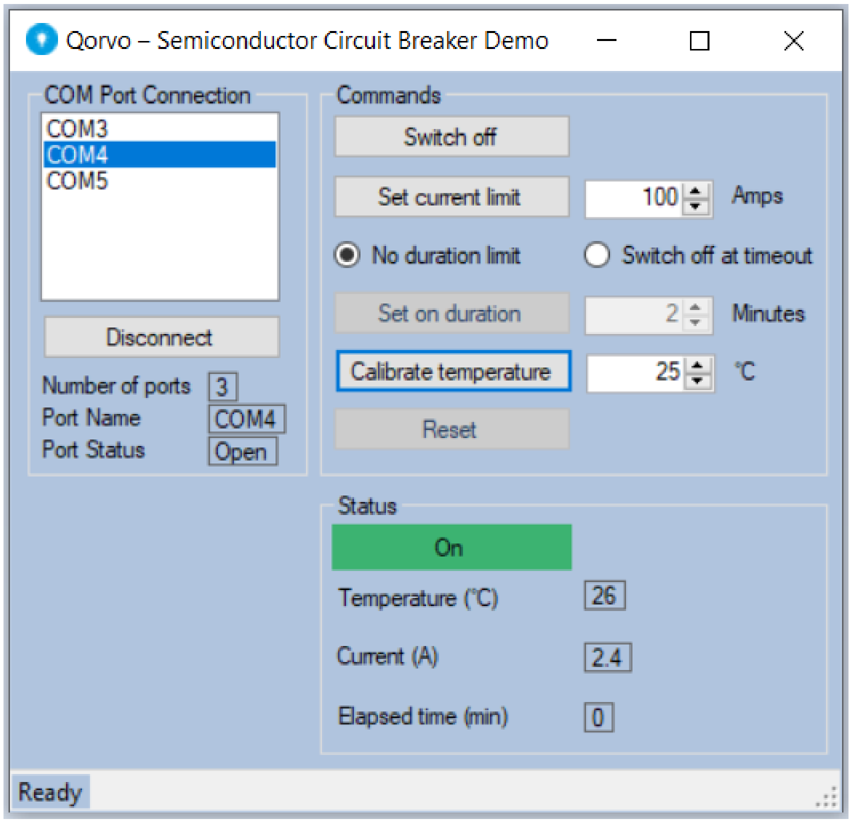
2. The GUI "talks" with the control card and automatically finds the correct COM port. The 'Find target' button text changes to 'Disconnect'. You will probably see an 'Overcurrent' warning. Ignore this and click the 'Reset' button. This clears the error and simultaneously calibrates the current to zero.



3. Click the ‘Switch on’ button to switch on the power semiconductors. This will enable temperature sensing.



4. Enter the temperature of the board (usually room temperature) in °C, then click the 'Calibrate temperature' button.



5. Current sensing is not fully supported at this time due to limited accuracy and response time, but you can see changes in current. It is best to set the current limit well above your expected operating current range. JFET temperature sensing is usable. You can have the controller automatically switch off the power semiconductors after a certain length of time by clicking the 'Switch off at timeout' radio button and then setting the desired duration.