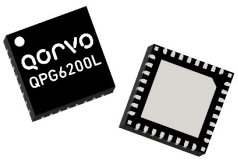
QPG6200L

Multi-Protocol SoC

Data Sheet



1 Product Overview

The QPG6200L is the industry's most reliable and robust wireless multi-standard System-on-Chip. Featuring Qorvo's ConcurrentConnect™ technology, the QPG6200L supports the latest standards for Matter (over Thread), Zigbee and Bluetooth® Low Energy in a truly concurrent way.

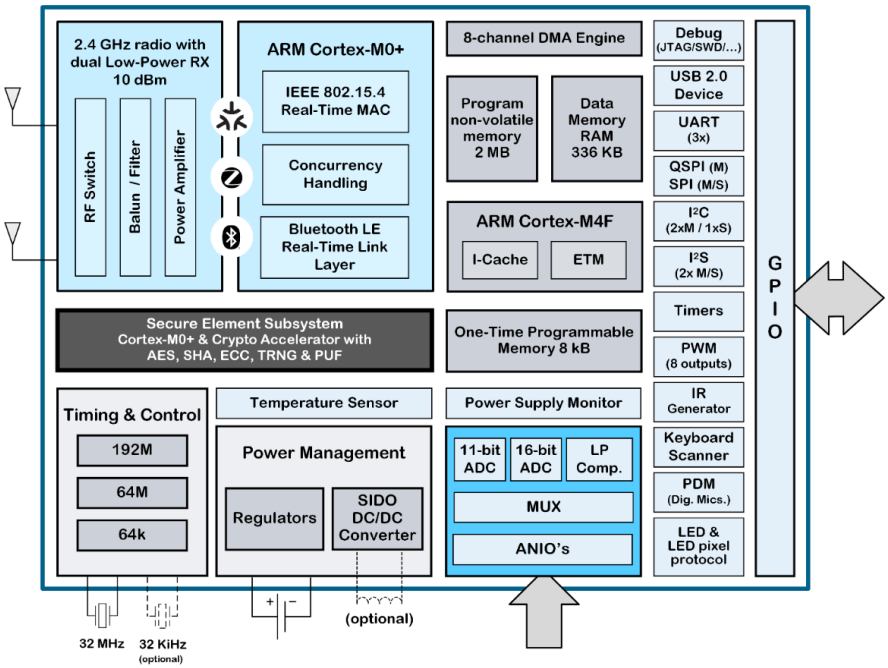
The low-power QPG6200L enables the adoption of Matter while supporting existing Zigbee networks without tradeoffs in latency and link performance.

Featuring ConcurrentConnect™ Technologies:

- **Antenna Diversity for Bluetooth Low Energy and IEEE 802.15.4 enables increased effective range and interference robustness.**
- **Multi-Radio capability allows continuously scanning for incoming packets across Bluetooth Low Energy and IEEE 802.15.4 protocols with no observable blind spots.**
- **Multi-Channel capability allows operating in up to 3 IEEE 802.15.4 PANs on different channels.**

- Integrated Secure Element Subsystem featuring:
  - Secure Boot (rooted in ROM with Boot Keys in OTP)
  - Secure Storage (PUF-based)
  - Secure Provisioning
  - Secure Debugging
  - Secure Device Attestation.
- Designed and optimized for low-power IoT end node applications such as:
  - Connected Lighting
  - Smart Sensors
  - Wearables
  - Gateways.

2 Functional Block Diagram



3 Key Features

Radio
- ✓ 2.4-GHz RF Transceiver compliant with: Bluetooth Low Energy v 5.4 and IEEE 802.15.4 for wireless personal area networks (WPAN).
- ✓ Preamble-based Antenna Diversity for Bluetooth Low Energy and IEEE 802.15.4
- ✓ IEEE 802.15.4 Packet-in-Packet resync.
- ✓ Transmitter output power programmable in 1 dB steps, stable over voltage and temperature
- ✓ Integrated RF filter and matching
- ✓ Compliant with worldwide RF regulations: ETSI EN 300 328 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T-66 (Japan)

Real-Time Bluetooth Low Energy Controller
- ✓ Bluetooth v 5.4 compliant LE Controller
- ✓ Enhanced data rate (2 Mbit/s)
  - ✓ Long Range Coded PHY
  - ✓ Link Layer Privacy
  - ✓ Advertising Extensions
- ✓ Full connection utilization

Real-Time 802.15.4 Medium Access Control
- ✓ IEEE 802.15.4-compliant MAC
- ✓ Automatic ACK handling and retransmissions
- ✓ Address recognition and packet filtering

Multi-Protocol Support
- ✓ Hardware accelerated Dynamic Multi-Protocol Bluetooth Low Energy and IEEE 802.15.4 Communications

Secure Element Subsystem
- ✓ Dedicated microcontroller for Secure Element operation
- ✓ Hardware accelerated AES and CCM/CCM* encryption and decryption with 128, 192 and 256-bit keys
- ✓ Hashing engine: SHA-128, SHA-2 (SHA-256, SHA-512)
- ✓ Public Key Crypto: Elliptic Curve; Support for ECDSA, ECDH, P256, Curve25519, J-Pake, ECMQV, EdDSA, etc.
- ✓ Support for PUF (Physical Unclonable Function)
- ✓ Secure boot from ROM with boot keys in OTP
- ✓ Cryptographic Random Number Generator.

Integrated Application Microcontroller
- ✓ Arm Cortex-M4 processor with DSP functionality
- ✓ Up to 192 MHz clock speed
- ✓ ETM Trace

Memory
- ✓ 2048 kB Non-Volatile Memory (RRAM), of which 8 kB is One-Time Programmable
- ✓ 336 kB Low Leakage Retention RAM 16-channel DMA Engine

Peripherals and Interfaces
- ✓ 14 programmable GPIO lines (up to 7 more when swapped with other pins, 4 of these are input only)
- ✓ 2 analog input lines
- ✓ 16-bit high-resolution and 11-bit GP ADC
- ✓ Temperature sensor
- ✓ Timers: 6x 32-bit or 12x 16-bit
- ✓ PWM Engine for 8 outputs
- ✓ LED Generator (8-bit PWM) with fading support for 4 signaling LEDs
- ✓ LED Pixel Protocol Master (RTZ) for dynamic control of LED light strips
- ✓ USB 2.0 Device supporting Full Speed (12 Mbit/s) data rate
- ✓ 2x PDM Microphone Interface
- ✓ 1x SPI Master and 1x SPI Slave interface
- ✓ 2x I^2C Master and 1x I^2C Slave interface
- ✓ 2x I^2S Master/Slave interface for digital audio devices
- ✓ 3x UART interface
- ✓ Keyboard Scanner
- ✓ IR Generator; High Drive Sink for IR

Power Management
- ✓ Operating voltage range: 1.71 ... 3.6V
- ✓ Integrated Regulators
- ✓ Integrated SIDO DC/DC Buck Converter
- ✓ Low power Sleep modes:
  Using internal LjRC oscillator: 0.9 µA
  Using 32 MHz crystal oscillator: 200 µA
- ✓ Data and state retention in all Sleep modes

Dimensions and Layout
- ✓ QFN32: Quad Flat No-lead package, 32 pins, 4x4 mm.
- ✓ No RF shielding required.

4 Ordering Information

Table 1: Ordering and Packing Information

Part Number	Chip Package	Tx Power	Stnd. GPIO+ ANIO Lines	Optional extra GPIO Lines (*)	Packing	Unit Qty	Box Dimensions (interior), [mm]
QPG6200LTR13	QFN32	10 dBm	14+2	7	13” Tape & Reel	4000	337x337x27
QPG6200LSR					Sample Reel	100	370x160x80

(*) see section 7.1 for details.

All QPG6200L part numbers contain 2 MB NVM (incl. OTP) and 336 KB RAM.

For ordering the QPG6200LDK-01 (IoT Dev Kit for QPG6200L) please refer to Qorvo’s website.
See also section 8.9 and 13.

5 Contact Information

Technical support:
www.qorvo.com/support/technical-support

all around you

Sales:
www.qorvo.com/support/how-to-buy/contact-a-sales-rep

A 3-page QPG6200 Product Brief is available on Qorvo’s website.

Table of Contents

6 Radio and Communication Protocols

6.1 2.4 GHz Radio

The QPG6200L radio transceiver provides all the functionality for the Physical layer (PHY) for both IEEE 802.15.4 and Bluetooth communications. The transceiver contains a highly configurable pulse shaping filter that can be used for both Bluetooth Low Energy and 802.15.4 transmission.

This section describes the generic features; following sections describe the specific features for IEEE 802.15.4 and Bluetooth.

6.1.1 RF Ports with Integrated Baluns and Filter

The antenna ports output is 50 Ω single ended.

6.1.2 Radio Configurations

The QPG6200L supports different radio configurations. It can be configured to use a different receive and transmit antenna. Antenna Diversity configuration is also possible for both Bluetooth Low Energy and IEEE 802.15.4 communications (see section 6.1.5). Two sample configurations are depicted below, but others are also possible.

Sample Configuration 1 (Figure 1):

- Single ended 50 Ω antenna.
- Using antenna 0 (RF0 pin) for both RX and TX.
- Antenna diversity disabled.

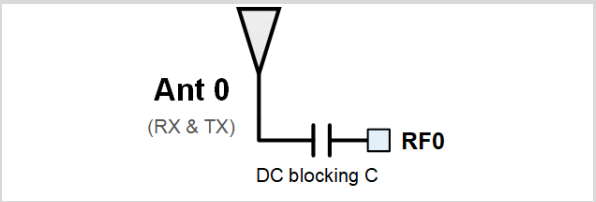


Figure 1: Single Antenna

Sample Configuration 2 (Figure 2):

- 2 single-ended 50 Ω antennas.
- Antenna diversity enabled. TX on same antenna as was selected best by RX.

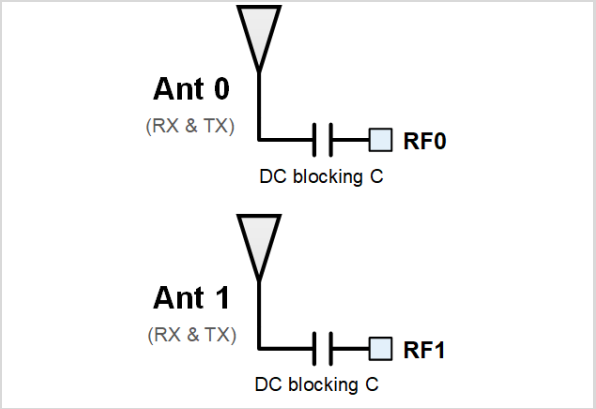


Figure 2: Two Antennas

6.1.3 RSSI

The PHY's RSSI circuitry measures the received signal energy level and this value is converted to dBm values in the Hardware Abstraction Layer (HAL). See Table 15 for the range and accuracy.

RSSI data is available for both Bluetooth Low Energy and IEEE 802.15.4 communication.

6.1.4 Transmit Power Control

The transmitter output power is configured by software, in steps of 1 dB.

6.1.5 ConcurrentConnect Antenna Diversity

Preamble based antenna diversity enables the PHY to choose the optimal antenna for every individual packet and increases the performance of the receiver in environments that are dominated by multipath fading effects and interference situations. In receive mode the PHY selects the antenna based on the best signal quality (signal-to-noise/interference ratio).

For typical indoor usage in an environment with 50 ns delay-spread and 2 MHz signal bandwidth using the Rayleigh fading model, antenna diversity with 2 antennas results in a ~8 dB improved link budget (at a 1% outage probability) compared to no antenna diversity. This translates into 70% more reliable range (using a log-distance breakpoint model[1] with path loss coefficients g1=2 (free space propagation) and g2=3.5 above the breakpoint at 10 m).

Unless configured otherwise, the QPG6200L will use the same antenna for transmission as the one that was used for the reception of the last packet.

[1] Refer to "T.S. Rappaport, Wireless Communications – Principles & Practice, Prentice Hall, 1996" for this model.

6.2 IEEE 802.15.4 Communications

6.2.1 2.4 GHz IEEE 802.15.4 Transceiver

The QPG6200L radio is compliant with the IEEE 802.15.4 2020 standard.

The QPG6200L supports all the IEEE Standard 802.15.4 defined channels in the 2.4 GHz ISM license-free frequency band (channels 11 .. 26).

The channel number (k) and center frequency (F_c) relate as follows: $\boldsymbol{F_c = 2405 + 5(k - 11)}$ [MHz]

6.2.2 Real-Time Medium Access Control (MAC)

The QPG6200L implements the 2.4 GHz OQPSK-required MAC features of the IEEE Standard 802.15.4 used by Thread/Matter and Zigbee (including Zigbee RF4CE). The MAC provides a packet-level service to the protocol stack, and handles packet transmissions and receptions autonomously, including:

- Performing CSMA/CA to avoid collisions when transmitting packets;
- Adding CRC and Sequence number;
- Acknowledgement handling for transmitted packets, including automatic retransmissions;
- Address recognition and packet filtering on received packets, including CRC checking;
- Acknowledgement handling for received packets, including automatic acknowledge transmission.

6.2.3 Link Quality Indication

In addition to the RSSI, there is also a link quality indication (LQI) determined for each received IEEE 802.15.4 data packet, for use at the network and application layers.

6.2.4 Clear Channel Assessment (CCA)

The PHY can perform a clear channel assessment (CCA) to avoid collisions. The IEEE 802.15.4 standard defines 3 CCA methods; the QPG6200L supports:

- CCA mode 1, **Energy Detect (ED)**: the medium is considered busy when the measured energy in the selected channel is above a certain threshold. This CCA threshold is programmable.
- CCA mode 3, **Energy Detect (ED) and Carrier Sense (CS)**: the medium is considered busy when a valid IEEE 802.15.4 carrier is detected in the selected channel and the measured energy in the selected channel is above the programmable threshold.

6.2.5 Packet-in-Packet Resynchronization

If the QPG6200L is receiving a packet from one node and is interrupted by the reception of another stronger packet from another node, the receiver will resynchronize to the latter and continue to receive and process this packet. This allows one packet (the strongest) to be received where otherwise both packets would have been lost. Packet-in-Packet collisions can occur in situations when neighbor network packets are received at a low level and in hidden node situations where not all nodes can see each other.

6.3 Bluetooth Communications

The QPG6200L implements the Bluetooth Low Energy (LE) Controller functionality, including PHY, Link Layer and HCI according to the Bluetooth Core Specification v 5.4 for Bluetooth Low Energy. When combined with a Bluetooth Low Energy Host Stack, it supports all GATT-based profiles and services, and it can operate as a Broadcaster, Observer, Central and Peripheral device.

6.3.1 2.4 GHz Bluetooth Low Energy PHY Layer

The QPG6200L implements the Bluetooth LE PHY layer, supporting all the (40) Bluetooth defined frequency channels in the 2.4 GHz ISM license-free frequency band.

The Bluetooth LE Controller supports the basic data rate of 1 Mbit/s, the enhanced data rate of 2 Mbit/s, as well as the Long Range Coded PHY data rates of 125 kbit/s and 500 kbit/s.

6.3.2 Real-Time Bluetooth Low Energy Link Layer

The Real-Time Link Layer implements the real-time functions of the Bluetooth LE Link Layer (LL) protocol for the Advertising, Scanning, Initiating and Connection States. Multi-state operation is supported: a multi-level priority mechanism ensures appropriate scheduling of Advertising, Scanning, Initiating and Connection-events.

In the Connection State, the Real-Time Link Layer maintains the LE Asynchronous Connection-oriented Logical (LE ACL) transport on master and/or slave connections, allowing transfer of control (LE-C) and user (LE-U) data. High-throughput applications are supported via a dedicated queue per (LE ACL) connection, thus ensuring efficient filling of Connection Events.

The maximal PDU size supported is 261 bytes (resulting in a full PDU payload size of 255 bytes). Together with 4 bytes of access code and 3 bytes of CRC, this gives a total packet size, excluding preamble, of 268 bytes.

The QPG6200L supports the Link Layer Privacy and Advertising Extensions as defined in the Bluetooth Core v 5.4 Specification.

6.3.3 Full Connection Utilization

The QPG6200L has been optimized for audio streaming over Bluetooth Low Energy with a full Bluetooth connection utilization under high CPU load conditions. This implies that the system can fill the complete connection with Bluetooth packets allowing to achieve the maximal bandwidth of the connection, even when the CPU is processing audio (decimation, equalizing, compressing), under a large variety of Bluetooth connection configurations; normal data and high data rate, short and long connection intervals, short and long Bluetooth packets.

6.4 Multi-Protocol Stack Support

The QPG6200L can support multiple protocol stacks. IEEE 802.15.4 based stacks can interface simultaneously with the QPG6200L MAC API through a MAC Dispatcher, while the Bluetooth Low Energy Stack can interface with the QPG6200L at the HCI level at the same time.

6.5 HW-Accelerated Dynamic Multi-Protocol Support

The QPG6200L has HW support to seamlessly interleave Bluetooth Low Energy communications (advertisements and Bluetooth connections) with IEEE 802.15.4 communications for applications that support dual mode communication (e.g., Bluetooth Low Energy / Thread). The Dynamic Multi-Protocol Support lets the IEEE 802.15.4 MAC autonomously schedule and interleave IEEE 802.15.4 traffic to ensure that Bluetooth connection traffic is maintained without any connection drops.

For use cases where more airtime is needed for Bluetooth data transfers, the following additional modes are supported:

- **Best effort mode**, for non-real time (bulk) Bluetooth data transfers, where the Bluetooth LE controller frees up airtime in the connection when an IEEE 802.15.4 data packet is queued.
- **Controlled bandwidth mode**, for real time (streaming) Bluetooth data transfers, where the Bluetooth LE controller reserves a configurable portion of the connection for IEEE 802.15.4 communication.

> **! This feature can be combined with ConcurrentConnect Multi-Channel Support to support three IEEE 802.15.4 stacks (each on its own channel), while simultaneously acting as a Bluetooth Low Energy peripheral and maintaining a Bluetooth connection with a smartphone.**
>
> This can also be combined with ConcurrentConnect Multi-Radio, allowing to combine Bluetooth LE scanning and 802.15.4 RX ON.

6.6 Coexistence Interface

This Interface can be used to enable coexistence of the QPG6200L radio with other potentially interfering radios (Bluetooth, Wi-Fi) within the same device. This enables the following features:

- Avoid RX desensitization of the QPG6200L radio when another radio within the same device would transmit while the QPG6200L radio is in receive mode.
- Avoid RX desensitization of another radio within the same device when the QPG6200L radio would transmit while the other radio is in receive mode.
- Allow the QPG6200L radio and the other radios within the same device to share the same transmit frequencies (TX channel overlap).

Radio coexistence is controlled by an arbiter, that may grant a radio access to the medium depending on the state of the other radios and assigned priorities. The QPG6200L contains an arbiter but can also use an external arbiter. The Coexistence Interface is user-configurable, and has two modes of operation:

Master : The internal arbiter of the QPG6200L is used; up to 2 other radios can be interfaced to this arbiter. The arbiter uses a straightforward request-granted approach with 4 priority levels.

Slave : The QPG6200L will request access to the medium from an external arbiter.

Table 2 below shows the signaling lines between the QPG6200L and the arbiter or other radio(s). The mapping of these signals to pins is given in Table 40.

Table 3 contains the options for coex signal configuration.

Table 2: Coex Signal Names

Master Signal Name	Input/Output	Function
COEX_MS_REQA	Input	Request signal from other radio A
COEX_MS_GRANTA	Output	Grant signal to other radio A
COEX_MS_PRIOA	Input	Priority signal from other radio A
COEX_MS_REQB	Input	Request signal from other radio B
COEX_MS_GRANTB	Output	Grant signal to other radio B
COEX_MS_PRIOB	Input	Priority signal from other radio B

Slave Signal Name	Input/Output	Function
COEX_SL_REQ	Output	Request signal from QPG6200L radio to the external arbiter
COEX_SL_REQ_NOT	Output	Request signal from QPG6200L radio to the external arbiter (inverted)
COEX_SL_GRANT	Input	Grant signal from the external arbiter to the QPG6200L radio
COEX_INT_PRIO_0	Output	Priority signal from QPG6200L radio to the external arbiter
COEX_INT_PRIO_1	Output	Priority signal from QPG6200L radio to the external arbiter

Table 3: Signal Configuration Options

Input Signal	Effect
Not Mapped - Treat as ’0’	input value is always treated as a ’0’
Not Mapped - Treat as ’1’	input value is always treated as a ’1’
Pin	’high’ is a logic ’1’; ’low’ is a logic ’0’
Inverse Pin	’high’ is a logic ’0’; ’low’ is a logic ’1’
Output Signal	**Effect**
Not Mapped	-
Push Pull	Push Pull Driver; logic ’1’ is ‘high’, logic ’0’ is ‘low’
Inverse Push Pull	Push Pull Driver; logic ’1’ is ‘low’, logic ’0’ is ‘high’
Open Drain	Open Drain Driver; logic ’1’ is ‘high’, logic ’0’ is ‘low’
Inverse Open Drain	Open Drain Driver; logic ’1’ is ‘low’, logic ’0’ is ‘high’

Until the software in the QPG6200L has been initialized, the coexistence signaling pins are floating.

7 Peripherals

The QPG6200L features a set of peripherals and allows configuration of the mapping between the IO signals needed by the peripherals and the available IO pins.

7.1 IO Pins

The QPG6200L features many IO pins that can be configured for pre-defined functional signals; see the Pin Assignments in section 12.1.1.

The complete pin configuration with associated settings is retained when going to Sleep mode.

Table 4: GPIO and ANIO Configurations

I/O Type	Number
GPIO (programmable General Purpose I/O)	14x
ANIO (programmable Analog I/O)	2x
pins for the optional ANIO's can alternatively be used as **GPIO**	2x (input only)
pins for the optional DC/DC converter can alternatively be used as **GPIO**	2x
pin for the optional LPBIAS can alternatively be used as **GPIO**	1x
pins for the optional 32 KiHz reference crystal can alternatively be used as **GPIO**	2x (input only)
max. number of GPIO's	17x input/output + 4x input only

7.2 GPIO

The QPG6200L features programmable GPIO lines that are mapped individually to functional signals, as specified in the Pin Assignments in Table 37 and Table 38, with following settings:

- **Pull-up/Pull-down:** most GPIO pins can be configured to the following pull-up/down modes:
  - Floating mode – Pull modes disabled
  - Pull down mode
  - Pull up mode.

  Exceptions are: GPI25 and GPI26 are always in floating mode.

  Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

  The GPIO pins can be individually weakly pulled up or weakly pulled down during active as well as Sleep states.

- **Wake up**: except for GPIO19 and GPIO20, all GPIO pins can be configured as wake-up pin. Each of these can be configured to trigger a wake-up event on a rising edge, on a falling edge, or on both edges seen on the pin.

- **Drive strength**: the drive strength of each GPIO output can be configured individually to 2 mA, 4 mA, 8 mA or 12 mA. This is applicable only to standard GPIO's that support both input and output, so not for input only GPIO's (GPI).

- **High Drive Sink**: on GPIO0 a high drive sink (MOSFET N-Type) can be enabled, suitable for e.g., driving a high-power IR LED circuit. Figure 3 shows an IR LED circuit with the high drive sink enabled. For comparison, Figure 4 shows an example without high drive sink.

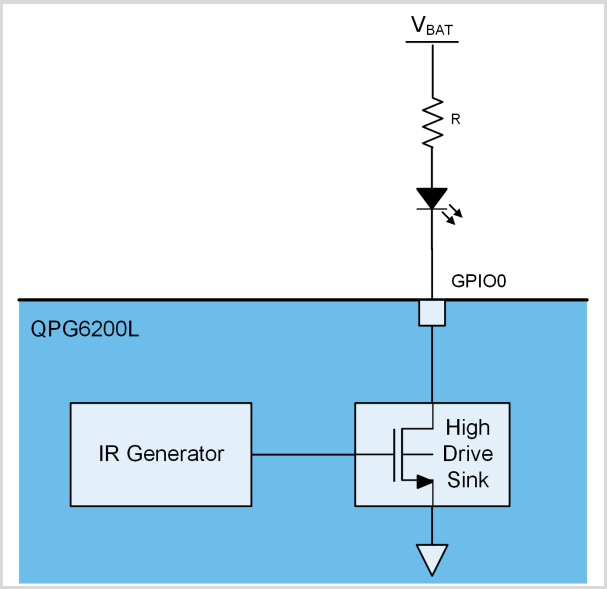


Figure 3: IR with High Drive Sink

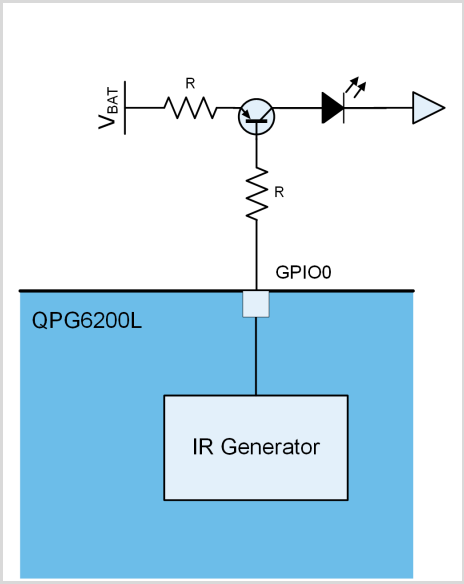


Figure 4: IR without High Drive Sink

7.3 ANIO / ADC

The QPG6200L has integrated ADC's that can be used to monitor external analog signals via the ANIO pins. 2 ANIO's are provided for inputs to:

- High-resolution 16-bit ADC
- General Purpose 11-bit ADC
- Low-power Comparator.

The QPG6200L contains a full switch matrix (MUX) connecting any ANIO to the ADC or the LPCMP.

ANIO's can be combined for differential measurements.

Section 11.11 provides the ADC's accuracy and other characteristics.

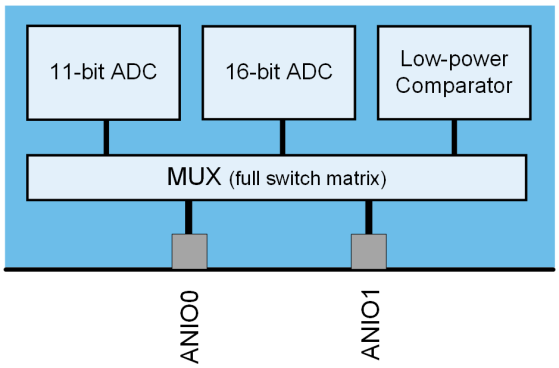


Figure 5: ANIO Connect Options

7.4 Battery / Temperature Monitor

The ADC module can be configured by software to monitor the power supply level internally; no external components are required. The power supply level and temperature are measured separate from the ANIO pins.

7.5 Keyboard Scanner

The QPG6200L has an integrated 8x8 Keyboard Scanner with ultra-low power wake-up on key press, keyboard scan and de-bounce. The keyboard scan operation is triggered by a change on the IO (key press), as well as by a timed event (for de-bouncing). The keys are organized in a matrix. The mapping of the physical keys (row/column) to the application or profile-defined keys is software configurable.

The maximum number of keyboard columns and rows depends on the number of other GPIO-devices enabled; see Table 37 and Table 38.

7.6 IR Generator

The QPG6200L has an InfraRed (IR) generator. The IR carrier and modulation parameters and codes are defined by the application software. The IR generator supports a wide range of common IR protocols.

The IR generator supports multiple modulation modes:

- Pattern based: input is a pattern of 0's and 1's in RAM
- Time based: input is a sequence of ON and OFF times
- Event based: modulation is controlled by scheduled actions.

7.7 LED Generator

The QPG6200L supports up to 4 signaling LEDs, with configurable function and events. The LED generator supports:

- 8-bit Pulse-Width Modulation (PWM)
- Fade-in/Fade-out
- Duty cycling to adjust brightness and save power.

7.8 LED Pixel Protocol Master (RTZ)

The QPG6200L contains two LED Pixel Protocol Masters which support many commercially available LED pixel driver IC's using the RTZ (Return To Zero) protocol. This will enable sending frames for all pixels, without microcontroller intervention.

- Supports Sequential (*Neopixel*) and Random (*Christmas tree*) addressing
- Highly configurable to support many protocols
- Efficient RAM usage for the pixel frames.

7.9 PDM Microphone Interface

The QPG6200L contains two Pulse-Density Modulation (PDM) MEMS Microphone Interfaces. It provides conversion from a Pulse Density Modulated signal (PDM), which is typically used for low-cost digital microphones, to a 16-bit Pulse Code Modulated signal (PCM). The PCM signal can then be used for further processing and compression of the audio using the embedded Audio Signal Processors.

The PDM interfaces supports:

- A Clock and Data pin for interfacing with a PDM MEMS microphone.
- Optionally Capturing Data on the Rising and Falling Edge of the Clock for Stereo operations.
- Configurable frequency of Clock signal:
  - Default = 2 MHz
  - Digital frequency synthesizer for generating frequencies up to 3072 kHz.
- HW CIC Decimation filter with programmable decimation factor (R=1…64) that converts 1-bit input samples to 16-bit output samples. HW CIC output can be connected to DMA, to allow this processing chain to be extended with further decimation, equalization, volume control and compression using the Cortex M4F DSP routines.

7.10 PWM Engine

The QPG6200L contains a PWM (Pulse-Width Modulation) peripheral.

The PWM peripheral enables the generation of 16-bit pulse width modulated signals on an assigned GPIO. Thanks to its advanced feature set it can support a wide range of use cases, including LED driver use cases.

The main features of the PWM peripheral are:

- Programmable PWM frequency
- Up to 8 PWM channels, each with an independent phase and duty cycle
- Arbitrary waveform generation driven by RAM defined sequences
- Glitch free parameter updates.

7.11 Generic Timers

The QPG6200L contains a number of generic timers; 6x 32-bits or 12x 16-bits (software selectable), allowing time intervals to be defined by the user. The timers can be used in a prescaled mode, where the counter is running from the main clock with a configurable divide ratio, or in count mode, where the counter is incremented on a configurable event (e.g., an external pin event).

Each timer has 4 capture/compare channels allowing generating interrupts when the count value matches the compare value, or to capture the count value on a configurable event (e.g., an external pin event).

8 System, Interfacing and Programming

8.1 Internal Microcontroller

The internal microcontroller is a high performance 32-bit Arm Cortex-M4 processor with floating point support and DSP functionality, optimized for low power consumption, performance and code size. This allows the QPG6200L to operate as a standalone system.

It runs at up to 192 MHz clock speed (*) and can execute code from NVM as well as from RAM, with zero wait states.

(*) 192 MHz supported over a limited temperature range, 96 MHz supported over the full temperature range.

Table 5: Memory Access Speeds

Arm clock	MCU RAM access	System RAM access	ROM access	NVM Memory access
32 MHz	32 MHz	32 MHz	32 MHz	32 MHz for linear code; 16 MHz worst case
64 MHz	64 MHz	32 MHz	32 MHz	64 MHz for linear code; 16 MHz worst case
96 MHz	96 MHz	32 MHz	32 MHz	96 MHz for linear code; 16 MHz worst case
192 MHz	192 MHz	32 MHz	32 MHz	192 MHz for linear code; 16 MHz worst case

8.2 Memory Architecture

The QPG6200L contains the following memory blocks:

- **336 kB RAM**: Low Leakage Random Access Memory (RAM).
  This is split in:
  - 288 kB MCU RAM, accessible to the internal microcontroller and the DMA Engine
  - 32 kB RAM available to the radio subsystem
  - 16 kB System RAM, accessible to the internal microcontroller, the DMA Engine and other functional blocks.
- **2 MB (**2048 kB) **NVM memory (RRAM),** for program storage, calibration data and NVM storage of critical run-time data (e.g., pairing information and frame counters). The contents are retained under all circumstances (Power-On-Reset, Sleep).

  Note: 8 kB of NVM memory is reserved for OTP.

The QPG6200L has a 16-channel DMA Engine that relieves the microcontroller from transferring data internally between RAM and peripherals.

8.3 System States

The QPG6200L is designed to work in an environment where low power consumption is very important. The QPG6200L System State is either **System Active** or **System Sleep** (*stand-by*) to achieve low power consumption. The following sections will explain the differences.

8.3.1 System Active

The System Active state is the default operational state after a Power-On-Reset. In this state all functional blocks, including the application microcontroller are active or can be activated, based on the configuration set by the application software. The software running on the application microcontroller will control the operational state and will initiate a state transition if that is desired. Power consumption is optimized in this state by disabling inactive clocks and by choosing the appropriate Power Mode (see Power Modes section 8.6).

8.3.2 System Sleep

The System Sleep state (*stand-by*) is the deepest power saving mode the device can use. In this state the main functional blocks are **not** active, including the application microcontroller. Only the LPS (Always On) blocks are available. See also Figure 6.

The System Sleep state can be entered when all functional blocks indicate there are no tasks pending and the application microcontroller allows the system to go into a deep power down mode, because the next tasks are far enough in the future, or a next task should be initiated by an external event.

The following events can cause the device to 'wake up' from the System Sleep state:

- **RTC timestamp match** - The Real Time Counter block provides a time base, clocked by the 64 kHz or 32 KiHz Real Time Clock or the divided down 32 MHz clock. The block can generate a wake-up trigger at a certain timestamp configured by application software.
- **GPIO pin event** - The always on GPIO event block can be configured to wake up the system on a rising edge and/or falling edge on a GPIO pin.
- **Low Power Comparator event** - The low power analog comparator can be configured to wake up the system on a compare valid event.
- **Reset** - A pin reset, or Power On reset detect will also cause the device to exit the System Sleep state.

The System Sleep state allows for reaching the lowest device power consumption. All HF clock sources (32 MHz, 64 MHz, 192 MHz) can be disabled and the main digital power blocks can be switched off. When the device wakes up from the System Sleep state, a wake-up procedure is performed that is similar to a reset procedure. One of the phases in the wake-up procedure is to restore the state of the different functional blocks. Depending on the power options used during the System Sleep state, this restoring can take more time.

Essentially there are 2 **groups** of Sleep modes:

- **eLPS and LPS power modes** (*Digital off modes*) – These are the lowest power modes, where the main digital domain power supply is switched off. All states are lost and the device depends on the Register Retention settings to be able to restore the state after wake-up.
- **HPSret** (*Digital retained mode*) - This is a mode where the digital domain power supply is kept on. In this case all states are retained, and no restoring is necessary. This a higher current System Sleep state that allows for a faster wake up but power consumption is higher compared to a *Digital off mode*.

When an application uses the System Sleep mode to get to the lowest possible power consumption, it can be necessary to also retain the content of the different data RAM's, next to the register retention mentioned above. The amount of RAM that is retained has a significant effect on the current consumption during System Sleep. it is important that the user is able to only retain the RAM that really holds application state. For this reason, the user has fine grained software control over what RAM is retained.

8.4 Oscillators & Clocks

The 64 MHz and 192 MHz ring oscillators provide the **HF main clocks**. The 192 MHz ring oscillator is needed for all use cases using the radio.

The **192 MHz ring oscillator** provides the HF main system clock. For most use cases, and for all use cases using the radio, this oscillator needs to be used as the main system clock. To use this clock, the 32 MHz reference clock must be running. Enabling the 192 MHz oscillator is under software control.

The **64 MHz ring oscillator** serves as the startup clock and the clock used by the PMU (Power Management Unit). At wake-up, the free running 64 MHz ring oscillator will provide a clock to allow digital processing while the 32 MHz crystal is still starting.

The **32 MHz crystal oscillator** is based on the required external 32 MHz crystal. This HF oscillator is used as the source for the high accuracy main system clock and reference frequency for the radio subsystem. And it is used as a reference for generating the internal 192 MHz clock. Enabling this crystal oscillator is under software control.

The **64 kHz Low Jitter RC** (LjRC) **oscillator** is an internal LF low-power oscillator designed to support applications needing an accurate time-base during Sleep (*standby*), effectively removing the need for a 32 KiHz oscillator with external crystal. High accuracy is obtained through regular calibration of the LJRC oscillator using the 32 MHz crystal reference clock. This oscillator can be the LF clock source of choice for cost constrained low-power use cases, as no additional external components are needed.

The optional **32 KiHz crystal oscillator** is based on the optional external 32 KiHz crystal. This LF oscillator can be used for lowest-power use-cases when accurate timing during Sleep is needed. For example, applications that implement long Sleep intervals requiring synchronized wake up events (i.e., Bluetooth Low Energy) as the more accurate timing results in a smaller guard band and more time spent in Sleep mode. It provides a very accurate time reference, at the cost of an additional external crystal.

Note that enabling / disabling the oscillators, and the switchover of the main system clock source, is very tightly coupled to the power mode that is in use.

8.5 Event Scheduler

The Event Scheduler uses an accurate Adaptive Timing Engine to generate a common and calibrated system time base. This time base is maintained over sleep cycles and can be used throughout the system to schedule actions, autonomously and periodically, in a just-in-time manner, improving the overall energy consumption of the system.

Additionally, the Event Scheduler also provides an advanced event handler function for scheduling software interrupts.

The time base spans up to 30 minutes with a 1 µs resolution.

8.6 Power Modes

In this section the different power modes in the QPG6200L are defined. The power mode is closely related to the system state of the device as some power modes are only available in one or the other state.

The QPG6200L supports the power modes as stated in Table 6 below.

The names of the power modes that start with “**e**”, for example; **e**LPS, are the **e**nhanced power modes that use the internal DCDC converter to minimize power consumption.

HPSret is a power mode that can be used to bring the system state to Sleep but allowing a fast wake-up. All states are retained and no restoring is necessary. Typical use cases are short sleep durations (no need for data backup/restore) and use cases where the 32 MHz crystal oscillator is used as sleep time base.

Table 6: Main Power Modes (lowest power consumption on top)

Name	Meaning	System state	Main system clock	Digital supply	Analog supply	DCDC	Benefits
eLPS	enhanced Low Power State	SLEEP	OFF	OFF	OFF	ON	lower power compared to LPS
LPS	Low Power State	SLEEP	OFF	OFF	OFF	OFF	low cost (*)
HPSret	High Performance State, retain all states	SLEEP	OFF	ON	ON	OFF	fast wake-up
eHPS	enhanced High Performance State	ACTIVE	192 MHz	ON	ON	ON	lower power compared to HPS
HPS	High Performance State	ACTIVE	192 MHz	ON	ON	OFF	low cost (*)

(*) no DCDC inductor needed.

Power modes can be identified by these properties (see table above):

- **Main clock**: defines what the **main** clock source is.
- **Digital supply**: defines if the main digital supply is ON or OFF.
- **Analog supply**: defines if the analog supply is ON or OFF.
- **DCDC**: defines if the power supplies are fed by the DCDC converter or the LDO's (see Figure 8).
- **System state**: defines if the power mode is applicable to the System Active state or System Sleep state.

Figure 6 below shows an overview of the different subsystems and digital peripherals. Its color indicates the 'minimal' power mode; (e)LPS or (e)HPS mode, that is required for the block to function correctly.

As an example, the block "2.4 GHz radio" has (e)HPS as minimal required power mode, so it will not correctly work in the (e)LPS power mode.

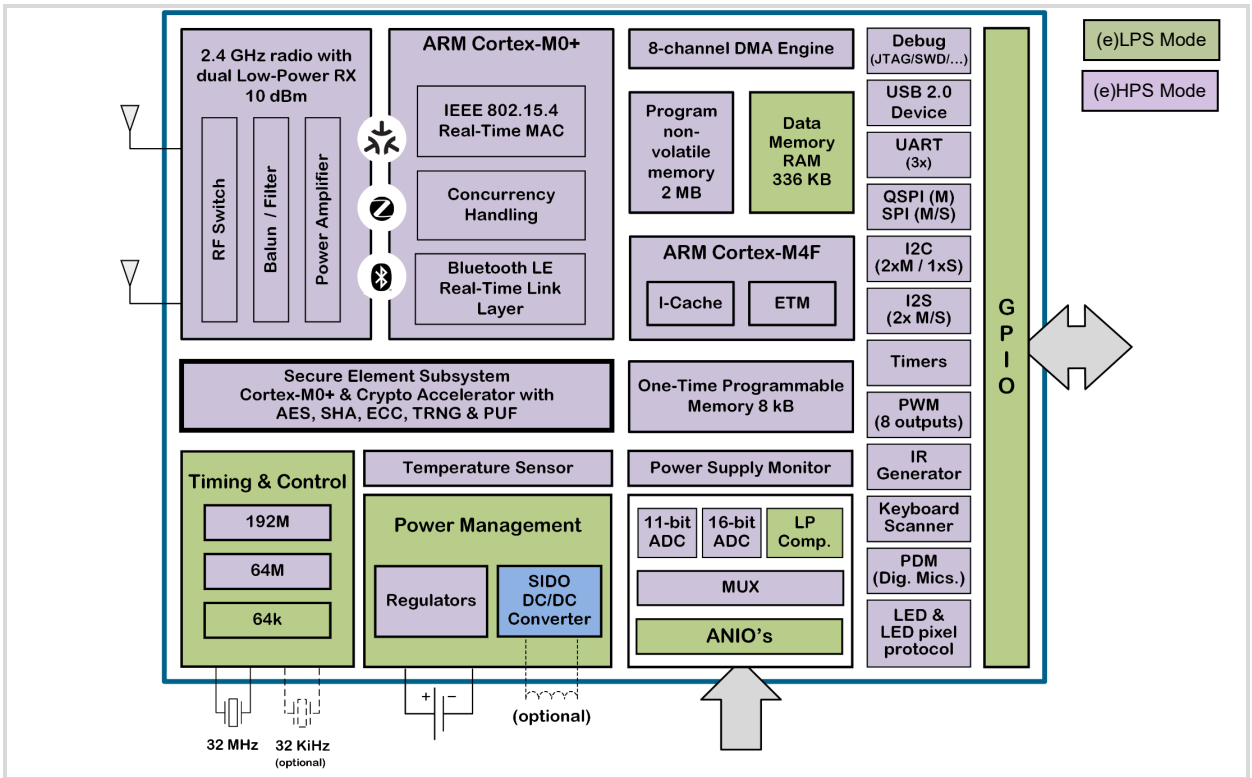


Figure 6: (e)LPS and (e)HPS Power Modes

8.7 Watchdog

The QPG6200L contains a Watchdog timer that serves to detect and resolve software failures and to trigger an interrupt, an internal microcontroller reset, or a system reset when the timer reaches a certain timeout value.

Timeout values are software configurable:

- 16-bit time-out values in 16 µs resolution
- Configurable watchdog time-out (16 µs - to 1 s)
- Configurable action (interrupt / Application Microcontroller reset / Chip Soft POR)
- Protection to accidental watchdog triggering and disabling.

8.8 Interfacing

8.8.1 UARTs

The QPG6200L contains three Universal Asynchronous Receiver and Transmitters (UARTs) for interfacing with additional peripheral devices and/or for terminal logging during (software) development. The UARTs support:

- Full-duplex operation
- Baud rates from 488 Bd to 2 MBd
- Serial frames with 5, 6, 7, 8 or 9 data bits and 1 or 2 stop bits, with framing error detection
- Odd or even parity generation and checking
- Buffer overflow detection
- False start bit detection and digital low pass filter for robustness against noise
- Separate interrupts on TX Complete, TX Data Register Empty and RX Complete
- Configurable pin mappings, i.e., a RX pin and a TX pin can be made available on the QPG6200L pin-out.
- Configurable hardware flow control.

8.8.2 USB Device

The QPG6200L supports a USB 2.0 Device supporting Full Speed (12 Mbit/s) data rate.

- Support for bulk, interrupt, and isochronous transfers
- programmable double buffering for bulk and interrupt endpoints
- 1 kB data buffer
- DMA for copying data to/from the USB data buffer
- supports USB remote wake-up.

8.8.3 QSPI Master

The QSPI Master provides an interface for accessing external memory slaves. Depending on the type of the memory slave, the interface between master and slave consists of up to four data signals (IO0, IO1, IO2, IO3), a serial clock (SCLK) and a slave select signal (SSN). It supports the Single SPI, Dual SPI and Quad SPI transfer modes.

8.8.4 SPI Master

The QPG6200L contains a Serial Peripheral Interface (SPI) for interfacing with additional peripheral devices. This SPI Master supports:

- Full-duplex synchronous transfers on three lines (MISO, MOSI, SCLK)
- Programmable clock polarity and phase, supports SPI mode 0, 1, 2 and 3
- Programmable data order with MSb-first or LSb-first shifting
- High speed clock generator supporting clock speeds up to 32 MHz
- 4-bit to 16-bit transfer frame format selection
- Three separate interrupts on TX Complete, TX Data Register Empty and RX Complete.

8.8.5 SPI Slave

The QPG6200L contains an SPI Slave interface. This SPI Slave supports:

- Generic customer protocols
- Proprietary Qorvo DMA protocol
- SPI mode 0
- SPI clock frequencies up to 16 MHz
- Limited to byte-based operation
- Flexible IO mapping.

8.8.6 I²C Master

The QPG6200L contains two I²C (Inter-Integrated Circuit) Master interfaces, also referred to as Two-Wire Interface (TWI), for interfacing with additional peripheral devices. This I²C Master supports:

- Standard mode and Fast mode
- Short (7-bit) and long (10-bit) addresses
- General call address (0x00)
- Clock stretching.

8.8.7 I²C Slave

The QPG6200L contains an I²C Slave interface. This I²C Slave supports:

- Standard mode and Fast mode
- Short (7-bit) and long (10-bit) addresses
- Configurable Slave Address
- General call address (0x00).

8.8.8 I²S Master/Slave

The QPG6200L contains two I²S (Inter-IC Sound) Master/Slave interfaces for interfacing with a broad range of I²S devices such as digital audio devices, ADC's, DAC's, audio CODEC's, etc. Each interface can either be in Master mode or in Slave mode.

These I²S interfaces support:

- Full duplex transfers
- Configurable word length
- Left justified (right justified mode can be emulated)
- Double buffered, DMA capable
- Master clock frequency selectable from 62.5 kHz up to 8 MHz
- External Slave clock input supporting speeds up to 4 MHz.

8.8.9 SPI Programming Interface

The primary programming interface for (production) programming of the NVM is the SPI Slave interface (see section 8.8.5). For this the signals shown in Table 7 shall be made available for programming.

Table 7: Mapping Signals for Programming via SPI

QPG6200L	Signal	Notes
EDP	GND	Ground.
VDD	VCC_DUT	The recommended supply voltage is: 3.3 V.
RESETN	RESETn	The reset signal.
GPIO6	PROG_SSn	Slave select signal.
GPIO7	PROG_SCLK	Clock provided by the Programmer.
GPIO8	PROG_MOSI	Data from Programmer to device.
GPIO9	PROG_MISO	Data from device to Programmer.
GPIO5	PROG_ENn	Low (stable) enables programming mode at startup/reset. Should be kept low at least until the first SPI access in programming mode. The time between Reset and the first SPI access must be at least 50 ms. If no command has been received within 4 s, the chip will enter normal application mode.

The following characteristics apply to the SPI programming interface:

- maximum SCLK frequency: 2.25 MHz
- minimum SSn high time: 2 µs
- minimum last SCLK to SSn high time: 10 µs.

8.8.10 Clock Output

The QPG6200L can provide two clocks to peripheral devices (CLK_OUT). The clock frequency is derived from the 192 MHz crystal oscillator system clock. It can be configured for frequencies up to 96 MHz.

8.9 Application Programming Information

Available from **Arm**:

Generic User Guide, Cortex™-M4 Devices;
https://developer.arm.com/documentation/dui0553/a/

Available from **Qorvo**:

IoT Dev Kit for QPG6200L (QPG6200LDK-01) includes:

- Hardware Development Kit
- Software Development Kit
- Tools for evaluation, development and production phases
- Certified stacks and turn-key reference applications
- Documentation for the hardware, software and tools.

For more information: see Qorvo's website.

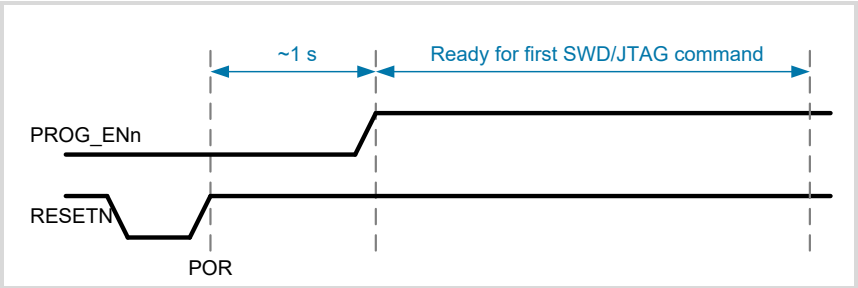
8.10 NVM Programming and Configuration

The NVM program and configuration memory is not programmed when the chips are shipped by Qorvo. To enable the functionality, the NVM must be programmed through a dedicated programming protocol. Please contact Qorvo Support for details of available programming solutions. If programming takes place on the target PCB, the Program Port signals need to be accessible on the PCB.

8.11 Debug Mode

During startup/reset the QPG6200L can be triggered to come up in debug mode. The SWD/JTAG signals shown in Table 8 below will then be available. The operation is dependent on the provisioned Secure Debug configuration.

Table 8: Debug Mode Signals

QPG6200L	SWD/JTAG	Notes
GPIO6	SWIO/TMS	
GPIO7	SWCLK/TCK	
GPIO8	TDI	
GPIO9	SWV/TDO	
GPIO5	PROG_ENn	Low for about 1 s after Reset, then high, enables debug mode.  **Figure 7: Entering Debug Mode** While PROG_ENn is asserted low, no transaction should be started on SPI or UART (otherwise programming mode will be entered). The QPG6200L will be ready for the first SWD/JTAG command for a period of 32 s. If then no command has been received, the chip will enter normal application mode.

9 Power Management

The QPG6200L has an integrated power management system which includes a SIDO (Single-Inductor Dual-Output) DC/DC Converter with several dedicated LDO's. When the DC/DC Converter is enabled, the power consumption of the chip can be severely reduced by a factor of 1.5 to 3, depending on the supply voltage. When the DC/DC Converter is not used, the Global LDO and the Core LDO are used to generate the internal power supplies.

The chip always powers up using the Global LDO and Core LDO where after the DC/DC Converter can be enabled or disabled by the application program.

Note that decoupling capacitors C_{ANA} and C_{CORE} are needed for VDDANA and VDDCORE respectively.

The Bandgap Reference is used for all LDO's.

9.1 DC/DC Converter

The QPG6200L contains an integrated SIDO DC/DC Converter to reduce the power consumption of the chip. The DC/DC Converter uses one low-cost external inductor as shown in Figure 8 below (see Table 33 for the required value). It converts the battery supply voltage to lower voltages that are used to supply the analog LDO's (feeding the analog/RF blocks) and the digital core blocks.

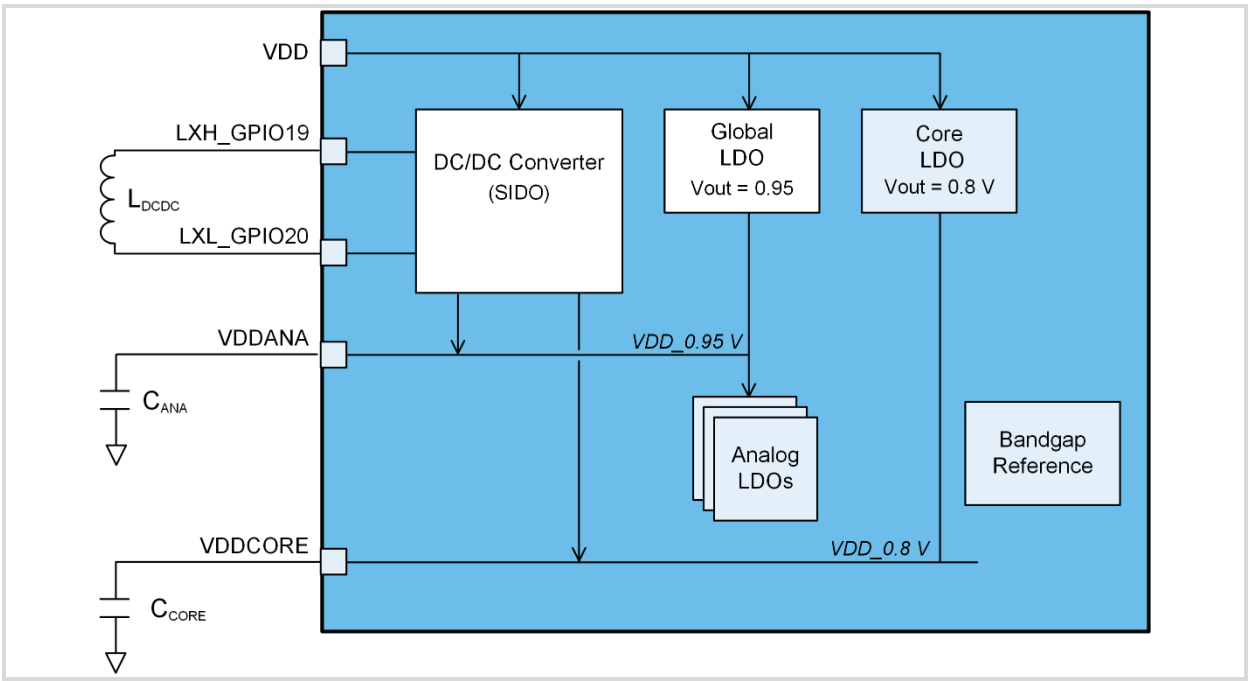


Figure 8: DC/DC Converter

The QPG6200L offers full flexibility to the application program to enable or disable the DC/DC Converter after the chip is powered up and out of Sleep mode. During Sleep (eLPS mode), the DC/DC Converter can be enabled to save power.

The DC/DC Converter requires a minimum supply voltage level to be efficient. The chip will detect when the input voltage gets too low (below 2.2 V) and will then automatically use the Global LDO. When the DC/DC Converter is enabled while the input voltage is too low, it will not start up and, after 1 ms, the chip will continue using the Global LDO.

If an application does not make use of the DC/DC Converter, the external inductor (L_{DCDC}) is not required to be placed. In this case, two pins of the DC/DC Converter can also be configured to be used as GPIOs (GPIO19 and GPIO20).

9.2 Low Voltage Behavior

The QPG6200L contains following features that can be combined to implement the desired low voltage behavior:

- **VDD Brown-out Interrupt**: interrupt that can be software configured to trigger when VDD drops below the VDD Brown-out threshold while being active. This interrupt can be used to trigger the software to disable the radio and go into Sleep mode. A higher value gives the application more time for state cleanup.

  The VDD Brown-out threshold is software configurable from 1.75 V to 2.1 V in steps of 50 mV; default value is 1.75 V.

- **Cut-Off**: a VDD threshold under which all functions are disabled, and current consumption is strictly limited.

Brown-out threshold	Cut-Off threshold
1.75 V (default)	1.575 (default)
1.80 V	1.60 V
1.85 V	1.625 V
1.90 V	1.65 V
1.95 V	1.675 V
2.0 V	1.70 V
2.05 V	1.725 V
2.1 V	1.75 V

- **VMT**: Voltage Minimum Threshold under which the chip will not wake up from Sleep mode. Its main function is to prevent battery leakage.

  The VMT range is software configurable from 1.6 V – 3 V in 50 mV steps.

  VMT crossing detection time is also software configurable; default is 125 µs. This value can be extended to 1 ms to save current.

- **POR Detector**: the Power-On-Reset circuit resets the chip before the VDD voltage reaches the minimal operating voltage. The chip embeds a Power-On-Reset circuit with internal and external triggers as shown in the table below.

Detector Type	**Trigger condition** (typ.)	**Response time** (typ.)
internal (on-chip VDD monitor)	VDD << 1 V	1 ms
external (RESETn input)	V_{resetn} < ½ VDD	< 10 ns
note: the internal reset trigger circuit samples VDD, the circuit behaves like a sample-based circuit at 1 kHz. The external reset trigger uses an asynchronous (direct) input.		

10 Security

The QPG6200L is equipped with a low-power Secure Element subsystem providing secure operation functionalities to the application. This subsystem contains a dedicated secure microcontroller, memories and interfaces. It can work independently from the Application Microcontroller, IEEE 802.15.4 MAC and Bluetooth LL.

The Secure Element Subsystem supports:

- **Secure Boot** (rooted in ROM with Boot Key in OTP), Physical Unclonable Function (PUF)-based **Secure (Key) Storage**, **Secure (Key) Provisioning**, **Secure Debugging**, **Secure Device Attestation**.
- Hardware accelerated **Public Key Crypto engine** for these crypto systems: ECC/ECDH/ECDSA, EdDSA, Primality Test (Rabin-Miller), J Pake and ECMQV.
- Hardware accelerated **ECC** dramatically improves performance on the following ECC curves: Curve25519/Ed25519, NIST P-192, NIST P-256, NIST P-384, NIST P-521/E-521.
- Hardware accelerated **Hash Crypto Engine**: SHA-1, SHA-2 (SHA-224, SHA-256, SHA-384, SHA-512), SHA-128.
- Hardware accelerated **AES Crypto Engine** supporting encryption and decryption of cyphering modes: ECB, CBC, CTR, CFB, CCM, CCM*, GCM, CMAC.
- Flexible **Tampering Detection** (Voltage tampering, BBPLL tampering, Boot authentication failure, PK ROM integrity error, SEUC RAM ECC correction or failure, Unauthorized access, Watchdog time-out).
- Cryptographic **Random Number Generator** featuring TRNG, DRBG, Conditioning and Health test.
- **Restriction Locks** to certain security-sensitive hardware aspects of QPG6200L, e.g., register maps, NVM regions, OTP.

11 Electrical Characteristics

The QPG6200L characteristics are determined in the circuits shown in Figure 9 to Figure 11 below.

- Current consumption values for transmit and receive are specified with and without the DC/DC Converter enabled.
- Transmit as well as receive behavior is measured in accordance with the IEEE 802.15.4 specification and the Bluetooth Test Specification (RF-PHY.TS.5.0.1).
- All parameters are measured at VDD = 3.0 V and T_A = 25 °C, unless otherwise specified.
- IEEE 802.15.4 channel rejection is measured with the QPG6200L reference design system as interferer.

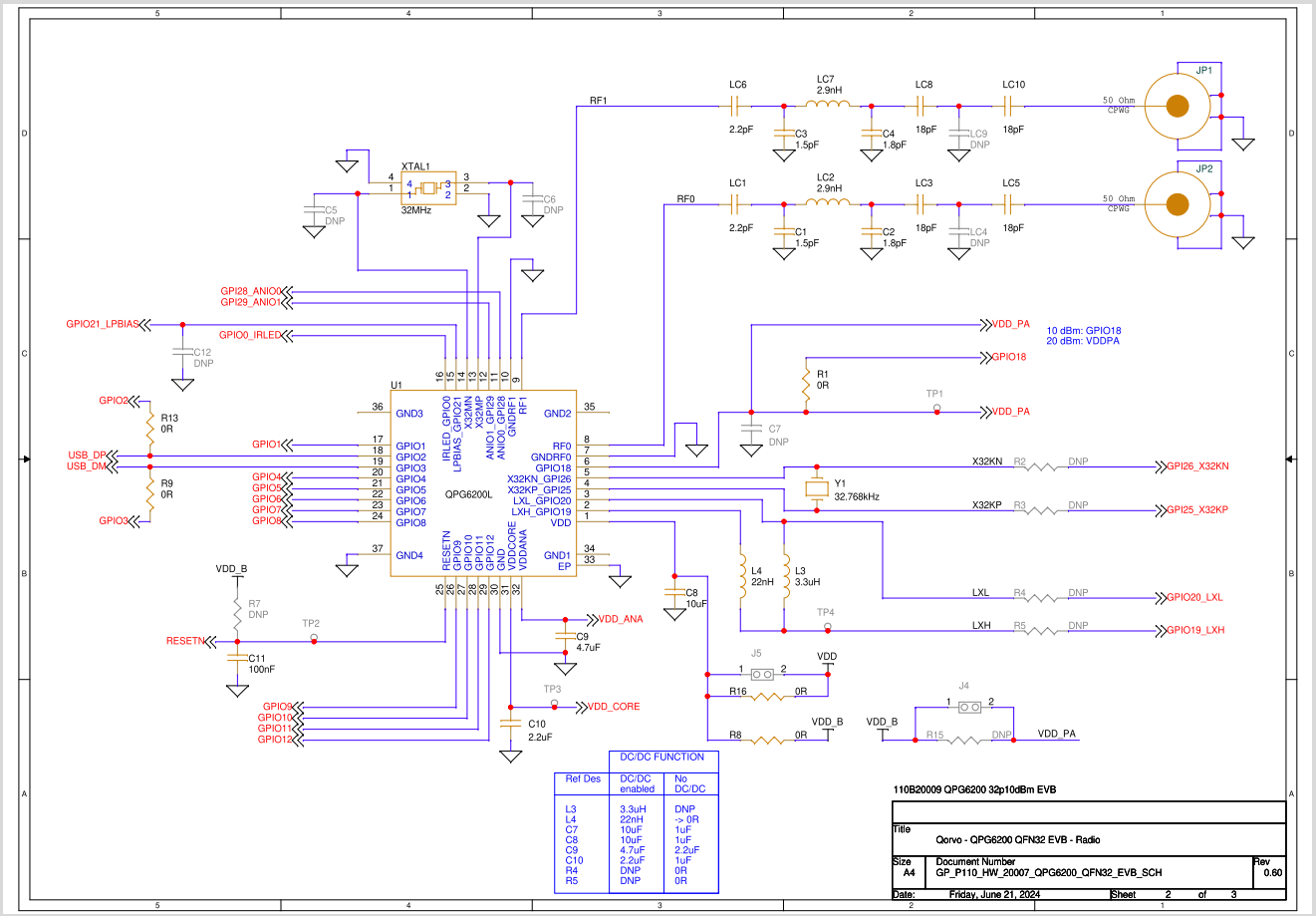


Figure 9: Parameter Evaluation Circuit (sheet 2 of 3)

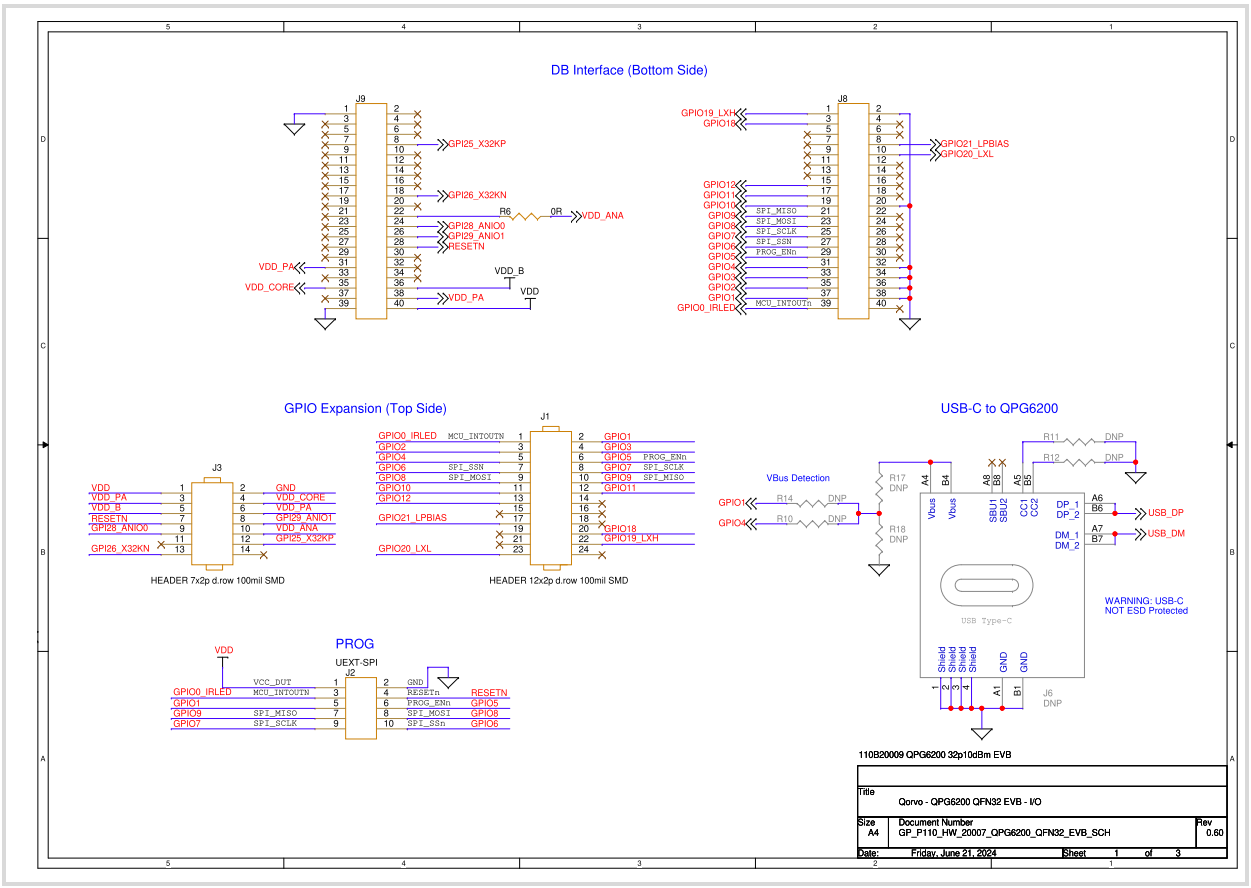


Figure 10: Parameter Evaluation Circuit (sheet 1 of 3)

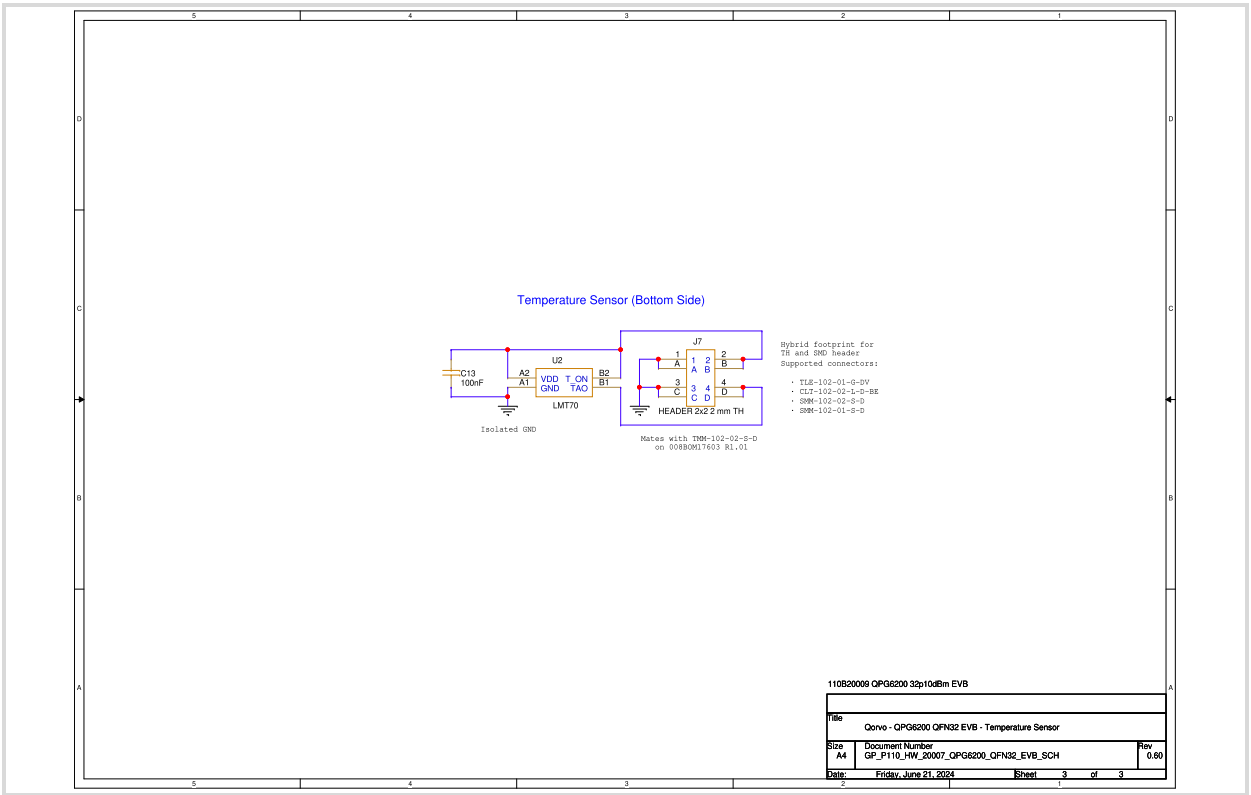


Figure 11: Parameter Evaluation Circuit (sheet 3 of 3)

11.1 Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VDD	Power supply input voltage	-0.3 to +3.6	V
Digital pins (see Table 36)	Digital IO voltage	-0.3 to VDD+0.3 (Max = +3.6)	
ANIO0..ANIO1	Analog IO voltage	-0.3 to +3.6	
Other analog pins (see Table 36)	Analog IO voltage	-0.3 to +1.05	
VDDCORE	Decoupling voltage	-0.3 to +1.05	
VDDANA	Decoupling voltage	-0.3 to +1.05	
RF0, RF1	RF IO voltage	-0.3 to +1.8 (ESD clamp diodes may limit applied voltage)	
P_{MAX}	Input RF level	+10	dBm
T_J	Junction Temperature	+145	°C
T_{stg}	Storage Temperature	-50 to +150	°C
T_{sol}	Reflow Soldering Temperature	+260	°C

ESD Test name	Test standard	Test results
ESD Human Body Model (**ESD HBM**)	ANSI/ESDA/JEDEC JS-001 2023	TBD
ESD Charged Device Model (**ESD CDM**)	ANSI/>ESDA/JEDEC JS-002 2022	TBD

11.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD	Power supply input Voltage		1.71	3.0	3.6	V
T_A	Ambient Temperature		-40	+25	+125	°C
F_{ref}	Reference Crystal Oscillation Frequency			32		MHz
V_{IH}	Input HIGH voltage (for all GPIO lines) (*)	VDD=1.71 V	-	-	VDD	V
		VDD=3.0 V	-	-	VDD	
		VDD=3.6 V	2.0	-	VDD	
V_{IL}	Input LOW voltage (for all GPIO lines) (*)	VDD=1.8 V	VSS	-	-	
		VDD=3.0 V	VSS	-	-	
		VDD=3.6 V	VSS	-	0.8	
V_{OH}	Output HIGH voltage (for all GPIO lines) (**)	VDD=1.8 V	-	-	VDD	
		VDD=3.0 V	2.4	-	VDD	
		VDD=3.6 V	-	-	VDD	
V_{OL}	Output LOW voltage (**) (for all GPIO lines) (**)	VDD=1.8 V	VSS	-	-	
		VDD=3.0 V	VSS	-	0.4	
		VDD=3.6 V	VSS	-	-	
R_{pu}	Resistance input pull-up resistor (for all GPIO lines)	VDD=1.8 V	-	-	-	kΩ
		VDD=3.0 V	-	-	61.4	
		VDD=3.6 V	16	-	-	
R_{pd}	Resistance input pull-down resistor (for all GPIO lines)	VDD=1.8 V	-	-	-	
		VDD=3.0 V	-	-	61.4	
		VDD=3.6 V	16	-	-	
V_h	Input hysteresis voltage	VDD=1.8 V	-	-	-	V
		VDD=3.0 V	0.2	-	-	
		VDD=3.6 V	-	-	-	
I_{pad}	Input leakage current	VDD=1.8 V	-	-	-	µA
		VDD=3.0 V	-	-	-	
		VDD=3.6 V	-5	-	+5	
I_{OH}	Total sourced current for all GPIO output lines combined (excluding the high drive of GPIO0)				100	mA
T_{INT}	Pulse width for GPIO interrupts		250			ns

Note (*): for GPIO0 with high drive sink, refer to section 11.14.

Note (**): Drive strength = 2 mA, 4 mA, 8 mA and 12 mA.

11.3 Current Consumption

Table 11: Current Consumption - Common

Symbol	Parameters		Conditions	Min	Typ	Max	Unit
I_{idle}	System state: **active**	HPS mode (DC/DC Off)	App. processor: idle radio and sensors: not active		1.3		mA
			App. processor running @ 64 MHz from RAM)		3.3		
			App. processor running @ 64 MHz from NVM cache		2.8		
			App. processor running @ 192 MHz from RAM		6.5		
			App. processor running @ 192 MHz from NVM cache		5.1		
		eHPS mode (DC/DC On)	App. processor: idle, radio and sensors: not active		0.6		
			App. processor running @ 64 MHz from RAM		1.2		
			App. processor running from NVM cache @ 64 MHz		1.2		
			App. processor running from RAM @ 192 MHz		2.2		
			App. processor running from NVM cache @ 192 MHz		1.9		
$I_{standby}$	System state: **sleep**	LPS mode (DC/DC Off)	64 kHz LjRC clock				µA
			32 KB RAM retained		1.8		
			128 KB RAM retained		4.4		
			256 KB RAM retained		TBD		
		eLPS mode (DC/DC On)	64 kHz LjRC clock				
			32 KB RAM retained		0.9		
			128 KB RAM retained		1.8		
			all RAM retained		4.5		
		eHPSret mode (DC/DC Off)	32 MHz sleep		400		
		eHPSret mode (DC/DC On)			200		
	(Current consumption depends on crystal specification and load capacitance.						
I_{reset}	**Reset Mode**				50		µA

Current consumption while app. processor is running depends on the user program. Given numbers are max currents for reference program used. (typical xtal 32 MHz running)

Table 12: Current Consumption - Active State - Bluetooth Low Energy - VDD =3 V

Symbol						Protocol		VDD					
I_{active}						Bluetooth Low Energy		3 V					
Single Antenna								Dual Antenna / Diversity					
DC/DC On			DC/DC Off					DC/DC On			DC/DC Off		
Min	Typ	Max	Min	Typ	Max	Condition	Unit	Min	Typ	Max	Min	Typ	Max
	2.2			5.5		RX listening* 1 Mbit/s	mA		3.1			8.5	
	2.2			5.5		RX listening* 2 Mbit/s			3.1			8.5	
	2.2			6		RX listening* 500 kbit/s			3.5			8.5	
	2.2			6		RX listening* 125 kbit/s			3.5			8.5	
	TBD			TBD		RX listening* multi-rate**			TBD			TBD	
	2.4			5.7		RX receiving packet, all modes except 125 kbit/s			3.5			8.5	
	2.45			5.9		RX receiving packet, 125 kbit/s			3.55			8.7	
	6			14		Tx @ 0 dBm	mA		6			14	
	7.5			18.5		Tx @ 4 dBm			7.5			18.5	
	19			48		Tx @ 10 dBm			19			48	

Notes:* “RX listening” is defined as receive mode during preamble hunt.
Digital current included, application controller not running.
** Multi-rate includes 1 Mbit/s, 500 kbit/s and 125 kbit/s (not 2 Mbit/s).

Table 13: Current Consumption - Active State – IEEE 802.15.4 – channel 20, VDD =3 V

Symbol						Protocol		VDD					
I_{active}						IEEE 802.15.4		3 V					
Single Antenna								Dual Antenna / Diversity					
DC/DC On			DC/DC Off					DC/DC On			DC/DC Off		
Min	Typ	Max	Min	Typ	Max	Condition	Unit	Min	Typ	Max	Min	Typ	Max
	1.25			3		RX listening* single-channel	mA		2.2			5.5	
	2.3			6		RX listening* high sensitivity mode			3.3			8.5	
	2.3			6		RX listening* multi-channel			3.3			8.5	
	2.4			5.8		Rx receiving packet			3.4			8.3	
	6			14		Tx @ 0 dBm	mA		6			14	
	7.5			18.5		Tx @ 4 dBm			7.5			18.5	
	19			45		Tx @ 10 dBm			19			45	

Notes:* “RX listening” is defined as receive mode during preamble hunt.
Digital current included, application controller not running.

Table 14: Current Consumption - Active State – ConcurrentConnect Multi-Radio – channel 20, VDD= 3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{active}	RX listening* Bluetooth Low Energy 1 Mbit/s only	DC/DC On		2.3		mA
	RX listening* Bluetooth Low Energy 1 Mbit/s + 125/500 kbit/s	DC/DC On		2.3		
	RX listening* Bluetooth Low Energy 1 Mbit/s only	DC/DC Off		6		
	RX listening* Bluetooth Low Energy 1 Mbit/s + 125/500 kbit/s	DC/DC Off		6		
	Notes:* "RX listening" is defined as receive mode during preamble hunt. Digital current included, application controller not running. Single antenna.					

11.4 Receiver Characteristics

Table 15: Receiver Characteristics - Common

Parameter	Conditions		Min	Typ	Max	Unit
RSSI range * (assuming the HAL is used, see section 6.1.3) Note: * lowest RSSI value is below sensitivity level.	5 dB accuracy	AGC activated	-110		0	dBm
	Resolution			1		dB
LO leakage	2.4 GHz				-70	dBm
	4.8 GHz				-70	

Table 16: Receiver Characteristics - IEEE 802.15.4

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Programmable in 5 MHz steps as defined by IEEE 802.15.4	2405		2480	MHz
Data rate			250		kbit/s
Receiver sensitivity	Single-Channel Mode (Measured in IEEE 802.15.4 channel 20)				
	single antenna		-99		dBm
	antenna diversity		-98.5		
	High Sensitivity Mode (Measured in IEEE 802.15.4 channel 20)				
	single antenna		-102		dBm
	antenna diversity		-101		
	Multi-Channel Mode (Measured in IEEE 802.15.4, 3 channels				
	single antenna		-98.5		dBm
	antenna diversity		-96		
	Antenna Diversity Gain (refer to section 6.1.5 for the channel model)		8		dB
RX carrier frequency offset range	Sensitivity loss < 1 dB	-220		+220	kHz
Maximum receive level	1% PER as defined in IEEE 802.15.4	+10			dBm
IIP3	RX mode, AGC enabled		25		dBm
P-1dB RF front-end	RX mode, AGC enabled		0		dBm
Adjacent channel rejection	as defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 5 MHz		32		dB
Alternate adjacent channel rejection	as defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 10 MHz		46		dB
Far away channel rejection	wanted signal at -82 dBm. IEEE 802.15.4 interferer, +/- 15 MHz		50		dB
Wi-Fi IEEE 802.11n rejection	wanted signal at -82 dBm; Wi-Fi centered at +12 MHz / -13 MHz or higher offset frequency		30		dB
Bluetooth rejection (fixed carrier, rejection of FSK modulated signal with frequency deviation +/- 160 kHz, BT=0.5)	wanted signal at -82 dBm, Bluetooth carrier at:				
	+/-4 MHz		30		dB
	+/-6 MHz		52		
Blocking / desensitization (e.g., mobile phone signal rejection)	(Measured according to ETSI EN 300 440-1 V1.6.1; 2010-08).				
	-100 MHz from lower band edge		-11		dBm
	-40 MHz from lower band edge		-13		
	-20 MHz from lower band edge		-14		
	+20 MHz from upper band edge		-14		
	+40 MHz from upper band edge		-12		
	+100 MHz from upper band edge		-10		

Table 17: Receiver Characteristics - Bluetooth Low Energy

Parameter		Conditions	Min	Typ	Max	Unit
RF channels		Channel spacing in 2 MHz steps	2402		2480	MHz
Frequency error tolerance			-250		250	kHz
Bit rates	(LE 1M)			1		Mbit/s
	(LE Coded)			125 and 500		kbit/s
	(LE 2M)			2		Mbit/s
Data rate error tolerance			-500		+500	ppm
Receiver sensitivity		* (RF-PHY/RCV-LE/CA/BV-01-C); BER = 10^{-3} (Measured in Bluetooth channel 0 = 2402 MHz)				dBm
		2 Mbit/s data rate		-94.5		
		1 Mbit/s data rate		-97.5		
		500 kbit/s		-100.5		
		125 kbit/s		-105		
Receiver saturation		* (RF-PHY/RCV-LE/CA/BV-06-C); BER = 10^{-3}		>+10		dBm
Co-Channel rejection		Wanted signal at -67 dBm, modulated interferer in channel, BER = 10^{-3} (1 Mbps / 2 Mbps)		-9		dB
		Wanted signal at -72 dBm, modulated interferer in channel, BER = 10^{-3} (500 kbps)		-9		
		Wanted signal at -79 dBm, modulated interferer in channel, BER = 10^{-3} (125 kbps)		-9		
Selectivity		* (RF-PHY/RCV-LE/CA/BV-03-C); Wanted signal at -67 dBm, BER = 10^{-3}, (1 Mbps / 2 Mbps) modulated interferer at:				dB
		-5 MHz or more		54		
		-4 MHz		52		
		-3 MHz		50		
		-2 MHz		38		
		-1 MHz		5		
		+1 MHz = image frequency -1 MHz		5		
		+2 MHz = image frequency		33		
		+3 MHz = image frequency +1 MHz		44		
		+4 MHz = image frequency		52		
		+5 MHz or more		54		

Parameter	Conditions	Min	Typ	Max	Unit
Selectivity	* (RF-PHY/RCV-LE/CA/BV-03-C); For 125 kbps: wanted signal at -79 dBm, BER = 10^{-3}. For 500 kbps: wanted signal at -72 dBm, BER = 10^{-3}. Modulated interferer at:				
	-5 MHz or more		56		dB
	-4 MHz		52		
	-3 MHz		48		
	-2 MHz		37		
	-1 MHz		7		
	+1 MHz = image frequency -1 MHz		7		
	+2 MHz = image frequency		33		
	+3 MHz = image frequency +1 MHz		44		
	+4 MHz = image frequency		52		
	+5 MHz or more		56		
Out-of-band blocking	* (RF-PHY/RCV-LE/CA/BV-04-C);				
	30 ... 2000 MHz		-8		dBm
	2003 ... 2399 MHz		-6		
	2484 ... 2997 MHz		-5		
	3000 MHz ... 12.75 GHz		3		
Intermodulation	* (RF-PHY/RCV-LE/CA/BV-05-C); Wanted signal at 2402 MHz, at -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level.		-28		

Note: * As defined in Bluetooth Test Specification RF-PHY.TS.5.0.1, and for 1 Mbit/s bit rate.

Table 18: Receiver Characteristics - ConcurrentConnect Multi-Radio Mode

Parameter	Conditions	Min	Typ	Max	Unit
Receiver Sensitivity	1 Mbps		-97.5		dBm
	500 kbps		-100.5		
	125 kbps		-100.5		
	IEEE 802.15.4		-97		

11.5 Transmitter Characteristics

Table 19: Transmitter Characteristics - Common

Parameter	Conditions	Min	Typ	Max	Unit
Maximum TX output power			10		dBm
Minimum TX output power	Active TX		-25		dBm
TX output power variation	Over full temperature range *		3		dB
	Over full power supply voltage range		0.1		
	Over Tx frequency		1		
	Part to part variation (+/-3σ)		TBD		
TX Harmonics	Conducted measurement at max. output power (1 MHz resolution bandwidth, average power and modulated carrier)		-41		dBm
TX out of band emissions	Measured at max. output power, modulated signal, on all IEEE 802.15.4 and Bluetooth channels. (1 MHz resolution bandwidth, average power)				
	< 2390 MHz		< -41		dBm
	> 2483.5 MHz		< -41		
	Note: * TX output power variation over full temperature range is with no calibration. Device does not require any TX power calibration.				

Table 20: Transmitter Characteristics - IEEE 802.15.4

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Programmable in 5 MHz steps as defined by IEEE 802.15.4	2405		2480	MHz
Data rate			250		kbit/s
Chip rate			2.0		Mchip/s
Offset EVM	Channel 11-24: Dirac impulse digital filter		0.5		%
	Channel 25-26: Gaussian digital filter (for spectral mask to meet FCC band-edge requirements at max. Tx power)		1.5		

Table 21: Transmitter Characteristics - Bluetooth Low Energy

Parameter		Conditions		Min	Typ	Max	Unit
RF channels		Channel spacing in 2 MHz steps		2402		2480	MHz
Bit rates	(LE 1M)				1		Mbit/s
	(LE Coded)				125 and 500		kbit/s
	(LE 2M)				2		Mbit/s
In-band emissions		* (RF-PHY/TRM-LE/CA/BV-03-C)					
		+/-2 MHz			TBD		dBm
		+/-(3+n) MHz (n=0,1,2…)			TBD		
Frequency deviation		* (RF-PHY/TRM-LE/CA/BV-06-C)					
		$\Delta f1_{avg}$	1 Mbit/s	225		275	kHz
		$\Delta f2_{avg}$ / $\Delta f1_{avg}$	1 Mbit/s		>0.92		
		$\Delta f1_{avg}$	2 Mbit/s	450		550	kHz
		$\Delta f2_{avg}$ / $\Delta f1_{avg}$	2 Mbit/s		>0.92		

Note: * As defined in Bluetooth Test Specification RF-PHY.TS.5.0.1, and for 1 Mbit/s bit rate unless specified otherwise.

11.6 Digital Timing Characteristics

Table 22: SPI Slave Timing Characteristics

Symbol	Parameter	Reference (Figure 12)	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency	t1	0		16	MHz
	SCLK duty cycle clock			50		%
	MOSI setup time	t2	10			ns
	MOSI hold time	t3	10			ns
	SCLK low to MISO valid time	t4			16	ns
	SSn setup time	t5	31.25			ns
	SSn high to MISO tri-state	t6			31.25	ns

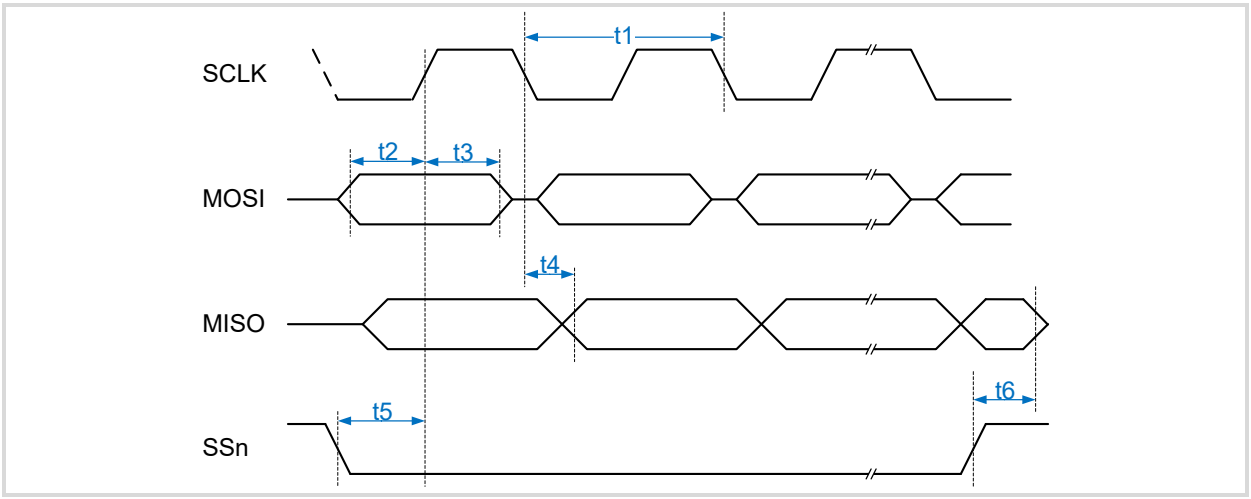


Figure 12: SPI Slave Signaling Timing Diagram

Table 23: I²C Timing Characteristics

Symbol	Parameter	Reference (Figure 13)	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
F_{SCL}	SCL frequency	t1		100		400	kHz
t_{HIGH}	Clock High Time	t2	4		0.6		µs
t_{LOW}	Clock Low Time	t3	4.7		1.3		µs
$t_{SU;STA}$	START condition setup time	t4	4		0.6		µs
$t_{HD;STA}$	START condition hold time	t5	4.7		0.6		µs
$t_{HD;DAT}$	Data hold time	t6	0		0		µs
$t_{SU;DAT}$	Data setup time	t7	0.25		0.1		µs
$t_{SU;STO}$	STOP condition setup time	t8	4		0.6		µs
t_{BUF}	Bus free time between a STOP and a START condition	t9	4.7		1.3		µs

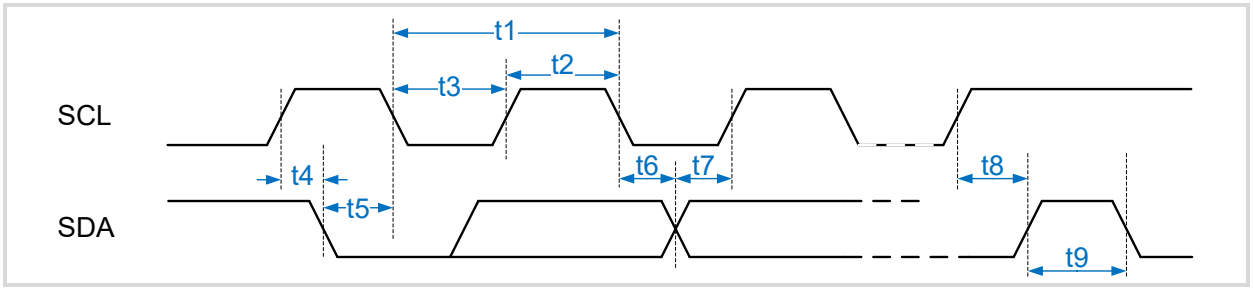


Figure 13: I²C Signaling Timing Diagram

11.7 Reset, Wake up and Sleep Timing Characteristics

Table 24: Reset, Wake up and Sleep Timing

Application use cases	Remarks	Min	Typ	Max	Unit
Power on detect	See Figure 14 below.		10		ms
From Power on detect, until application main function	See Figure 14 below.		45		ms
External Reset, until application main function	See Figure 15 below.		45		ms
RESETN pulse width	See Figure 14 below. The RESETN is asynchronous. A practical minimum is 10 ns.				
From sleep trigger in HPS mode until in LPS standby mode			200		µs
From sleep trigger in eHPS mode until in eLPS standby mode			253		µs
From sleep trigger in HPS mode until in HPSret standby mode			150		µs
Wake up from trigger in LPS mode until HPS back in main function			2		ms
Wake up from trigger in eLPS mode until eHPS back in main function			2.1		ms
Wake up from trigger in HPSret mode until HPS back in main function			216		µs

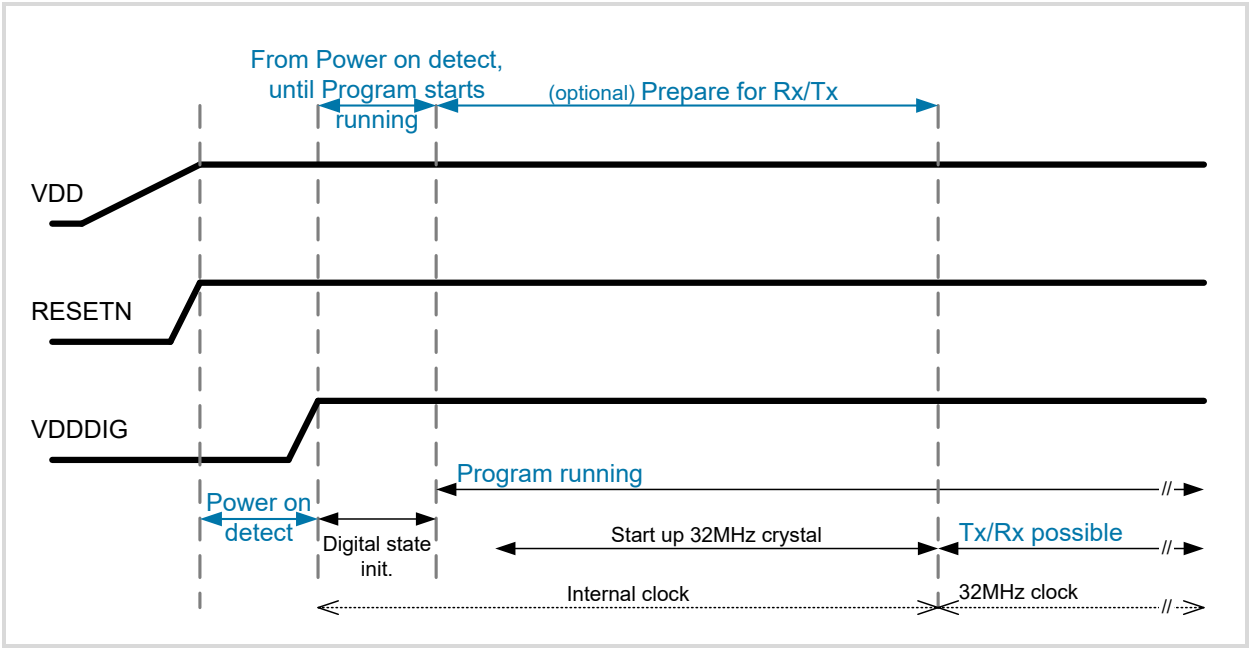


Figure 14: Power On Timing (not to scale)

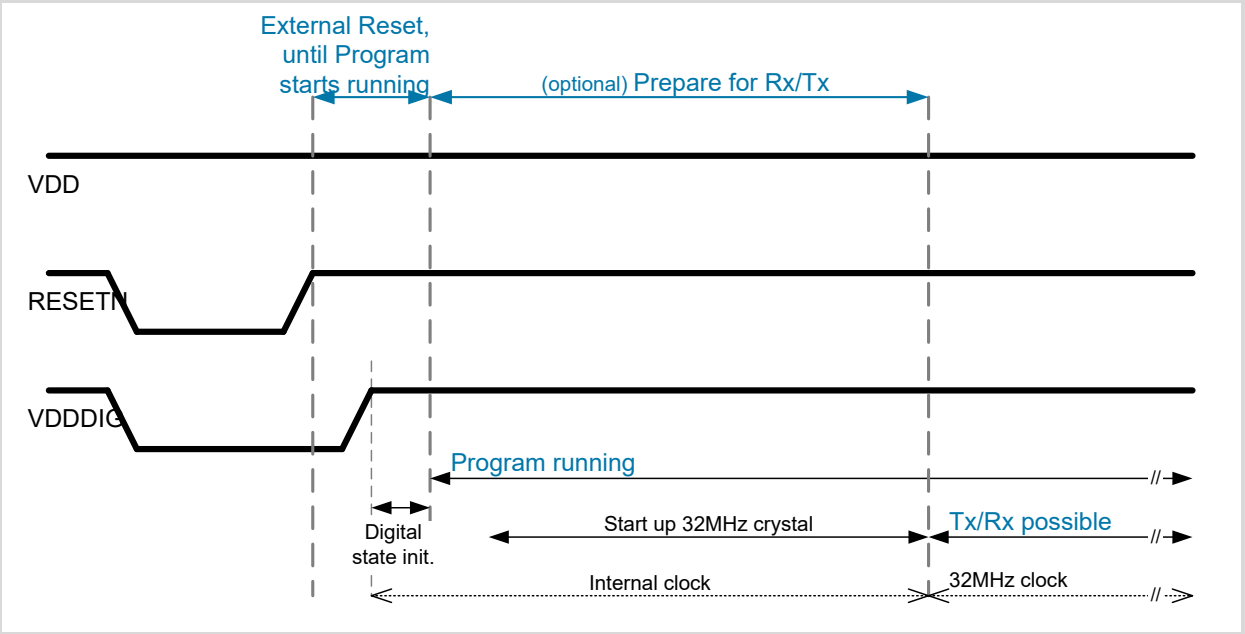


Figure 15: External Reset Timing (not to scale)

11.8 NVM Characteristics

Table 25: NVM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Retention period	85°C	10			year
	Number of ERASE cycles		10k			
	VDD for programming	Zero source resistance	1.8		3.6	V
	Data word size			128		bits
T_{WR}	Write time (1 word)	Physical operations, so excl. software overhead and transmission times		50		µs
I_{WR}	Write current	Average delta current		13		mA

11.9 Crystal Oscillator Specifications

11.9.1 32 MHz Crystal Oscillator

The 32 MHz crystal oscillator is an AGC controlled oscillator that provides a high gain at start-up, to assure fast start-up times, and low gain when running, to minimize current consumption. It generates the system clock for the QPG6200L and can also be used as time base generation.

For reliable operation, and to meet the specified Sleep current and startup time, the crystal should comply with the Qorvo Procurement Specifications for the crystal. These specifications, as shown in Table 26, will become available at Qorvo's website soon.

Qorvo's *Crystal Procurement Tool* (available soon) can be used to check if the electrical parameters, given in the crystal specification, can meet Qorvo procurement requirements. If needed, a header file for frequency offset compensation over temperature can be extracted.

Table 26: 32 MHz Crystal Specifications

Package	Size	Type	Procurement Specification
SMD	3.2 x 2.5 mm	4 pads SMD	GP_P010_PS_20298
SMD	2.0 x 1.6 mm	4 pads SMD	GP_P010_PS_20299
SMD	1.6 x 1.2 mm	4 pads SMD	GP_P010_PS_20300

Figure 16 below shows the typical configuration of the oscillator.

The QPG6200L features internal programmable crystal load capacitors that can be set from 13.2 - 25 pF each.

Note that the values of the internal and optional external load capacitors (Cx, Cy) are crystal type dependent.

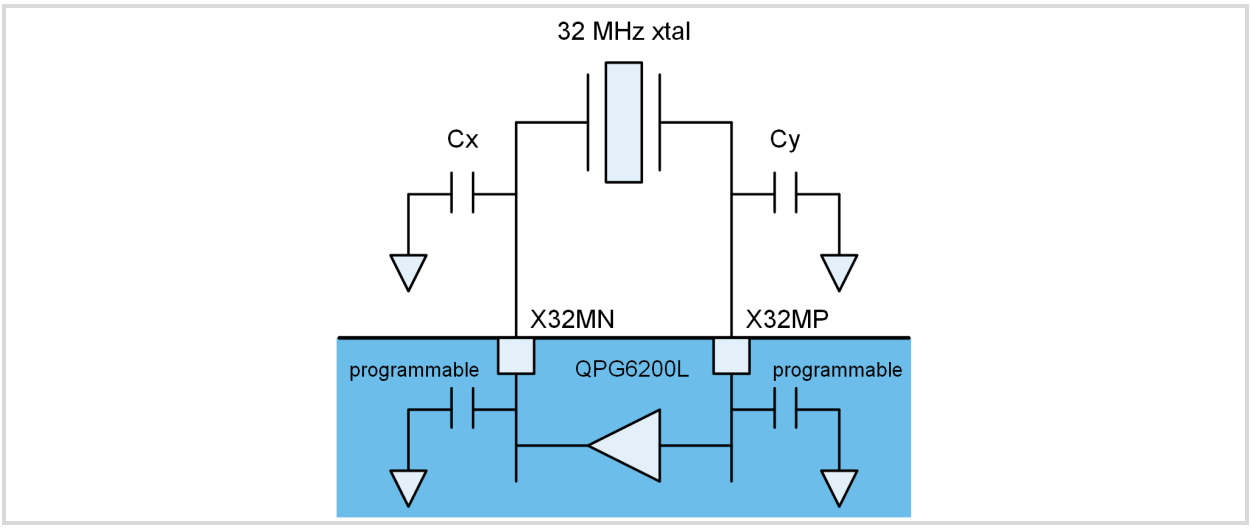


Figure 16: Typical 32 MHz Crystal Configuration

11.9.2 32 KiHz Crystal Oscillator (optional)

The 32.768 kHz (in short: 32 KiHz) crystal oscillator is optional and can be used for ultra-low power time base generation for the Event Scheduler with high accuracy. A side effect of this low power consumption is that the start-up time of the 32 KiHz oscillator is very dependent on the crystal and the capacitive load on the X32K oscillator pins.

Within the operational temperature range, the 32 KiHz oscillator will always start within one second (at 25°C the start-up time is less than 0.5 s). The application must make sure that the QPG6200L does not enter the 32 KiHz Sleep mode before the 32 KiHz oscillator is stable.

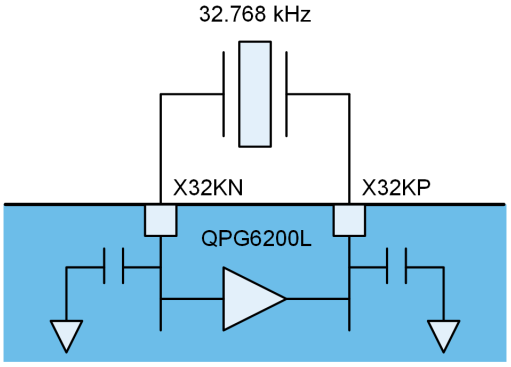


Figure 17: 32 KiHz Crystal Configuration

For reliable operation and to meet the specified characteristics, the crystal should comply with Qorvo Procurement Specification GP_P010_PS_20408. This specification will become available at Qorvo's website soon.

Figure 17 above shows the application circuit of this oscillator.
Note: the crystal load capacitors are integrated in the chip.

11.10 Internal Pull-up / Pull-down Characteristics

Table 27: Internal Pull-up / Pull-down Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Internal pull-up resistance	VDD=3.3V, T_A=25°C, Input is grounded.		41		kΩ
		VDD=1.71V, T_A=25°C, Input is grounded.		99		
	Internal pull-down resistance	VDD=3.3V, T_A=25°C, Input is VDD level.		42		
		VDD=1.71V, TA=25°C, Input is VDD level.		115		

11.11 ADC Characteristics

Table 28: General Purpose ADC Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	Sample rate			0.04		1	MS/s
	Resolution	Sample rate up to 1 MS/s			11		bits
		Oversampling ratio (OSR) = 16			13		bits
V_{IN}	Measurement range	At ANIO pin	single ended	0		VDD	V
			differential	-VDD		VDD	
	Channel Switching Time				4		µs
SNR	Signal-to-Noise Ratio	Single ended, 1.07 MS/s			50.5		dB
		Differential, 1.07 MS/s			56.5		
INL	Integral Nonlinearity	Single ended, OSR = 1024			2		LSb
		Differential, with chopping, OSR = 512			1		
DNL	Differential Nonlinearity	Differential measurement		> -1			LSb

Table 29: High-Resolution ADC – General Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	Sample rate			3.9		15.6	kSps
	Oversampling ratio			64		256	
	Resolution				16		bits
V_{IN}		At the ANIO pin	single-ended	0		VDD	V
			differential	-VDD		VDD	

Table 30: High-Resolution ADC - SNDR and Nonlinearity Characteristics

Symbol	Parameter	Conditions	Typ	Typ	Typ	Typ	Unit
SNDR	Measurement range (*)	Scaler gain	**1/4x**	**1x**	**4x**	**8x**	
		Single-ended	0 to +VDD	0 to +1 V	0 to +0.25 V	0 to +0.125 V	dB
		Differential	-VDD to +VDD	-1V to +1 V	-0.25 V to +0.25 V	-0.125 V to +0.125 V	
	Signal-to-(Noise +Distortion) Ratio	Single ended	77	77	77	77	
		Differential	TBD	TBD	TBD	TBD	
INL	Integral Nonlinearity	OSR = 256	8	8	8	8	LSb
		Differential measurement, OSR = 256	TBD	TBD	TBD	TBD	
DNL	Differential Nonlinearity	Differential measurement	>-2	>-2	>-2	>-2	LSb

Note (*): the ADC contains a scaler, which allows several measurement ranges.

11.12 Battery and Temperature Monitor Characteristics

Table 31: Battery Monitor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Battery level range		1.71		3.6	V
	Resolution of battery level measurement			10		mV
	Accuracy of battery level measurement	Max over process, voltage and temperature.		25	60	mV

Table 32: Temperature Monitor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Temperature measurement range		-40		+125	°C
	Resolution of temperature measurement			0.15		
	Accuracy of temperature measurement			3		
	Temperature measurement conversion time			128		µs

11.13 DC/DC Converter Information

Table 33: DC/DC Converter Information

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_DCDC	Inductance of DCDC inductor			3.3		µH
Eff_{DCDC}	Efficiency	L_DCDC= 3.3 µH (10 mA load)		85		%

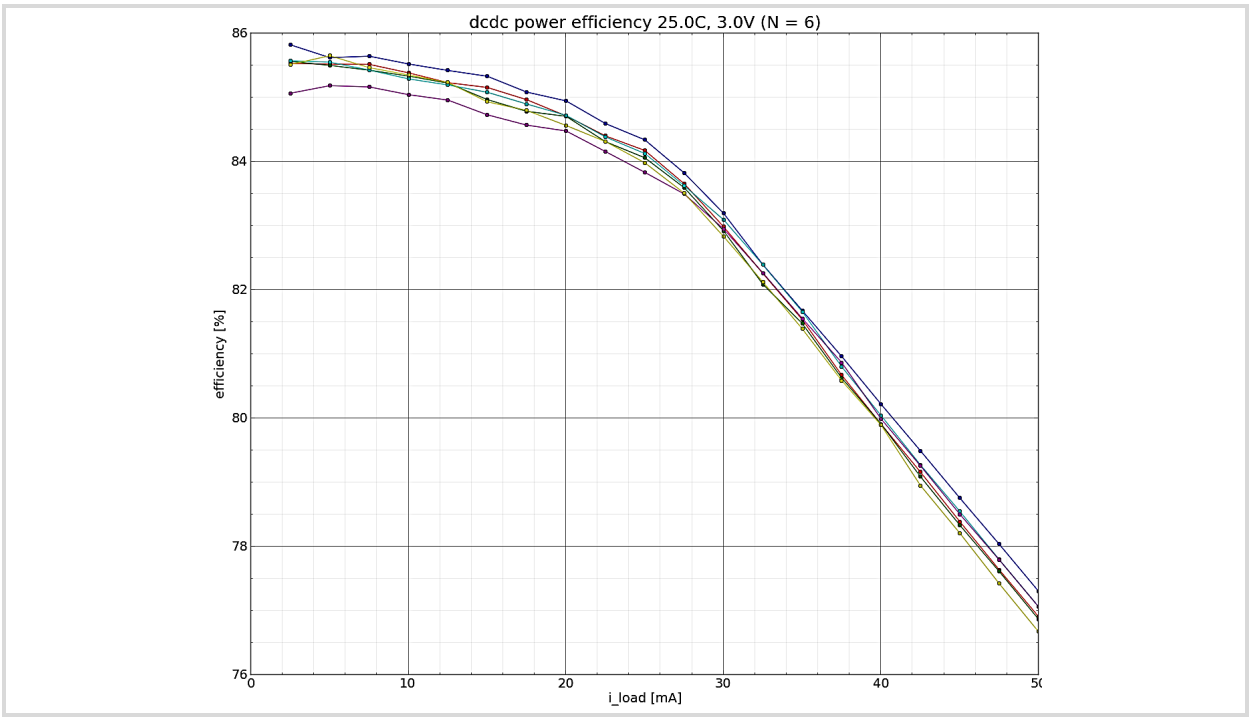


Figure 18: DCDC Converter Efficiency at Higher Current Loads

11.14 GPIO0 High Drive Sink Characteristics

Table 34: High Drive Sink Characteristics

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
I_{MAX}	Current handling	Advised max current, going beyond may reduce lifetime and might cause failure or increased leakage			600	mA
I_{OFF}	Off / leakage current	Leakage current when driver is not sinking current		0.5		µA
R_{ON}	On resistance	Equivalent resistance when driver is sinking current		0.8		Ω
T_{RISE}	Rise time of the current	Time to reach 90% of the target end voltage. Measured with VDD = 3.6 V and external load resistor of 5 Ω (resulting to a 600 mA current when active).		50		ns
V_{OL}	Output Low Voltage	At 600 mA continuous current				
		VDD = 1.71 V		TBD		
		VDD = 3.0 V		0.50		V
		VDD = 3.6 V		0.45		

11.15 64 kHz LjRC Oscillator Characteristics

Table 35: 64 kHz LjRC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
64kRC-tolerance	Frequency stability	1σ value, TA=25°C, calibration performed at least every 2.5 s for an averaging period >1 ms		+/-100		ppm
64kRC-Tc	Temperature coefficient			< +/-100		ppm/K

12 Device Information

12.1 Package

12.1.1 Pin Assignments

Figure 19 below shows the (top view) pin connections for the QPG200L. Table 36 lists the pin assignments.

Table 37 and Table 38 provides GPIO assignment options for various functions. For the software configuration options of the GPIO pins, please refer to section 7.2 section and Table 36.

Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

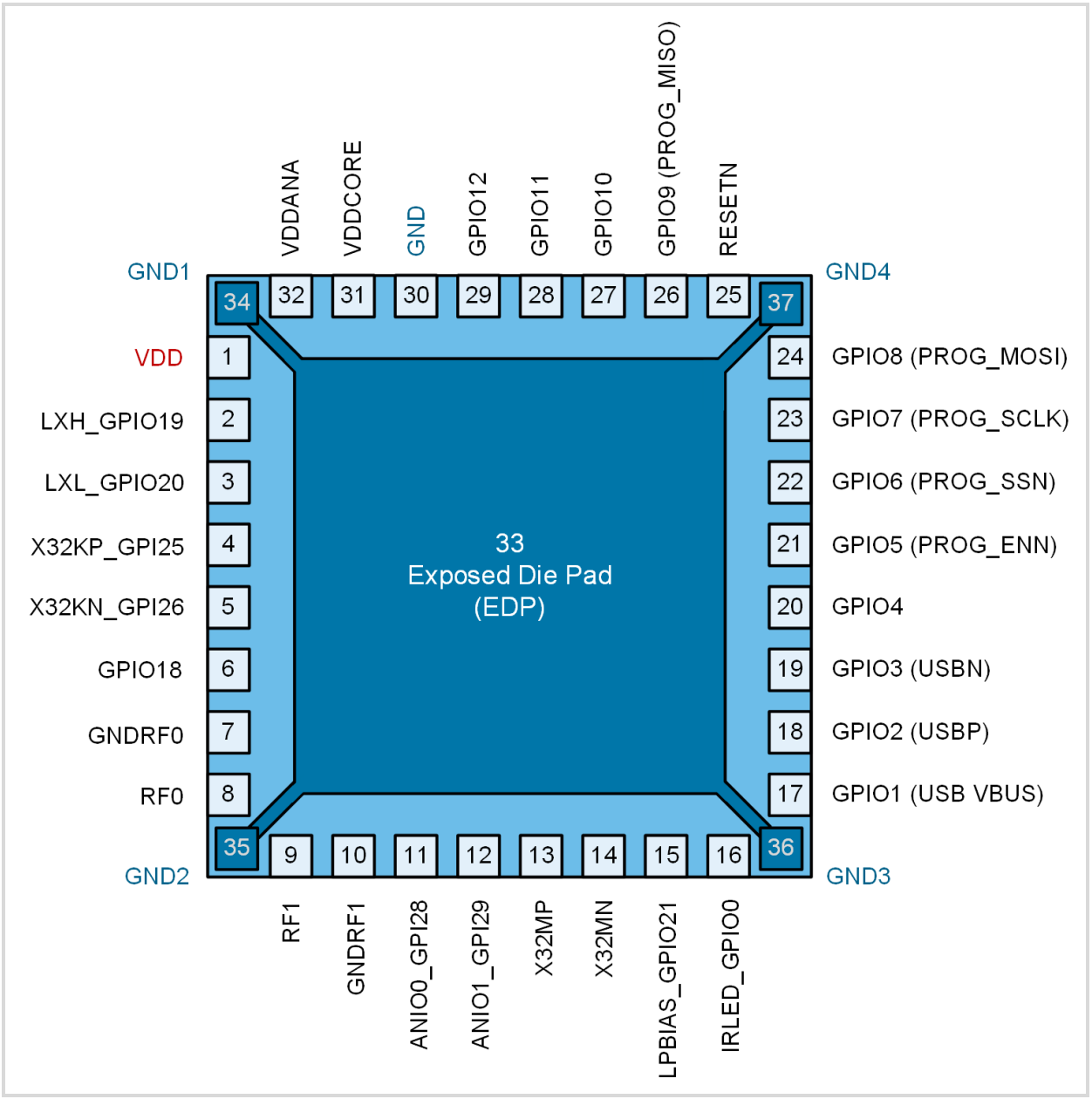


Figure 19: Pin Connections – Top View

Table 36: Pin Assignments

Pin #	Name	Type	Description	Notes
1	VDD	Power	Power supply input	
2	LXH_GPIO19	Power or Digital	Optional DC-DC converter output, or configurable GPIO	Connection to inductor for optional DC-DC converter. See sections 9.1 and 11.13.
3	LXL_GPIO20	Power or Digital	Optional DC-DC converter output, or configurable GPIO	
4	X32KP_GPI25	Analog or Digital	Optional 32 KiHz reference xtal input, or configurable digital input	Both pins should either be used for the 32 KiHz reference crystal or defined as GPIO. If a pin is not used, it must be connected to the Exposed Die Pad (GND) or software should disable the input buffer, to prevent leakage current. If defined as GPIO, apply external pull up or pull down to avoid floating input. No internal pull-up or pull-down capability.
5	X32KN_GPI26	Analog or Digital	Optional 32 KiHz reference xtal output, or configurable digital input	
6	GPIO18	Digital	Configurable GPIO	
7	GNDRF0	RF	RF0 ground return	Must be connected to the Exposed Die Pad (GND). Preferably with a top-level trace.
8	RF0	RF	RF port 0 for antenna	In all cases the RF pins should be isolated from ground or VDD.
9	RF1	RF	RF port 1 for antenna	
10	GNDRF1	RF	RF1 ground return	Must be connected to the Exposed Die Pad (GND). Preferably with a top-level trace.
11	ANIO0_GPI28	Analog or Digital	ADC's input, or configurable GPIO (input only)	ANIO pins that are not used, are recommended to be connected to the Exposed Die Pad (GND).
12	ANIO1_GPI29	Analog or Digital	ADC's input, or configurable GPIO (input only)	
13	X32MP	Analog	32 MHz reference crystal input	The QPG6200L does not support an external clock.
14	X32MN	Analog	32 MHz reference crystal ground	
15	LPBIAS_GPIO21	Analog or Digital	Programmable Low Power bias voltage, or configurable GPIO	
16	IRLED_GPIO0	Digital	Configurable GPIO	GPIO has High Drive function, e.g., for IR LED. Up to 600 mA output drive strength.
17	GPIO1 (USB VBUS)	Digital	Configurable GPIO	USB VBUS
18	GPIO2 (USBP)	Digital	Configurable GPIO	Also serves as USB differential data D+.
19	GPIO3 (USBN)	Digital	Configurable GPIO	Also serves as USB differential data D-.
20	GPIO4	Digital	Configurable GPIO	
21	GPIO5 (PROG_ENN)	Digital	Configurable GPIO	Also serves as PROG_ENN.
22	GPIO6 (PROG_SSN)	Digital	Configurable GPIO	Also serves as PROG_SSN.
23	GPIO7 (PROG_SCLK)	Digital	Configurable GPIO	Also serves as PROG_SCLK.

Pin #	Name	Type	Description	Notes
24	GPIO8 (PROG_MOSI)	Digital	Configurable GPIO	Also serves as PROG_MOSI.
25	RESETN	Digital	Active-low reset circuit	Internally pulled up, so no external pull up is required. This pin shall be available for NVM programming, see section 8.8.9.
26	GPIO9 (PROG_MISO)	Digital	Configurable GPIO	Also serves as PROG_MISO.
27	GPIO10	Digital	Configurable GPIO	
28	GPIO11	Digital	Configurable GPIO	
29	GPIO12	Digital	Configurable GPIO	
30	GND	Digital	Ground	Connected to Exposed Die Pad for ESD.
31	VDDCORE	Analog	Digital core voltage decoupling	Decoupling to ground.
32	VDDANA	Analog	Analog voltage decoupling	Decoupling to ground.
33	EDP	Ground	Exposed Die Pad	Analog chip ground.
34	GND1	Ground	Additional ground connections, internally connected to EDP via the lead frame.	Available for easier ground routing.
35	GND2	Ground		
36	GND3	Ground		
37	GND4	Ground		

For the software configuration options of the GPIO pins, please refer to Table 37 and Table 38.

Unless specified otherwise, at power-up/reset all GPIO pins are default set to floating mode.

Table 37: GPIO Assignment Table – SPI / I2C / I2S / UART / PDM / SWD/JTAG / USB

Pin Name	Pin#	Wake Up	QSPI	SPI Master	SPI Slave	I²C Master_ 0/1	I²C Slave	I²S Master / Slave_0	I²S Master / Slave_1	UART 0 /1 / 2	PDM0 (mic)	PDM1 (mic)	SWD	JTAG	Trace	USB
GPIO**0**	16	x	SCLK	MOSI	-	SDA / -	SDA	SDO / WS_IN	-	TX / RX / TX	DATA	CLK	-	-	TRACE_CLK	-
GPIO**1**	17	x	IO_**0**	MISO	MISO	SCL / -	SCL	SDI / REF_IN	SDI / REF_IN	RX / TX / RX	CLK	DATA	SWDIO	TMS	TRACE_DATA_**0**	VBUS
GPIO**2**	18	x	IO_**2**	SSn	SSN	SDA / -	SDA	WS / WS_IN	WS / WS_IN	TX / RX / CTS	DATA	CLK	SWCLK	TCK	TRACE_DATA_**1**	DP (+)
GPIO**3**	19	x	IO_**1**	SCLK	SCLK	SCL / -	SCL	SCK / SCK_IN	SCK / SCK_IN	RX / TX / -	CLK	-	-	TDI	TRACE_DATA_**2**	DM (-)
GPIO**4**	20	x	IO_**3**	MOSI	MOSI	SDA / -	SDA	SDO / -	SDO / -	CTS / CTS / -	DATA	-	SWV	TDO	TRACE_DATA_**3**	-
GPIO**5**	21	x	SCLK	MISO	MISO	-	-	SDI / REF_IN	-	-	-	-	-	-	TRACE_CLK	-
GPIO**6**	22	x	IO_**0**	SSn	SSn	-	-	WS / WS_IN	-	-	-	-	SWDIO	TMS	-	-
GPIO**7**	23	x	IO_**2**	SCLK	SCLK	-	-	SCK / SCK_IN	-	-	-	-	SWCLK	TCK	-	-
GPIO**8**	24	x	IO_**1**	MOSI	MOSI	-	-	SDO / -	-	TX / RX / -	-	-	-	TDI	-	-
GPIO**9**	26	x	IO_**3**	MISO	MISO	-	-	SDI / -	-	RX / TX / -	-	-	SWV	TDO	-	-
GPIO**10**	27	x	SCLK	SSn	SSn	- / SDA	-	WS / WS_IN	-	TX / TX / TX	-	-	-	-	-	-
GPIO**11**	28	x	IO_**0**	SCLK	SCLK	SCL / SCL	-	SCK / SCK_IN	-	RX / RX / -	DATA	CLK	-	-	TRACE_CLK	-
GPIO**12**	29	x	IO_2	MOSI	MOSI	SDA / -	-	SDO / -	SDO / -	CTS / TX / RX	CLK	DATA	SWDIO	TMS	TRACE_DATA_**0**	-
GPIO**18**	6	x	-	-	-	SCL / SCL	SCL	SDI / -	-	TX / CTS / TX	-	CLK	-	-	-	-
GPIO**19**	2	-	IO_**1**	MOSI	-	SCL / -	SCL	SDO / -	-	- / - / RX	-	-	-	-	-	-
GPIO**20**	3	-	IO_**3**	MISO	-	SDA / -	SDA	SDI / -	-	- / - / TX	-	-	-	-	-	-
GPIO**21**	15	x	IO_3	SCLK	-	SCL / -	SCL	SCK / -	-	RX / TX / CTS	CLK	-	-	-	TRACE_DATA_**0**	-
GPI**25**	4	x	-	MISO	-	-	-	- / WS_IN	-	RX / - / CTS	-	-	-	-	-	-
GPI**26**	5	x	-	-	-	-	-	- / SCK_IN	-	- / - / CTS	-	DATA	-	-	-	-
GPI**28**	11	x	-	-	-	-	-	- / SCK_IN	-	-	-	DATA	-	-	-	-
GPI**29**	12	x	-	MISO	-	-	-	SDI / REF_IN	SDI / REF_IN	CTS / CTS / -	DATA	-	-	-	-	-

I²C bus signals (SCL, SDA) require external pull up.
I²S Master uses SDO, SDI, SCK, WS and optionally REF_CLK.
I²S Slave uses SDO, SDI, SCK_IN, WS_IN and optionally REF_CLK. WS_IN and SCK_IN may require external pull down to prevent floating input signals, depending on the behavior of the master device (e.g. during sleep state).

Table 38: GPIO Assignment Table – Keybd Scan / IR / PWMXL / LED / Clock Output / Antsw_Ctrl / Coex

Pin Name	Pin#	Wake Up	Keyboard Scan (column = input, row = output)	IR	PWMXL	LED Pixel Protocol Master	LED	Clock Output	Antsw_ Ctrl	Coex MS	Coex SL	Coex Attenuation
GPIO**0**	16	x	Column **7**	OUT (*)	PWMXL_**0**	- / TX	LED**0**	CLKGEN_**1**	-	COEX_MS_GRANTB	COEX_SL_REQ	-
GPIO**1**	17	x	Column **0**, Row **0**	-	PWMXL_**1**	-	LED**1**	-	-	COEX_MS_REQB	-	-
GPIO**2**	18	x	Column **1**, Row **1**	-	PWMXL_**2**	-	LED**2**	-	-	COEX_MS_PRIOB	-	-
GPIO**3**	19	x	Column **2,** Row **2**	-	PWMXL_**3**	-	LED**3**	-	-	-	-	-
GPIO**4**	20	x	Column **3**, Row **3**	OUT	PWMXL_**6**	-	-	CLKGEN_**1**	PHY_ANTSW_**2**	COEX_MS_REQA	COEX_SL_REQ_NOT	-
GPIO**5**	21	x	Column **4,** Row **4**	-	PWMXL_**7**	-	-	CLKGEN_**0**	-	COEX_MS_PRIOA	COEX_SL_PRIO_**0**	-
GPIO**6**	22	x	Column **5**, Row **5**	-	PWMXL_**0**	-	-	-	-	-	-	-
GPIO**7**	23	x	Column **6**, Row **6**	-	PWMXL_**1**	-	-	-	-	-	-	-
GPIO**8**	24	x	Column **7**, Row **7**	-	PWMXL_**2**	TX / -	-	-	-	-	-	-
GPIO**9**	26	x	Column **0**, Row **0**	-	PWMXL_**3**	- / TX	LED**3**	-	PHY_ANTSW_**2**	-	-	-
GPIO**10**	27	x	Column **1**, Row **1**	-	PWMXL_**4**	TX / -	LED**2**	CLKGEN_**0**	PHY_ANTSW_**3**	-	-	-
GPIO**11**	28	x	Column **2**, Row **2**	-	PWMXL_**5**	- / TX	LED**1**	CLKGEN_**1**	PHY_ANTSW_**0**	COEX_MS_GRANTB	COEX_SL_PRIO_**0**	-
GPIO**12**	29	x	Column **3**, Row **3**	OUT	PWMXL_**0**	TX / -	LED**0**	CLKGEN_**0**	PHY_ANTSW_**1**	COEX_MS_GRANTA	COEX_SL_REQ_NOT	-
GPIO**18**	6	x	Column **1**, Row **1** Row **4**	OUT	PWMXL_**0**	TX / -	LED**3**	CLKGEN_**0**	PHY_ANTSW_**2**	COEX_MS_GRANTB	COEX_SL_GRANT	COEX_ATT_CTRL_**2**
GPIO**19**	2	-	-	-	PWMXL_**5**	-	-	-	PHY_ANTSW_**2**		COEX_SL_PRIO_**1**	-
GPIO**20**	3	-	-	-	PWMXL_**0**	-		-	PHY_ANTSW_**3**		COEX_SL_REQ	-
GPIO**21**	15	x	Column **6**	OUT	PWMXL_**7**	TX / -	LED**3**	CLKGEN_**0**	-	COEX_MS_GRANTA	COEX_SL_PRIO_**1**	-
GPI**25**	4	x	Column **2**	-	-	-	-	-	-	COEX_MS_REQB	COEX_SL_GRANT	COEX_ATT_CTRL_**1**
GPI**26**	5	x	Column **3**	-	-	-	-	-	-	COEX_MS_PRIOB		COEX_ATT_CTRL_**2**
GPI**28**	11	x	Column **1**	-	-	-	-	-	-	COEX_MS_PRIOA		COEX_ATT_CTRL_**0**
GPI**29**	12	x	Column **2**	-	-	-	-	-	-	COEX_MS_REQA	COEX_SL_GRANT	COEX_ATT_CTRL_**1**

(*) GPIO0 is generally preferred for IR due to increased drive strength possibility of GPIO**0** (see sections 7.2 and 11.14) .

12.1.2 Package Drawing and Recommended Land Pattern

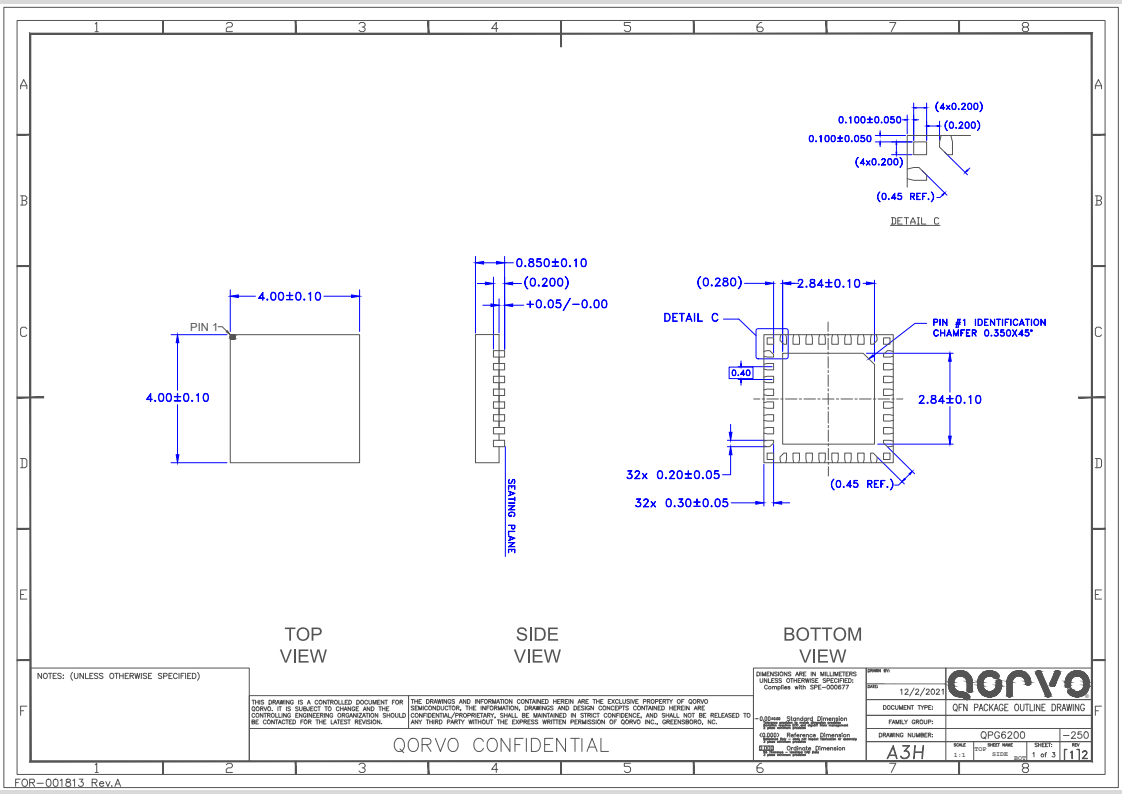


Figure 20: Package Drawing and Dimensions

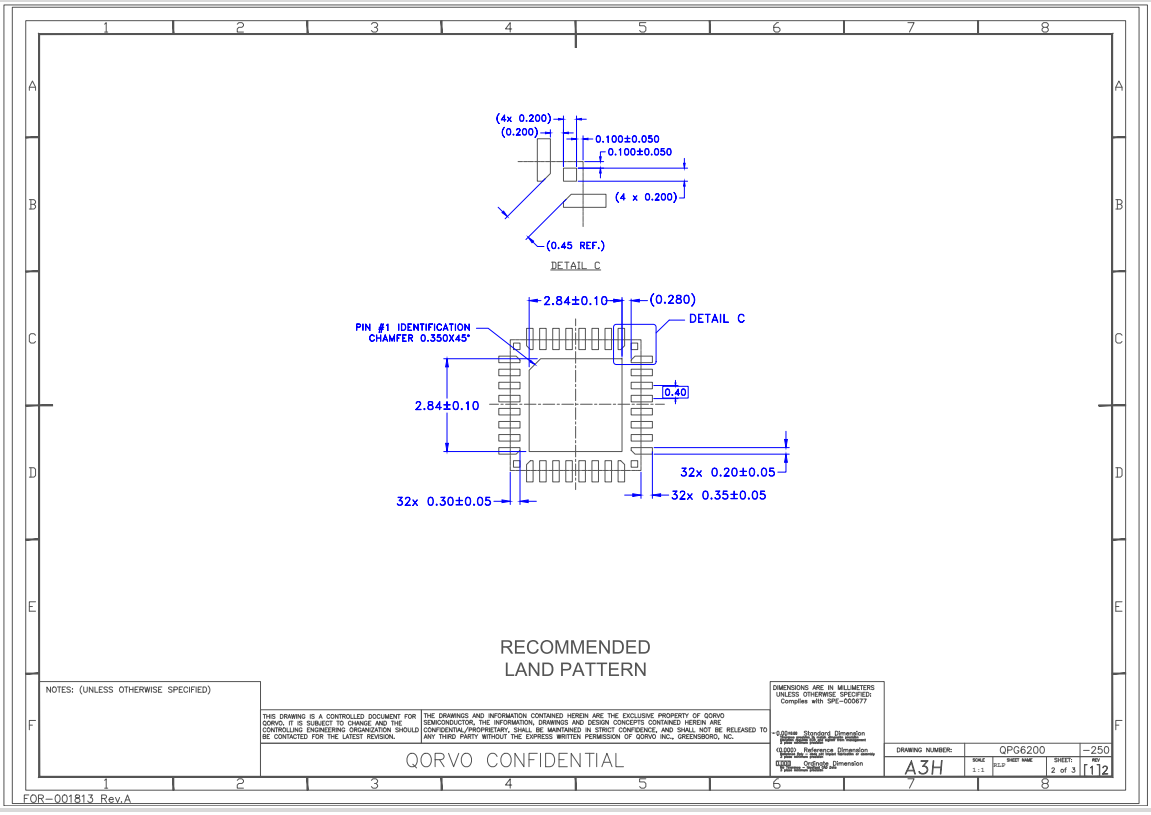


Figure 21: Recommended Land Pattern

12.1.3 Package Information

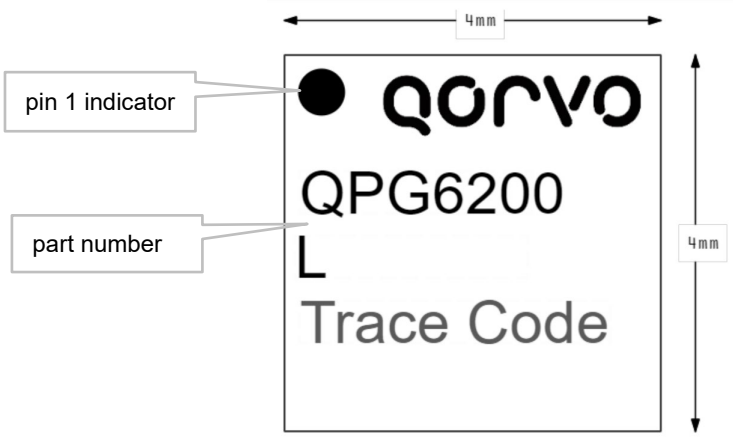


Figure 22: Package Information

Note: Product code = first 8 characters of the part number

12.1.4 Thermal Characteristics

Table 39: Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
Theta JA ($R_{\theta JA}$)	Thermal resistance from junction to ambient	JEDEC JESD 51-2; JEDEC 2S2P (4L) board as per JESD 51-7	40	K/W
Psi-JT (Ψ_{JT})	Junction-to-Top (of package) thermal characterization parameter	JEDEC JESD 51-12	15	K/W

12.1.5 Tape and Reel Information

12.1.5.1 Carrier and Cover Tape Dimensions

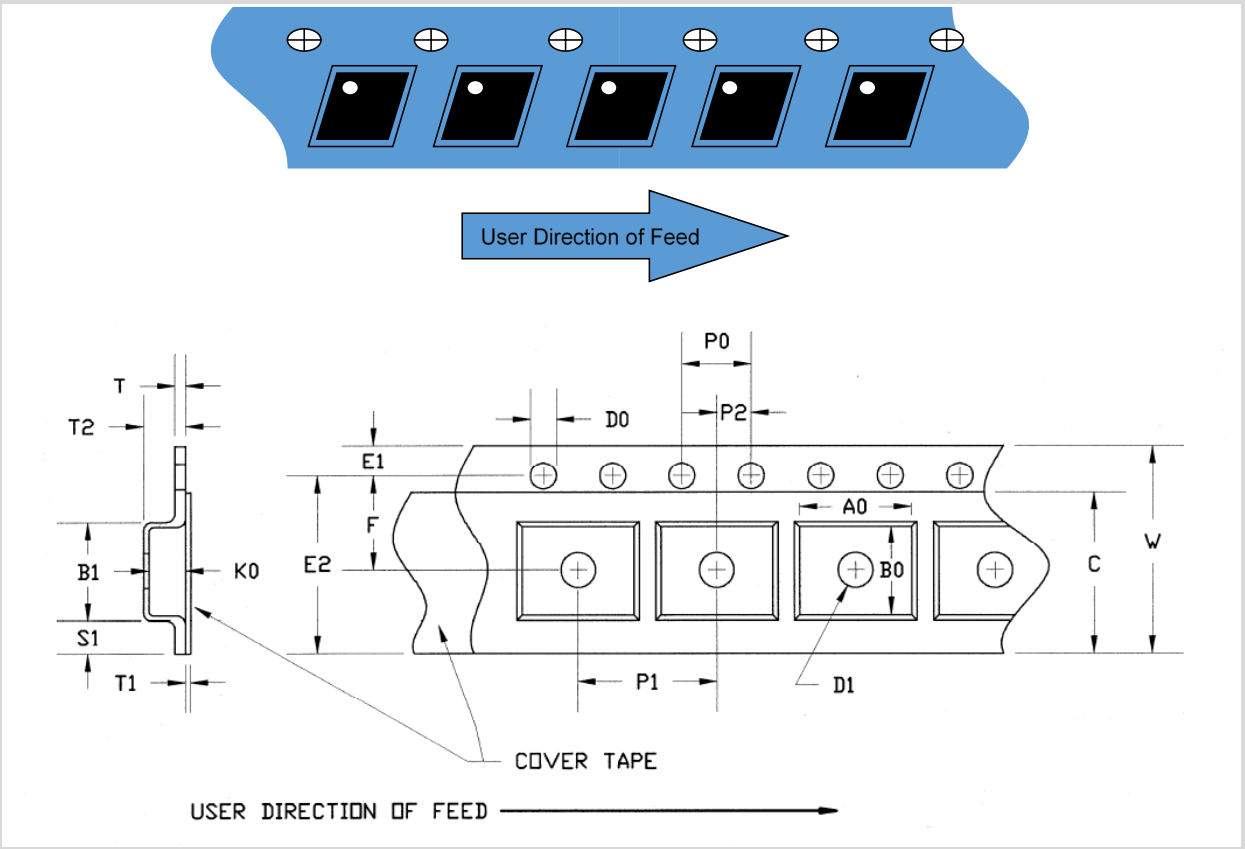


Figure 23: Carrier and Cover Tape Dimensions

Table 40: Carrier and Cover Tape Dimensions

Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.170	4.3
	Width	B0	0.170	4.3
	Depth	K0	0.049	1.25
	Pitch	P1	0.315	8.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

12.1.5.2 Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.

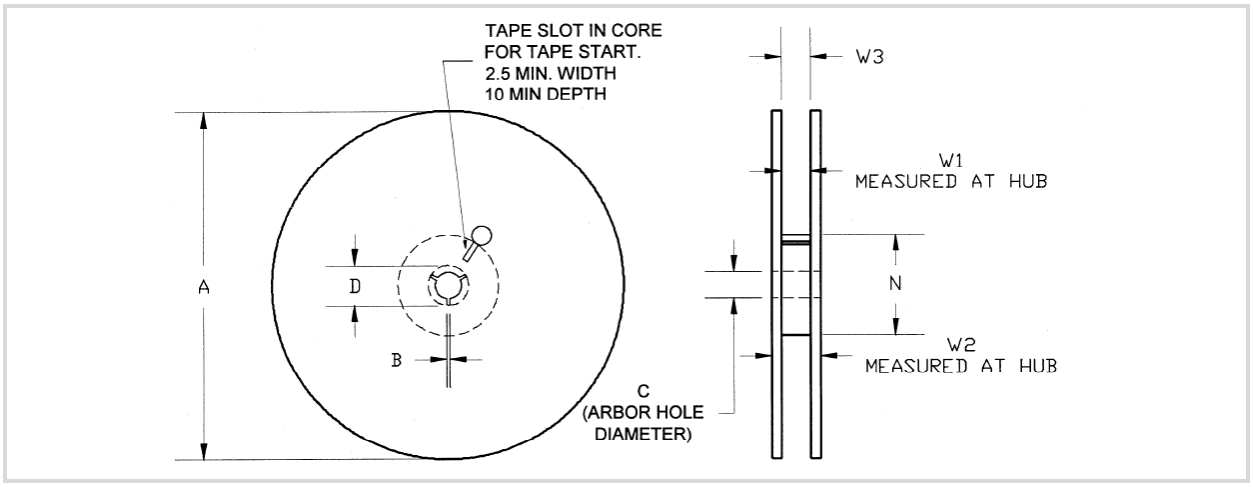


Figure 24: Reel Dimensions

Table 41: Reel Dimensions

Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

12.1.5.3 Tape Info and Label Placement

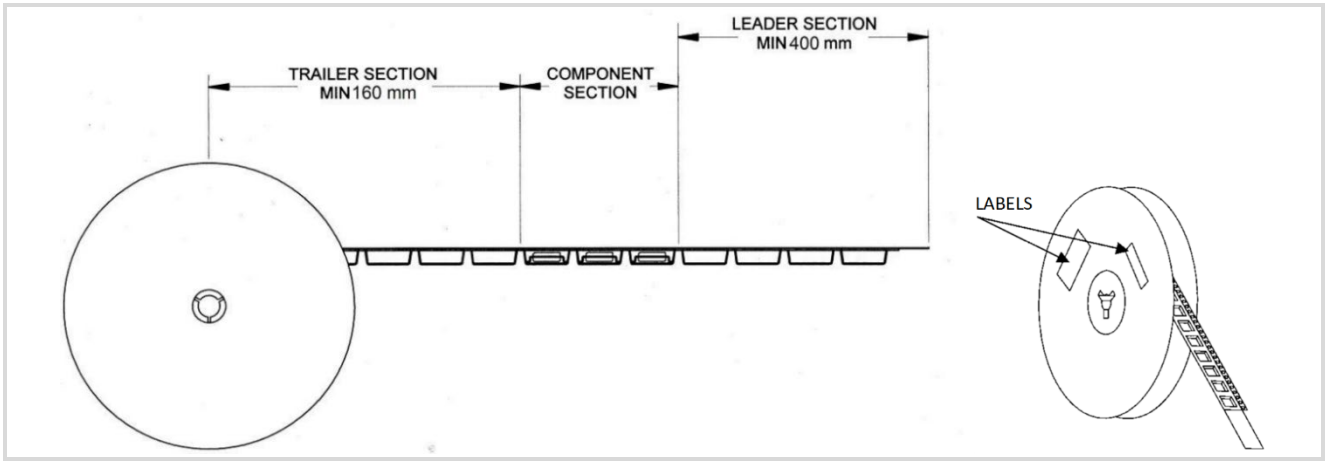


Figure 25: Tape and Labels

Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

12.2 Moisture/Reflow Sensitivity

Table 42: Moisture/Reflow Sensitivity

Symbol	Parameter	Conditions	Value	Unit
	Soldering Process		Pb-free	
T_c	Peak reflow temperature	10 s max.	260	°C
MSL	Moisture Sensitivity Level		3	
	The Moisture/Reflow Sensitivity is classified according to: IPC/JEDEC J-STD-020D.1 (March 2008) Joint Industry Standard; Moisture/Reflow Sensitivity Classification for Non-hermetic Solid-State Surface Mount Devices.			

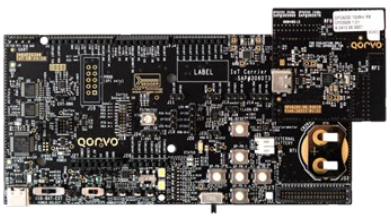
12.3 Environmental Compliance

Table 43: Environmental Compliance

Symbol	Attribute	Compliant
RoHS	Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment; Directives 2011/65/EU and 2015/863/EU.	✓
Pb	Lead Free	✓
	Halogen Free (Chlorine, Bromine)	✓
	Antimony Free	✓
	TBBP-A ($C_{15}H_{12}Br_4O_2$) Free	✓
	PFOS Free	✓
	SVHC Free	✓

13 Development Kit

Qorvo provides the QPG6200LDK-01, an IoT Development Kit that offers a complete solution for building multi-standard Matter™, Thread, Zigbee, and Bluetooth® Low Energy based on the QPG6200L.



This kit enables easy integration of **ConcurrentConnect** technology in your application:

- **Multi-channel** enables Zigbee + Matter concurrently
- **Antenna Diversity** doubles the effective range
- **Multi-radio** enables BLE scanning + Matter concurrently.

More information available on Qorvo's website.

Abbreviations

ACL	Asynchronous Connection Logical transport
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
ANIO	Analog Input/Output
AoD	Angle of Departure
API	Application Program(ming) Interface
ARIB	(Japan) Association of Radio Industries and Businesses
ASME	American Society of Mechanical Engineers
CCA	Clear Channel Assessment
CCM	Counter with CBC-MAC (ciphering)
CCM*	extension of CCM
CDM	(ESD) Charged Device Model
CSMA/CA	Carrier Sense Multiple Access with Collision Avoidance
DNL	Differential Nonlinearity
ECDH	Elliptic-Curve Diffie–Hellman
ECDSA	Elliptic-Curve Digital Signature Algorithm
ECMQV	Elliptic-Curve MQV (Menezes–Qu–Vanstone)
EdDSA	Edwards-curve Digital Signature Algorithm
ESD	Electrostatic Discharge
ETSI	European Telecommunication Standardization Institute
EVM	Error Vector Magnitude
FCC	(US) Federal Communications Commission
FEM	Front-End module
GATT	Generic Attribute Protocol
GND	Ground
GPIO	General Purpose Input / Output
HAL	Hardware Abstraction Layer
HBM	(ESD) Human Body Model
HCI	Host Controller Interface
HID	Human Interface Device
(e)HPS	(enhanced) High Performance State
HPSret	High Performance State digital retained
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Nonlinearity
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IIP3	Third Order Input Intercept Point
IO	Input/Output
IR	InfraRed
ISM	Industrial, Scientific, and Medical (license-free frequency band)
LDO	Low Drop-Out voltage regulator
LE	(Bluetooth) Low Energy
LED	Light Emitting Diode
LFSR	linear feedback shift register
LjRC	Low jitter Resistor–Capacitor (circuit)
LL	(Bluetooth) Link Layer
(e)LPS	(enhanced) Low Power State
LQI	Link Quality Indication
LSb	Least-Significant bit
MAC	Medium Access Control layer
MCU	Micro Controller Unit
MEMS	Micro-Electro-Mechanical Systems
MOQ	Minimum Order Quantity
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MSb	Most-Significant bit
OTA	Over the Air
OTP	One-Time Programmable Memory
PCB	Printed Circuit Board
PDM	Pulse-Density Modulation
PER	Packet Error Rate
PHY	Physical layer
PMU	Power Management Unit
POR	Power On Reset
PSRR	Power Supply Rejection Ratio
PUF	Physical Unclonable Function
PWM	Pulse-Width Modulation
QFN	Quad Flat No leads (package)
RAM	Random-Access Memory
RC	resistor–capacitor (circuit)
RF	Radio Frequency
RSSI	Received Signal Strength Indication
RoHS	Restriction of Hazardous Substances (Directive)
ROM	Read-Only Memory
RX	Receive
SHA	Secure Hash Algorithm
SIDO	Single-Inductor Dual-Output
SPI	Serial Peripheral Interface
TX	Transmit
UART	Universal Asynchronous Receiver and Transmitter
VDD	Voltage-Drain-Drain (i.e. positive voltage supply)
VMT	Voltage Minimum Threshold

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Product Status

Marking	Product Status	Definition
ADVANCE INFO	Formative / In Design	Datasheet contains design specifications for product development. Specifications may change in any manner without notice.
► PRELIMINARY	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Qorvo reserves the right to make changes at any time without notice to improve the design.
(none)	Full Production	Datasheet contains final specifications. Qorvo reserves the right to make changes at any time without notice to improve the design.
OBSOLETE	Not in Production	Datasheet contains specifications on a product that is discontinued. The datasheet is for reference information only.

Document History

Version	Date	Section	Changes
0.1	22 Sep 2023	all	Released version.
0.2	9 May 2024	Table 38	High-sink IR for GPIO4 removed.
		12	Micbias signal changed to LPbias.
0.3	17 May 2024	2	Block diagram updated.
		7.3	ANIO / ADC section updated.
		11	Parameter Evaluation Circuit diagrams updated.
		11.3-11.5	Data updated.
		12.1.2	Package drawings and land patterns updated.
		Figure 6	Power modes diagram updated.
		Table 38	GPIO mapping table updated (IR).
0.4	28 May 2024	7.2	5V tolerance text added.
			GPIO mapping tables updated.
		3	Timers added in Key Features.
0.5	24 Jul 2024	11.3	TBD's removed in max. and max. columns in current consumption tables.
		11	Parameter evaluation circuit diagrams for QFN32 updated to Rev 0.6.
		6.2.2	RF4CE functionality added.
		11.13	DCDC Efficiency graph added.
		Table 37 and Table 38	GPIO mapping tables updated.
		all	Minor format and textual updates.
0.6	27 Sep 2024	all	1st draft for QPG6200L. From this version the general QPG6200 DS converges to the QPG6200L DS version.
		all	AoA/AoD text removed.
		2	Block diagram updated.
		3, 7.3, 11.11	ANIO / ADC sections updated.
		5	Contact information updated.
		7.2	5V Tolerance text removed.
		8.9	Application Programming Information updated.
		10	Support for DPA counter measures removed.
		11.5	EVM filtering details updated.
		11.7	Table for Reset, Wake up and Sleep Timing Characteristics renewed.
		11.9.1	32 MHz Crystal Oscillator text updated.
		11.9.2	32 KiHz Crystal Oscillator text updated.
		13	Development Kit text updated.
		all	Minor text and format updates.