APPLICATION NOTE

QPQ5501

Wi-Fi U-NII 2c-4 band Boost BAW Filter

Product Overview

The purpose of this application note is to help customers translate the layout and design guidelines for the Qorvo® QPQ5501 Bulk Acoustic Wave (BAW) band-pass filter.

The Qorvo® QPQ5501 is a high-performance, high power, Bulk Acoustic Wave (BAW) band-pass filter with extremely steep roll-offs, simultaneously exhibiting low loss in the Wi-Fi UNII 2c - 4 band and high near-in rejection in the UNII 1 – 2a and UNII 5 – 8 bands.

The filter module is specifically designed to enable industry's leading capacity performance in Wi-Fi applications that result in higher power capacity in more Wi-Fi channels.

This application note serves the purpose of component integration while using advanced laminate module packaging techniques to achieve high integration in an industry leading compact footprint. And at the same time negating as many external passive component placements to assist end users ease of integration into their circuits.

Product Details

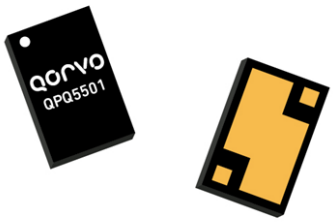


Figure 1a. Device Packaging Detail

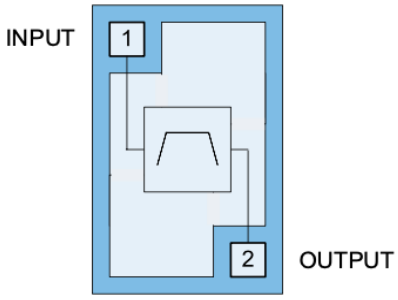


Figure 1b. Functional Block Diagram & Pin-Out Detail

Table 1. QPQ5501 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	RF_In	RF input. Internally matched to 50Ω and internally DC blocked.
3	RF_Out	RF output. Internally matched to 50Ω and internally DC blocked
2	GND	RF Ground connection. Use recommended via pattern to minimize inductance and thermal resistance.

Notes:

1. Pin 1 is the unidirectional large signal input port and pin 3 is the unidirectional large signal output port.
2. The Transmit (Pin 1) and Antenna (Pin 3) ports are both bidirectional for small signals only.
3. It's recommended not to exceed the max power handling conditions specified on the data sheet or permanent damage may occur.

Evaluation Board Information

The Qorvo® QPQ5501 evaluation board is designed to provide performance representative of that obtainable in an actual application. The evaluation board is designed to operate with 50Ω load impedances at all RF ports, which are provided with SMA connector interfaces.

Figure 2a. QPQ5501 Evaluation Board PCB

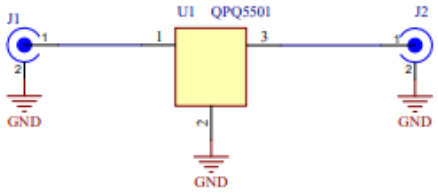


Figure 2b. QPQ5501 Evaluation Board Schematic

Table 2. QPQ5501 PCB Stack-Up

LAYER	NAME	MATERIAL	THICKNESS	DIELECTRIC CONSTANT
	Top Overlay	-	-	-
	Top Solder	Solder Resist	0.0008in	
1	Top Layer	Copper	0.0007in	-
	Dielectric 1	Rogers 4350B	0.0066in	3.68
2	Layer 2/ Metal 2	Copper	0.0007in	-
	Dielectric 2	FR4	0.045in	4.1
3	Layer 3/ Metal 3	Copper	0.0007in	-
	Dielectric 3	FR4	0.006in	4.8
4	Bottom Layer/ Metal 4	Copper	0.0007in	-
	Bottom Solder	Solder Resist	0.0008in	3.5
	Bottom Overlay	-	-	-

Note:

Total PCB Thickness: 0.062in

Table 3. QPQ5501 Evaluation Board Bill of Materials

REF. DES.	VALUE	DESCRIPTION	MANUF.	PART NUMBER
-	-	Printed Circuit Board		
U1	-	5GHz bandBoost U-NII 2c-4 Filter	Qorvo	QPQ5501

System Architecture Application Circuit Recommendations

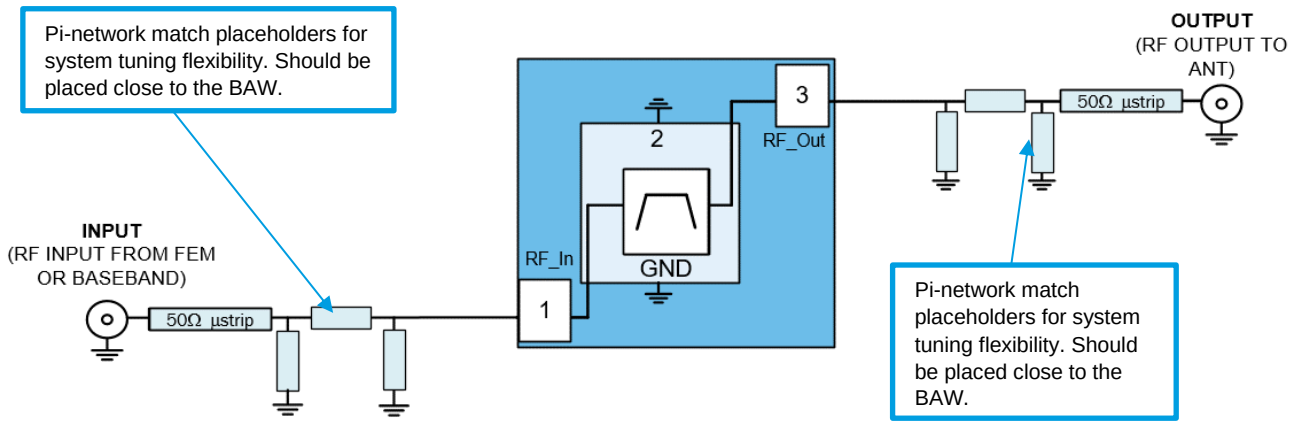


Figure 3. Recommended Application Circuit in a System

RF Matching Considerations

The above schematic shows Qorvo® recommended Pi-network match placeholders for system tuning flexibility based on the QPQ5501 evaluation board and should be placed close to the BAW.

- The customer should ensure that sufficient Pi-matching is provided based on their PCB layout.
- If additional out-of-band rejections/ attenuations are needed the matching at the output port will help to improve the filtering.
- Matching at the Input port side of the BAW will help in improving the in-band ripple and insertion loss.

PCB Layout Considerations

The board layout must be carefully considered to achieve optimal performance from any BAW filter, including the QPQ5501. In addition to providing connectivity between the BAW and external components, the PCB layout is a part of the overall circuit. The PCB parasitics of the RF traces, along with coupling between traces, must be evaluated. The QPQ5501 evaluation board PCB layout guidelines provide a good starting point for designing the layout in the actual application.

RF and DC Trace Routing

All PCB traces between the RF pins and matching networks (where applicable) should be 50Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. RF traces should be isolated from other RF and DC signals from other components by adding solid ground planes (with vias) between them to minimize coupling or cross-talking. All DC traces routed near the BAW must be isolated from the BAW with a GND in between the BAW and the DC trace. Qorvo® recommends to avoid routing traces/ tracks underneath the BAW.

In addition, Qorvo® also recommends reducing RF trace lengths, wherever possible. Fenced or shielding vias are recommended around RF traces to help maintain a low impedance or short return current path.

Grounding Considerations

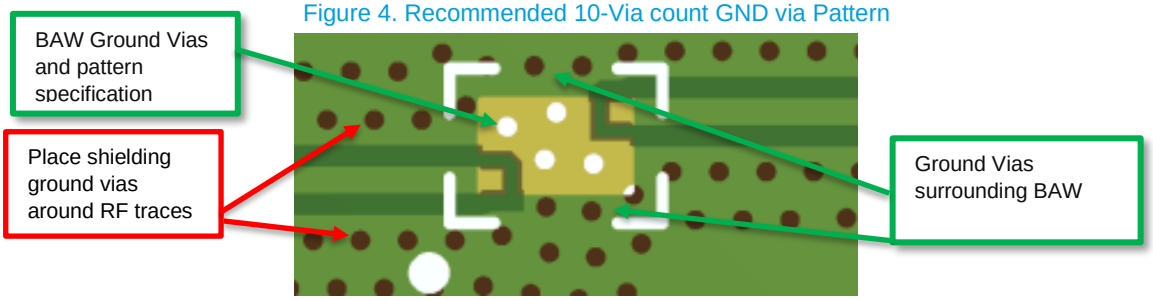
Grounding of BAW GND pad – The ground pad serve as the primary RF ground reference for the entire BAW. Connect the BAW filter ground pad directly to the main ground plane layer of the PCB. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible to reduce inductance. Although the QPQ5501 Evaluation Board uses Blind vias routed from the top layer through to the 2nd layer ground underneath the BAW, this type of via is not mandatory. They can be routed from the top layer to the bottom layer GND without any performance changes to the BAW and is the preferred method.

Reference Plane Ground – Qorvo® recommends distributing a large number of via holes over the entire area below/around the BAW to provide good RF ground reference ground plane, as shown in the thermal via array pattern in **Figure 4** below. The GND planes on the rest of the PCB should have vias on them which route from the top layer through to the bottom GND layer.

GND Vias for Thermal Considerations – The BAW GND pins serve as the primary path for heat removal, additionally, the PCB ground vias will serve as a low resistance thermal path between the BAW and the PCB. Vias passing through multiple copper layers provide the best overall RF and thermal performance. The QPQ5501 ground pad has special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduction path for heat dissipation. The GND pad, vias pattern, size, and type used on the Qorvo® evaluation board should be replicated on the final product. The Qorvo® layout files in Gerber format can be provided to the reader upon request.

- The QPQ5501 evaluation board uses GND vias with an 5mil hole size and 10mil diameter along RF traces.
- Qorvo recommends using GND vias between 3.8 and 8mil hole size and to follow the thermal via array patterns similar to what's shown in **Figure 4.**
- Qorvo® recommends using a **Direct Connect** ground connection underneath the QPQ5501 rather than use the Thermal Relief style ground connection.
- The Qorvo® QPQ5501 Evaluation Board uses Filled Vias on the GND pad.

Figure 4. Recommended 10-Via count GND via Pattern

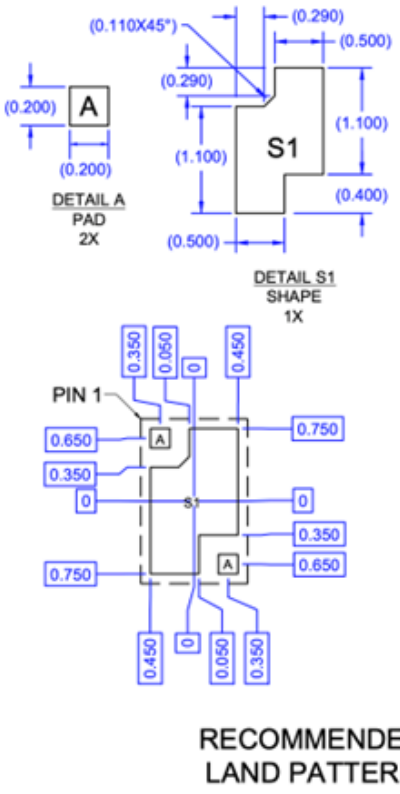


Land Pattern Recommendation

PCB Footprint Recommendations

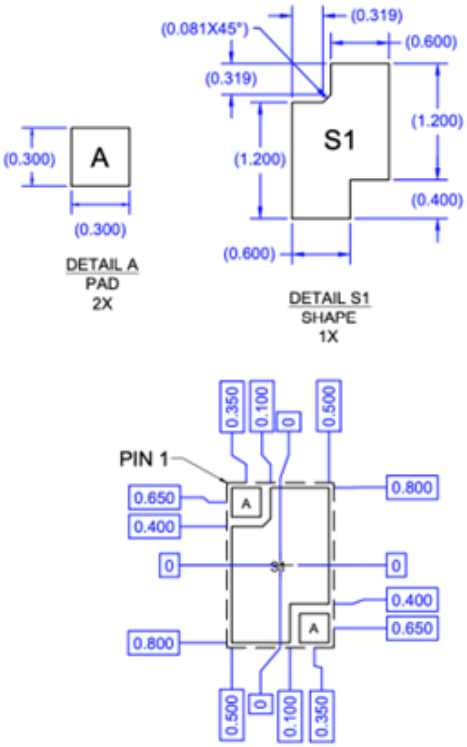
See **Figures 5a and 5b** below for the Qorvo® recommended package outline drawing and solder mask patterns.

Land Pattern Recommendation



RECOMMENDED
LAND PATTERN

Figure 5a. PCB Footprint Recommended Landing Pattern



RECOMMENDED
LAND PATTERN MASK

Figure 5b. PCB Footprint Recommended Solder Mask Pattern

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Qorvo® recommends to use a 2mil e-FAB stencil.

Package Information

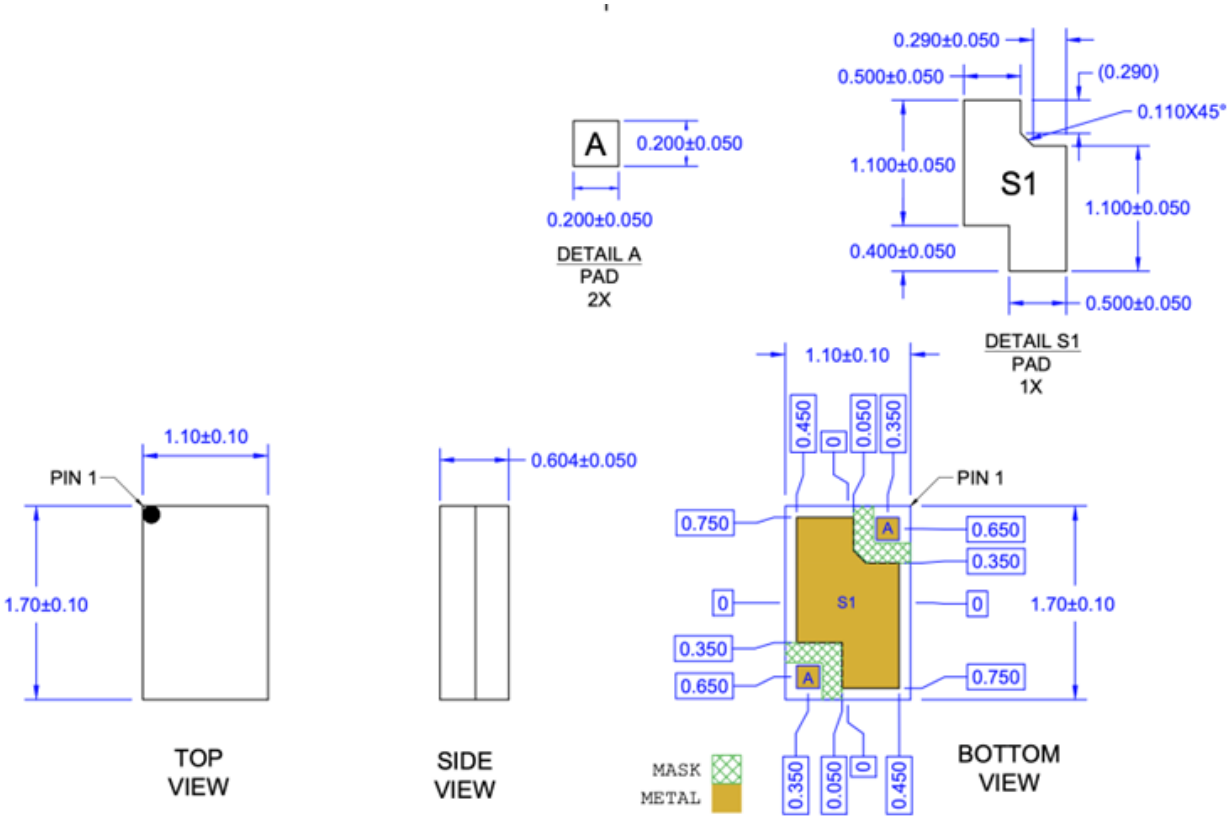


Figure 6a. Marking Diagram

Figure 6b. QPQ5501 Package Outline Drawing

Package Style: Laminate
Dimensions: 1.1 x 1.7 x 0.604 mm

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo® evaluation board for this product.
3. Some modifications may be necessary to suit end user assembly materials and processes.

Support Data

For any further data on the QPQ5501, please request Qorvo® point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo® for general guidelines.

Revision History

Revision	Create Date (mm/dd/yyyy)	Description of Change
A	10/14/2024	Initial Release

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
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