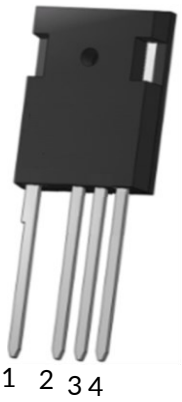
DATASHEET

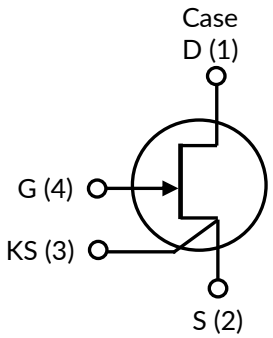
UJ4N075005K4S

750V-4.8mΩ SiC Normally-on JFET

Rev. B, June 2024

CASE





Part Number	Package	Marking
UJ4N075005K4S	TO-247-4L	UJ4N075005K4S

RoHS COMPLIANT | Pb LEAD FREE | HF HALOGEN FREE

Description

Qorvo's UJ4N075005K4S is a 750 V, 4.8mΩ high-performance Gen 4 normally-on SiC JFET transistor. This device exhibits ultra-low on resistance ($R_{DS(on)}$) in a TO-247-4L package, making it an ideal fit to address the challenging thermal constraints of solid-state circuit breakers and relay applications. Additionally, the JFET is a robust device technology capable of the high-energy switching required in circuit protection applications.

Features

- Single digit on-resistance
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- Short circuit rated
- RoHS compliant

Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-30 to +3	V
		AC [1]	-30 to +30	V
Continuous drain current [2]	I_D	T_C < 127°C	120	A
Pulsed drain current [3]	I_{DM}	T_C = 25°C	588	A
Short circuit withstand time	t_{SC}	V_{DS} = 400V, $T_{J(START)}$ = 175°C	5	µs
Power dissipation	P_{tot}	T_C = 25°C	714	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1. +30V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by bondwires
3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.16	0.21	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=-20V, I_D=2mA	750			V
Total drain leakage current	I_{DSS}	V_{DS}=750V, V_{GS}=-20V, T_J=25°C		13	120	µA
		V_{DS}=750V, V_{GS}=-20V, T_J=175°C		65		
Total gate leakage current	I_{GSS}	V_{GS}=-20V, T_J=25°C		0.1	100	µA
		V_{GS}=-20V, T_J=175°C		0.3		µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=2V, I_D=80A, T_J=25°C		4.8		mΩ
		V_{GS}=0V, I_D=80A, T_J=25°C		5.4	6.6	
		V_{GS}=2V, I_D=80A, T_J=175°C		10.4		
		V_{GS}=0V, I_D=80A, T_J=175°C		11.9		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=180mA	-8.3	-6.0	-3.7	V
Gate resistance	R_G	f=1MHz, open drain		0.8		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=400V, V_{GS}=-20V f=100kHz		3028		pF
Output capacitance	C_{oss}			364		
Reverse transfer capacitance	C_{rss}			360		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=-20V		448		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=-20V		36		µJ
Total gate charge	Q_G	V_{DS}=400V, I_D=80A, V_{GS} = -18V to 0V		400		nC
Gate-drain charge	Q_{GD}			270		
Gate-source charge	Q_{GS}			60		

Typical Performance Diagrams

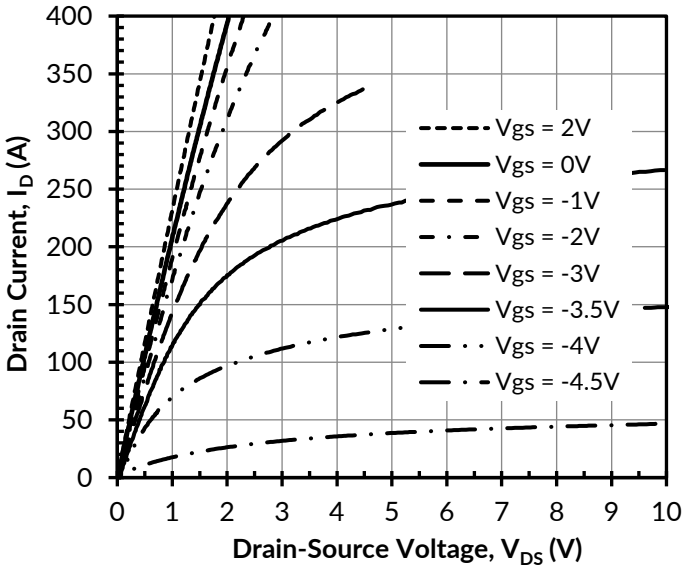


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

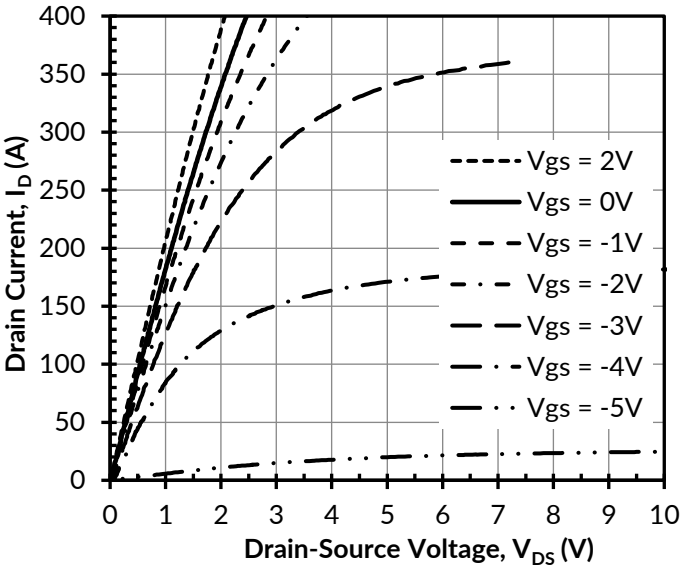


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

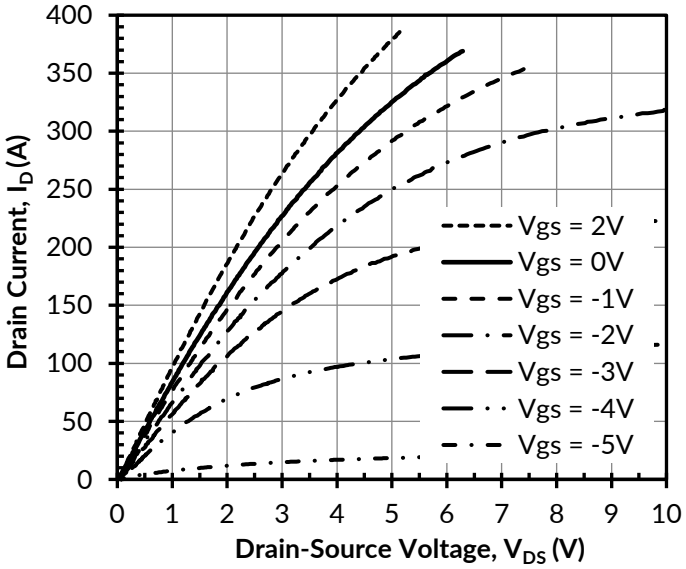


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

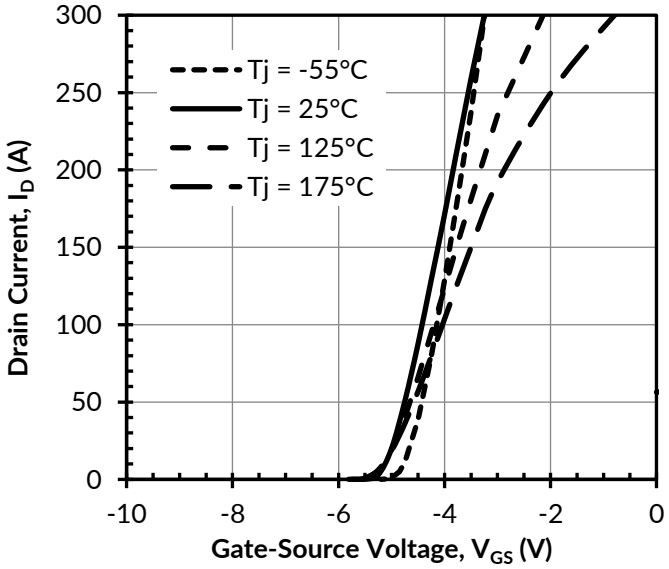


Figure 4. Typical transfer characteristics at V_{DS} = 5V

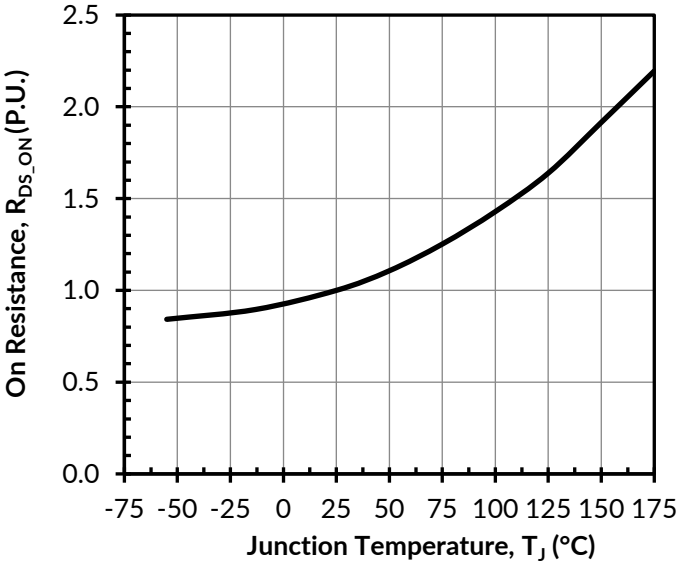


Figure 5. Normalized on-resistance vs. temperature at V_{GS} = 0V and I_D = 80A

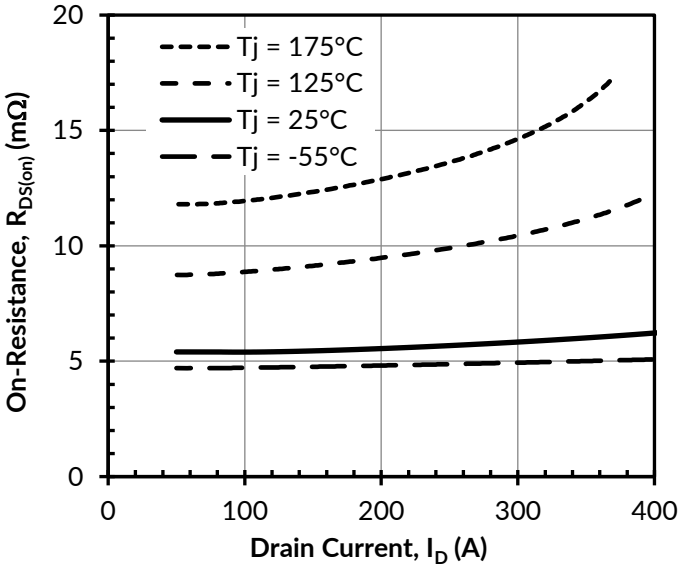


Figure 6. Typical drain-source on-resistances at V_{GS} = 0V

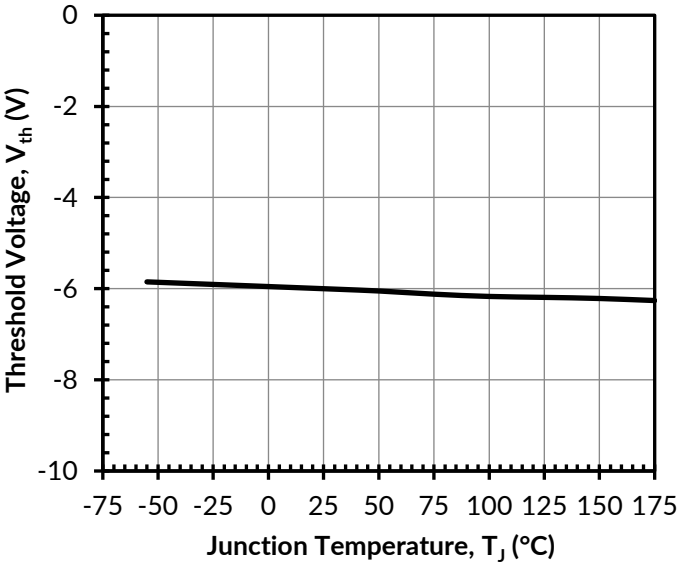


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 180mA

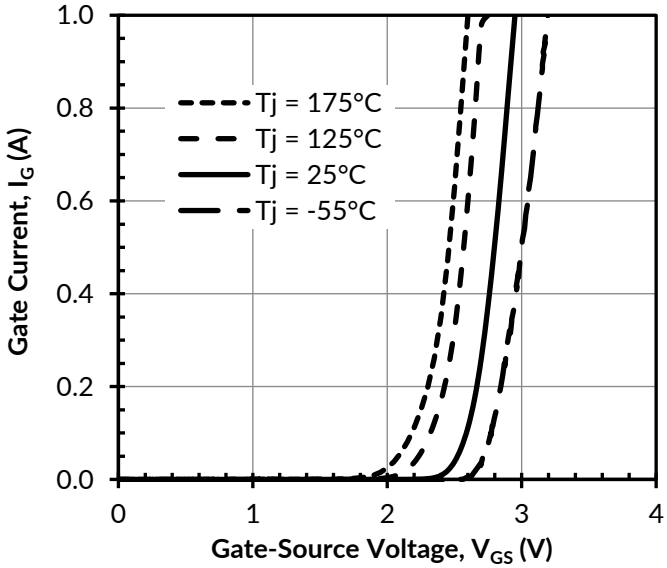


Figure 8. Typical gate forward current at V_{DS} = 0V

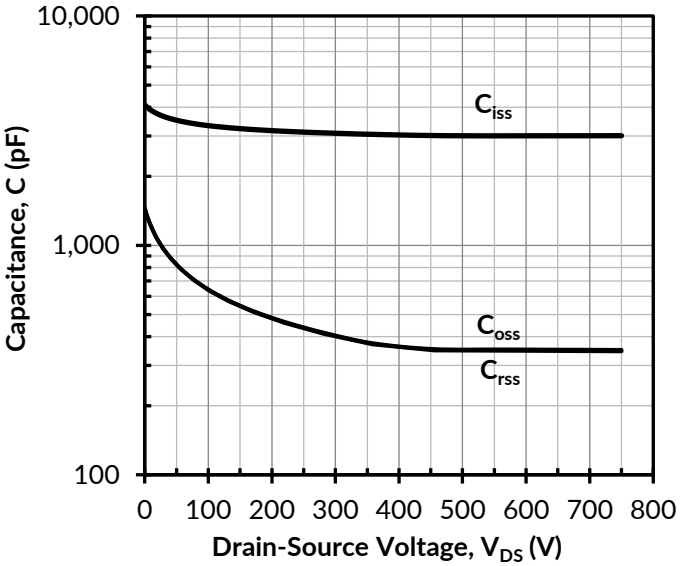


Figure 9. Typical capacitances at f = 100kHz and V_{GS} = -20V

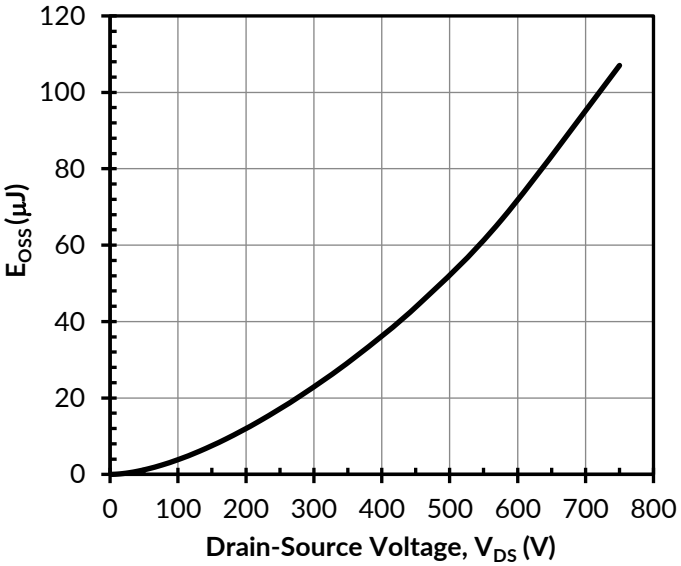


Figure 10. Typical stored energy in C_{OSS} at V_{GS} = -20V

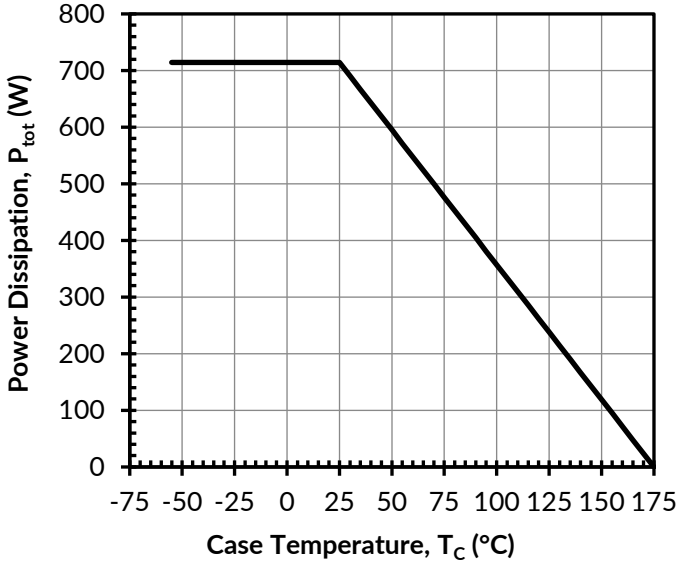


Figure 11. Total power Dissipation

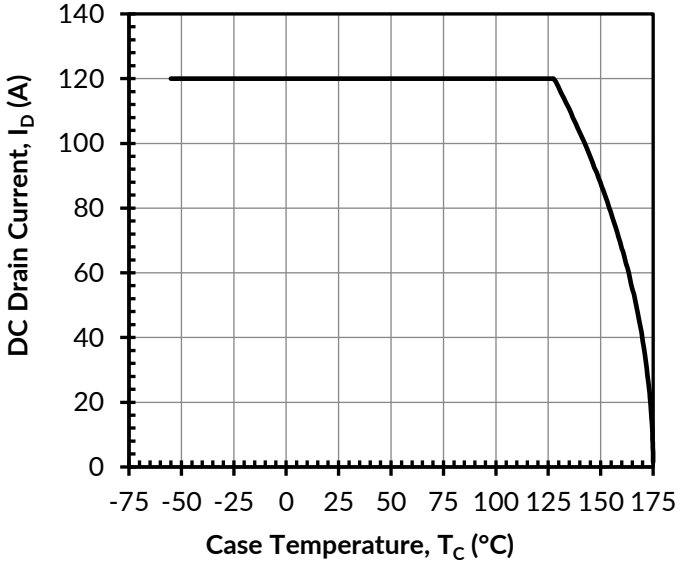


Figure 12. DC drain current derating

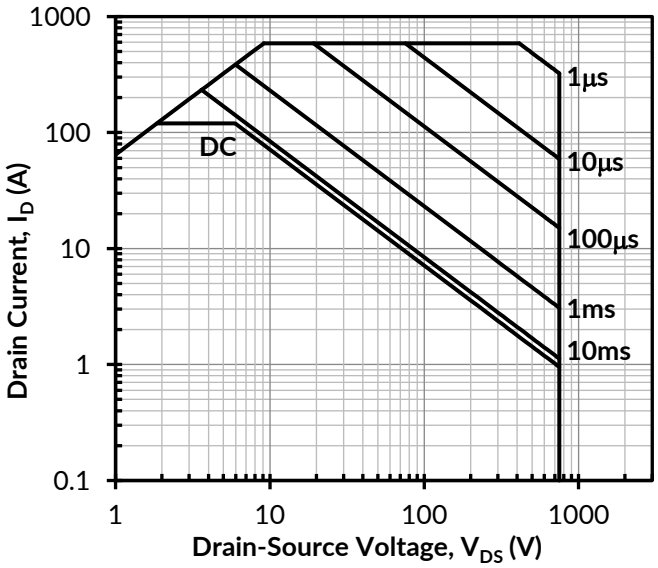


Figure 13. Safe operation area at T_C =25°C, Parameter t_p

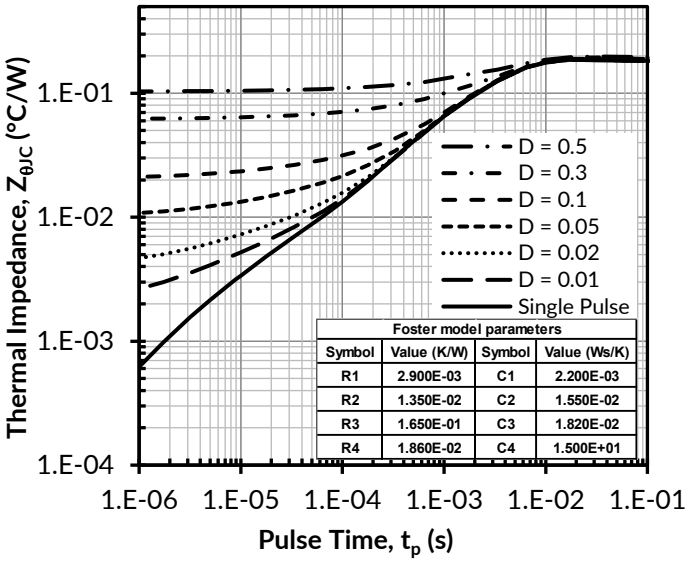


Figure 14. Maximum transient thermal impedance

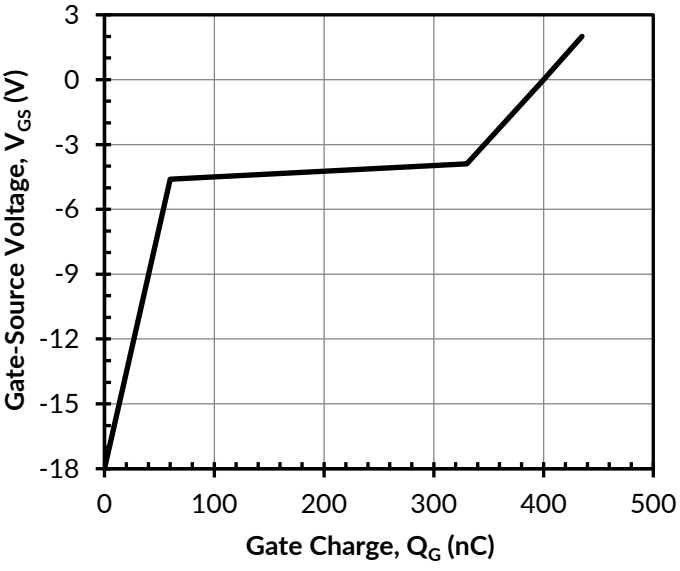


Figure 15. Typical gate charge at V_{DS} = 400V and I_D = 80A

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