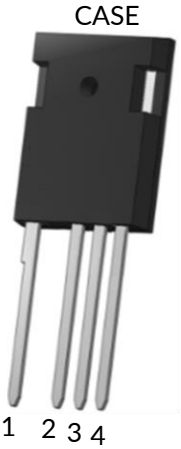
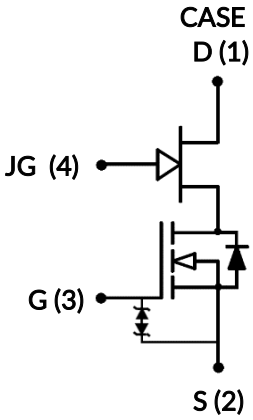
DATASHEET

# UG3SC120009K4S




| Part Number | Package | Marking |
|---|---|---|
| UG3SC120009K4S | TO-247-4L | UG3SC120009K4S |

RoHS COMPLIANT | Pb LEAD FREE | HF HALOGEN FREE

# 1200V-7.6mΩ Combo-FET

## (SiC JFET w/ Si MOSFET)

Rev. B, June 2024

## Description

Qorvo's UG3SC120009K4S "Combo-FET" integrates both a 1200V SiC JFET and a Low Voltage Si MOSFET into a single TO-247-4L package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

## Features

- Single digit $R_{DS(on)}$
- Normally-off capability
- Improved speed control
- Improved parallel device operation (3+ FETs)
- Operating temperature: 175C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- Short circuit rated

## Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High power switch mode converters (>25kW)

## Maximum Ratings

| Parameter | Symbol | Test Conditions | Value | Units |
|---|---|---|---|---|
| Drain-source voltage | $V_{DS}$ | | 1200 | V |
| JFET Gate (JG) to source voltage | $V_{JGS}$ | DC | -30 to +3 | V |
| | | AC [1] | -30 to +30 | V |
| MOSFET Gate (G) to source voltage | $V_{GS}$ | DC | -20 to +20 | V |
| | | AC (f > 1Hz) | -25 to +25 | V |
| Continuous drain current [2] | $I_D$ | $T_C$ < 112°C | 120 | A |
| Pulsed drain current [3] | $I_{DM}$ | $T_C$ = 25°C | 550 | A |
| Single pulsed avalanche energy [4] | $E_{AS}$ | L=15mH, $I_{AS}$ =8.6A | 555 | mJ |
| Power dissipation | $P_{tot}$ | $T_C$ = 25°C | 789 | W |
| Maximum junction temperature | $T_{J,max}$ | | 175 | °C |
| Operating and storage temperature | $T_J$,$T_{STG}$ | | -55 to 175 | °C |
| Max. lead temperature for soldering, 1/8" from case for 5 seconds | $T_L$ | | 250 | °C |

1. +30V AC rating applies for turn-on pulses <200ns applied with external $R_G$ > 1Ω.
2. Limited by bondwires
3. Pulse width $t_p$ limited by $T_{J,max}$
4. Starting $T_J$ = 25°C

## Thermal Characteristics

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Thermal resistance, junction-to-case | $R_{\theta JC}$ | | | 0.15 | 0.19 | °C/W |

## Electrical Characteristics ($T_J$ = +25°C and $V_{JGS}$ = 0V unless otherwise specified)

### Typical Performance - Static

| Parameter | Symbol | Test Conditions | | Value | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Drain-source breakdown voltage | $BV_{DS}$ | $I_D$=1mA, $V_{GS}$=0V | | 1200 | | | V |
| Total drain leakage current | $I_{DSS}$ | $V_{DS}$=1200V, $T_J$ = 25°C, $V_{GS}$=0V | | | 6 | 600 | µA |
| | | $V_{DS}$=1200V, $T_J$ = 175°C, $V_{GS}$=0V | | | 65 | | |
| Total JFET gate leakage current | $I_{JGSS}$ | $V_{JGS}$=-20V, $V_{GS}$=12V | | | 15 | 300 | µA |
| Total MOSFET gate leakage current | $I_{GSS}$ | $V_{GS}$=-20V / +20V | | | 5 | 20 | µA |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_{GS}$=12V, $I_D$=100A | $V_{JGS}$=2V, $T_J$=25°C | | 7.6 | | mΩ |
| | | | $T_J$=25°C | | 8.8 | 11 | |
| | | | $T_J$=125°C | | 13.7 | | |
| | | | $T_J$=175°C | | 18.5 | | |
| JFET gate threshold voltage | $V_{JG(th)}$ | $V_{DS}$=5V, $V_{GS}$=12V, $I_D$=320mA | | -9.3 | -7 | -4.7 | V |
| MOSFET gate threshold voltage | $V_{G(th)}$ | $V_{DS}$=5V, $V_{JGS}$=0V, $I_D$=10mA | | 4 | 4.7 | 6 | V |
| JFET gate resistance | $R_{JG}$ | f=1MHz, open drain | | | 0.54 | | Ω |
| MOSFET gate resistance | $R_G$ | f=1MHz, open drain | | | 3.5 | 6 | Ω |

### Typical Performance - Reverse Diode

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Diode continuous forward current [1] | $I_S$ | $T_C$ < 112°C | | | 120 | A |
| Diode pulse current [2] | $I_{S,pulse}$ | $T_C$ = 25°C | | | 550 | A |
| Forward voltage | $V_{FSD}$ | $V_{GS}$=0V, $I_S$=100A, $T_J$=25°C | | 1.65 | 2 | V |
| | | $V_{GS}$=0V, $I_S$=100A, $T_J$=175°C | | 2.4 | | |
| Reverse recovery charge | $Q_{rr}$ | $V_{DS}$=800V, $I_S$=100A, $V_{GS}$=$V_{JGS}$=0V, $R_{JG}$=0.7Ω di/dt=1200A/µs, $T_J$=25°C | | 785 | | nC |
| Reverse recovery time | $t_{rr}$ | | | 119 | | ns |
| Reverse recovery charge | $Q_{rr}$ | $V_{DS}$=800V, $I_S$=100A, $V_{GS}$=$V_{JGS}$=0V, $R_{JG}$=0.7Ω di/dt=1200A/µs, $T_J$=150°C | | 815 | | nC |
| Reverse recovery time | $t_{rr}$ | | | 124 | | ns |

## Typical Performance - Dynamic with MOSFET gate as control terminal and $V_{JGS}$=0V

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| MOSFET input capacitance | $C_{iss}$ | $V_{DS}$=800V, $V_{GS}$=0V, f=100kHz | | 8157 | | pF |
| Output capacitance | $C_{oss}$ | | | 351 | | |
| Reverse transfer capacitance | $C_{rss}$ | | | 2 | | |
| Effective output capacitance, energy related | $C_{oss(er)}$ | $V_{DS}$=0V to 800V, $V_{GS}$=0V | | 394 | | pF |
| Effective output capacitance, time related | $C_{oss(tr)}$ | | | 920 | | pF |
| $C_{OSS}$ stored energy | $E_{oss}$ | $V_{DS}$=800V, $V_{GS}$=0V | | 125 | | µJ |
| Total gate charge | $Q_G$ | $V_{DS}$=800V, $I_D$=100A, $V_{GS}$ = 0V to 15V | | 196 | | nC |
| Gate-drain charge | $Q_{GD}$ | | | 41 | | |
| Gate-source charge | $Q_{GS}$ | | | 41 | | |
| Turn-on delay time | $t_{d(on)}$ | Notes 5 and 6 $V_{DS}$=800V, $I_D$=100A, $V_{GS}$=0V to +15V, $R_{G\_ON}$=1Ω, $R_{G\_OFF}$=2Ω, $R_{JG\_ON}$=0.7Ω, $R_{JG\_OFF}$=3.3Ω, Inductive Load, FWD: same device with $V_{GS}$ = 0V, $V_{JGS}$=0V, $R_G$ =2Ω, $R_{JG}$=0.7Ω, $T_J$=25°C | | 160 | | ns |
| Rise time | $t_r$ | | | 73 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 210 | | |
| Fall time | $t_f$ | | | 59 | | |
| Turn-on energy | $E_{ON}$ | | | 11.5 | | mJ |
| Turn-off energy | $E_{OFF}$ | | | 2.5 | | |
| Total switching energy | $E_{TOTAL}$ | | | 14 | | |
| Turn-on delay time | $t_{d(on)}$ | Notes 5 and 6 $V_{DS}$=800V, $I_D$=100A, $V_{GS}$=0V to +15V, $R_{G\_ON}$=1Ω, $R_{G\_OFF}$=2Ω, $R_{JG\_ON}$=0.7Ω, $R_{JG\_OFF}$=3.3Ω, Inductive Load, FWD: same device with $V_{GS}$ = 0V, $R_G$ =2Ω, $V_{JGS}$=0V, $R_{JG}$=0.7Ω, $T_J$=150°C | | 158 | | ns |
| Rise time | $t_r$ | | | 79 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 53 | | |
| Fall time | $t_f$ | | | 212 | | |
| Turn-on energy | $E_{ON}$ | | | 12.3 | | mJ |
| Turn-off energy | $E_{OFF}$ | | | 2.8 | | |
| Total switching energy | $E_{TOTAL}$ | | | 15.1 | | |

5. Measured with the half-bridge mode switching test circuit in Figure 23.

6. Driven with the ClampDRIVE method as descriped in the section "Recommended Gate Drive Approach: ClampDRIVE method".

## Typical Performance - Dynamic with JFET gate as control terminal and $V_{GS}$=+12V

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| JFET input capacitance | $C_{Jiss}$ | $V_{DS}$=800V, $V_{JGS}$=-20V, f=100kHz | | 8110 | | pF |
| JFET output capacitance | $C_{Joss}$ | | | 368 | | |
| JFET reverse transfer capacitance | $C_{Jrss}$ | | | 358 | | |
| JFET total gate charge | $Q_{JG}$ | $V_{DS}$=800V, $I_D$=100A, $V_{JGS}$ = -18V to 0V | | 830 | | nC |
| JFET gate-drain charge | $Q_{JGD}$ | | | 520 | | |
| JFET gate-source charge | $Q_{JGS}$ | | | 120 | | |

## Typical Performance Diagrams - MOSFET gate as control terminal and $V_{JGS}$=0V

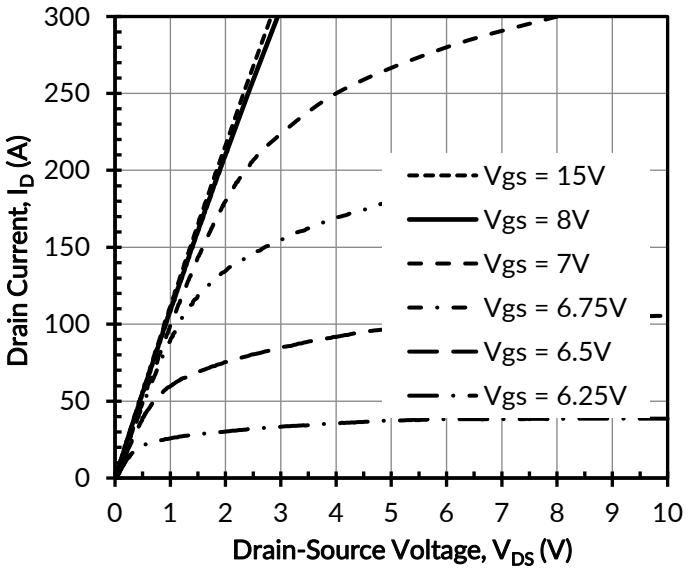



Figure 1. Typical output characteristics at $T_J$ = - 55°C, $t_p$ < 250µs

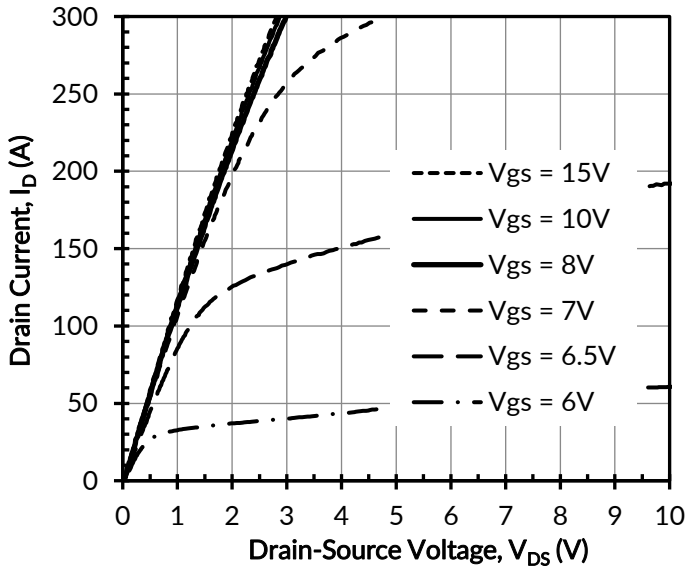



Figure 2. Typical output characteristics at $T_J$ = 25°C, $t_p$ < 250µs

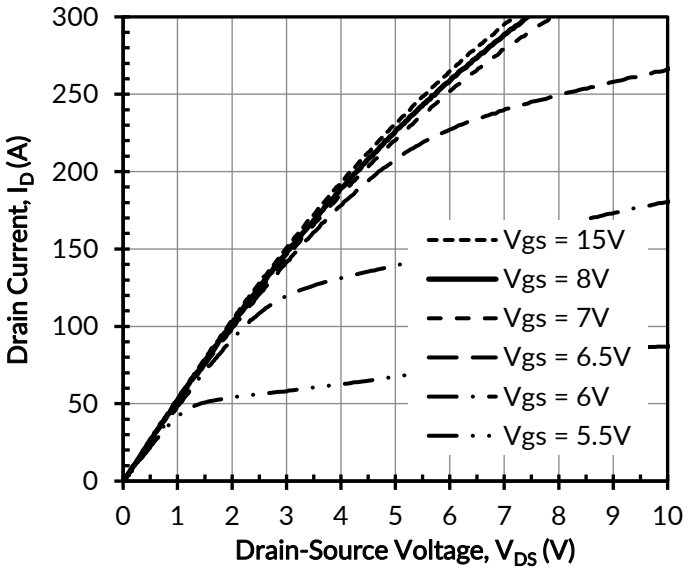



Figure 3. Typical output characteristics at $T_J$ = 175°C, $t_p$ < 250µs

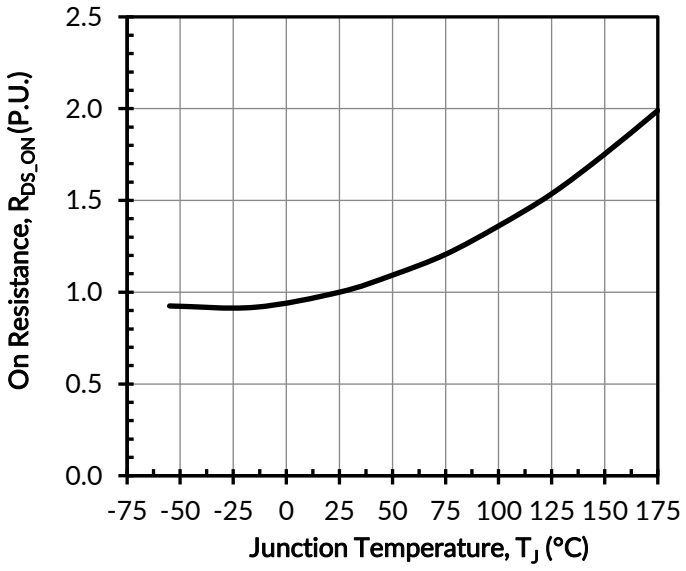



Figure 4. Normalized on-resistance vs. temperature at $V_{GS}$ = 12V and $I_D$ = 100A

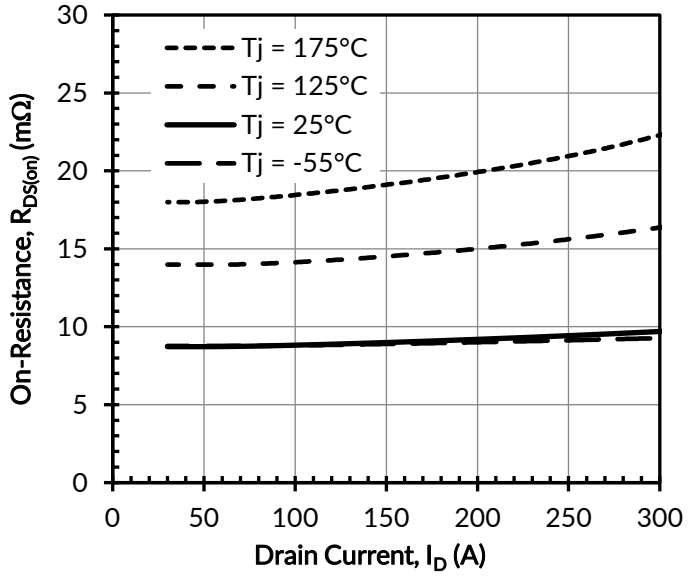



Figure 5. Typical drain-source on-resistances at $V_{GS}$ = 12V

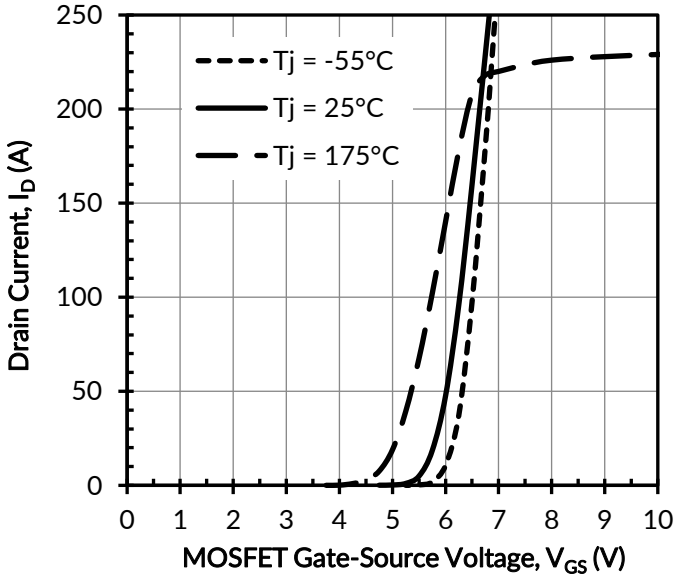



Figure 6. Typical transfer characteristics at $V_{DS}$ = 5V

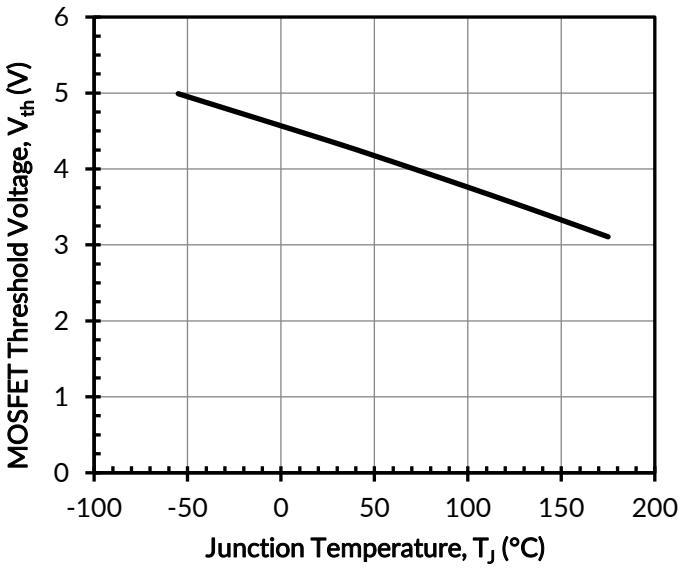



Figure 7. MOSFET threshold voltage vs. junction temperature at $V_{DS}$ = 5V and $I_D$ = 10mA

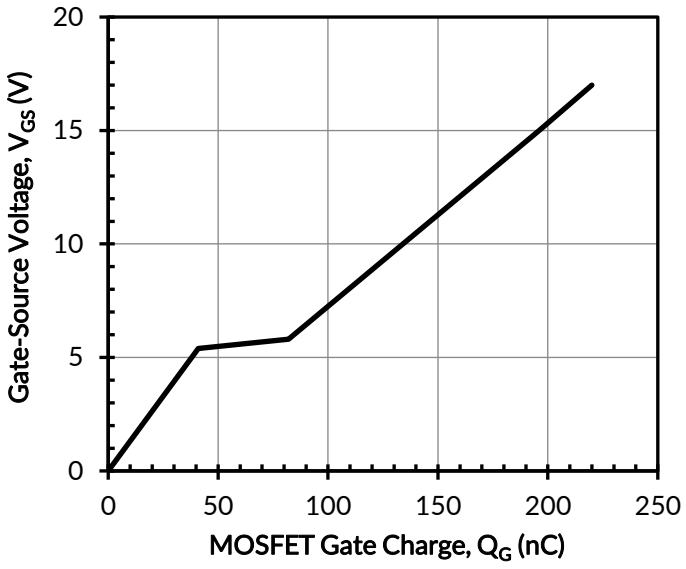



Figure 8. Typical MOSFET gate charge at $V_{DS}$ = 800V and $I_D$ = 100A

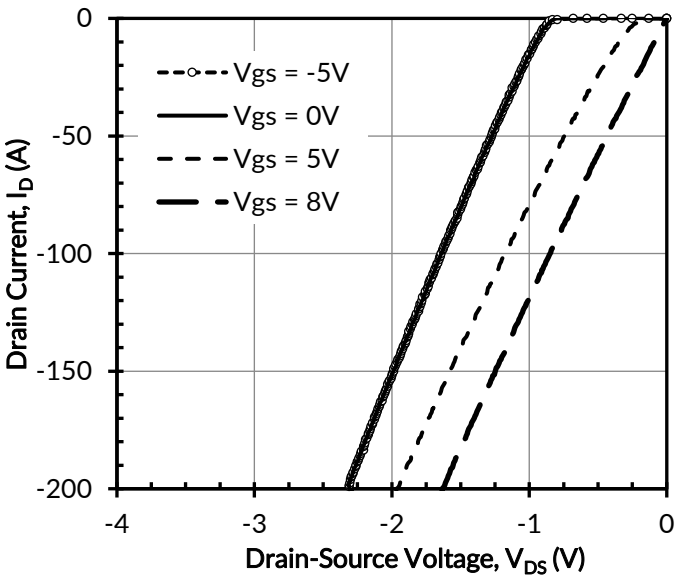



Figure 9. 3rd quadrant characteristics at $T_J$ = -55°C

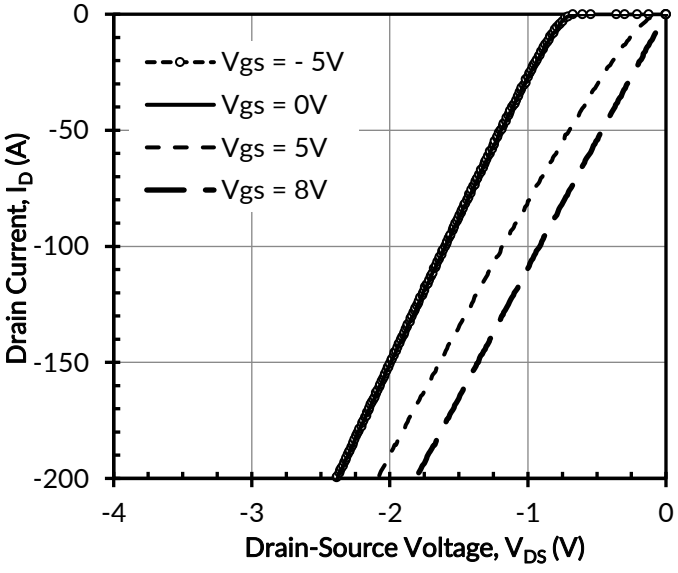



Figure 10. 3rd quadrant characteristics at $T_J$ = 25°C

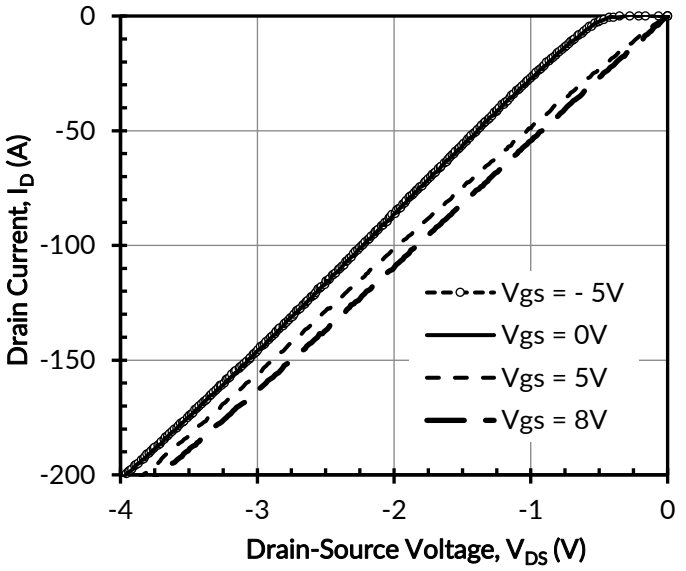



Figure 11. 3rd quadrant characteristics at $T_J$ = 175°C

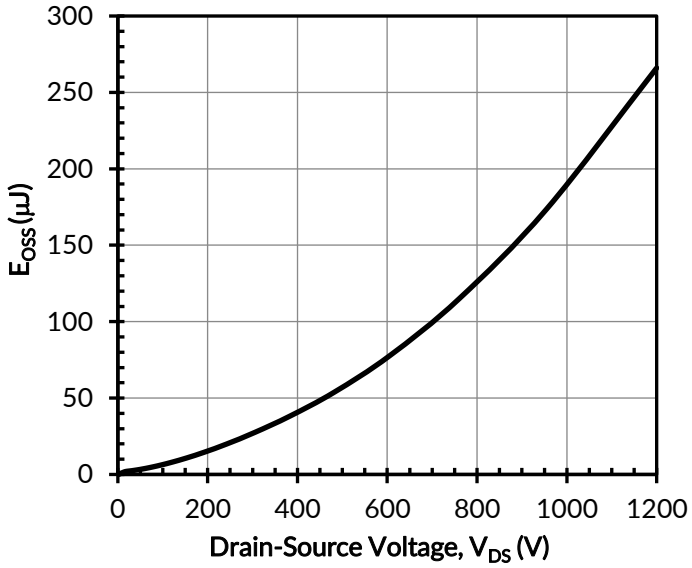



Figure 12. Typical stored energy in $C_{OSS}$ at $V_{GS}$ = 0V

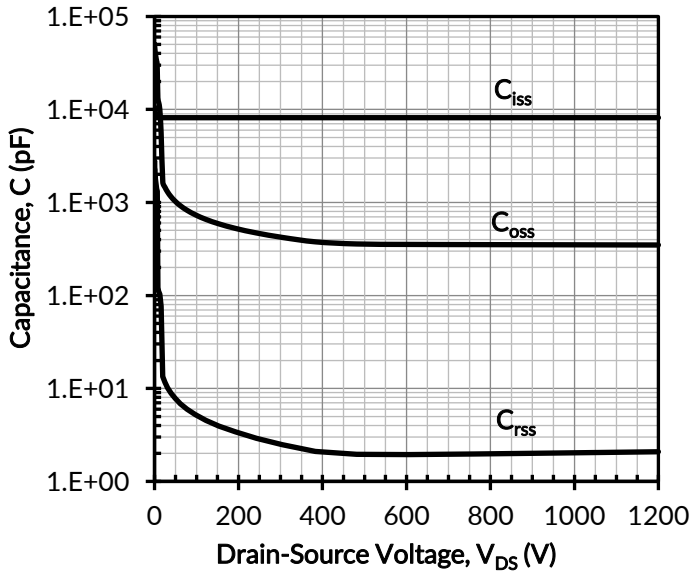



Figure 13. Typical capacitances at f = 100kHz and $V_{GS}$ = 0V

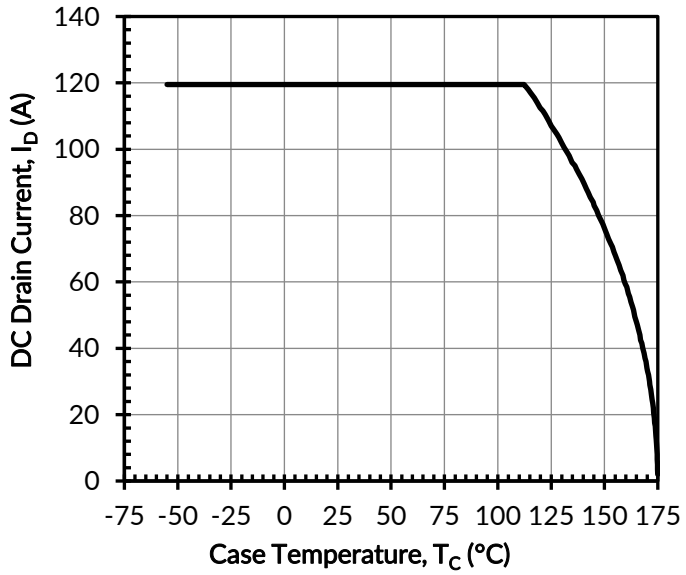



Figure 14. DC drain current derating

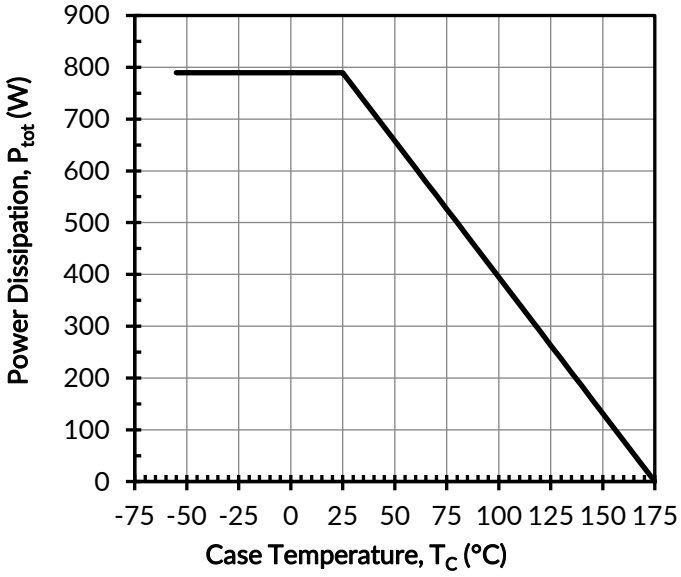



Figure 15. Total power dissipation

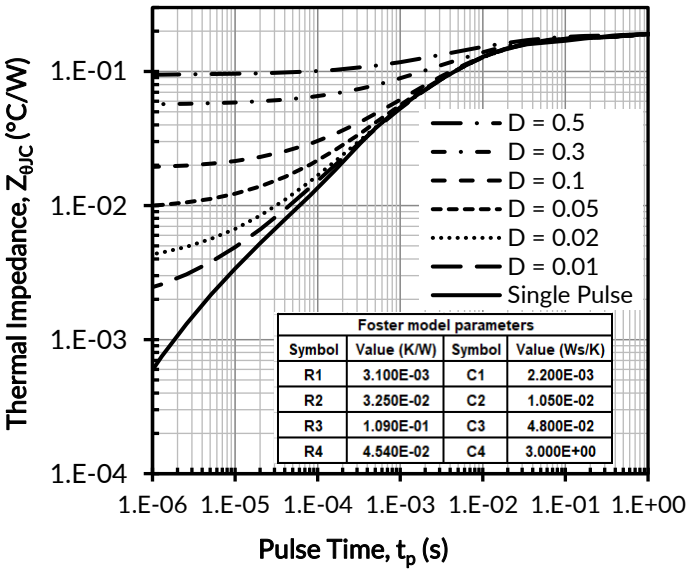



Figure 16. Maximum transient thermal impedance

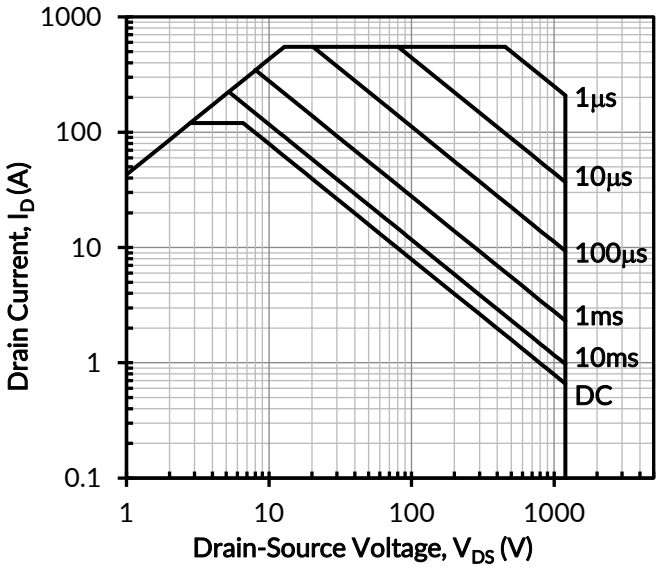



Figure 17. Safe operation area at $T_C$ = 25°C, D = 0, Parameter $t_p$

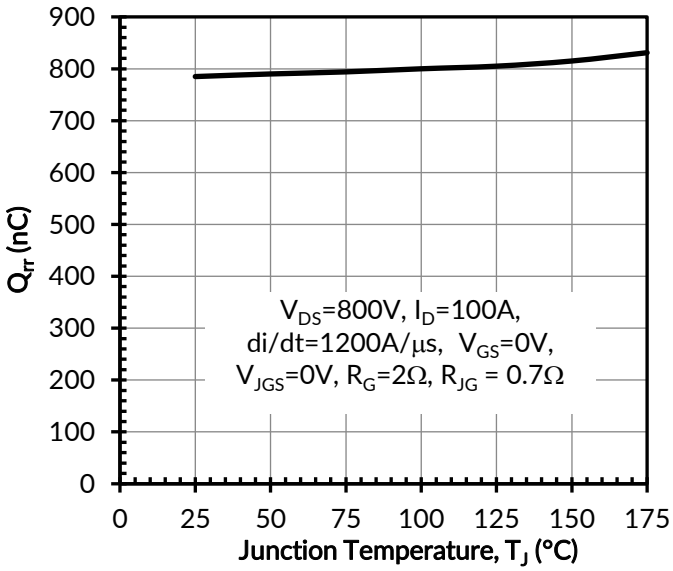



Figure 18. Reverse recovery charge $Q_{rr}$ vs. junction temperature

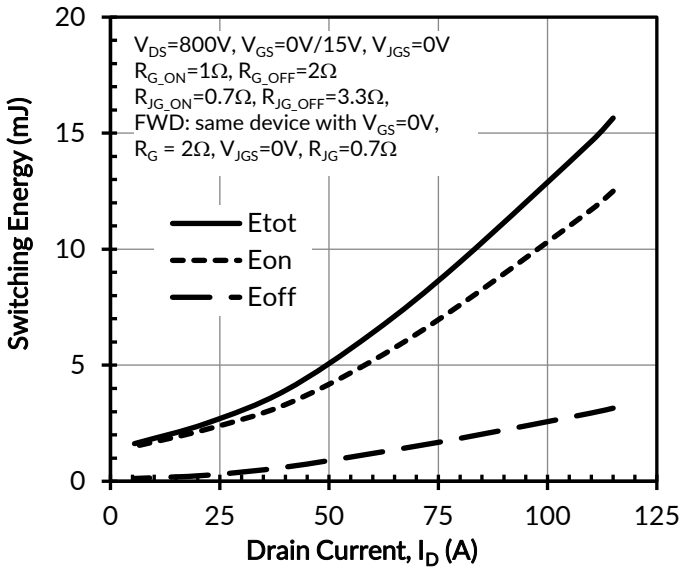



Figure 19. Clamped inductive switching energy vs. drain current at $T_J$ = 25°C

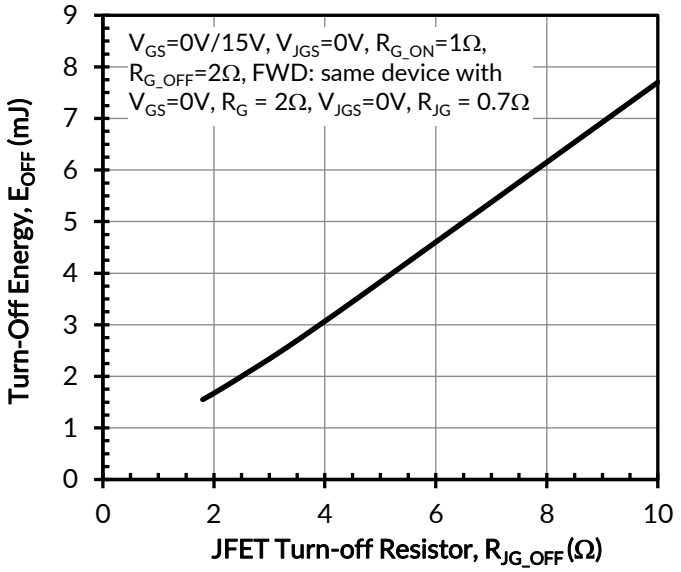



Figure 20. Clamped inductive switching turn-off energy vs. JFET gate resistor $R_{JG\_OFF}$ at $V_{DS}$ = 800V, $I_D$ = 100A, and $T_J$ = 25°C

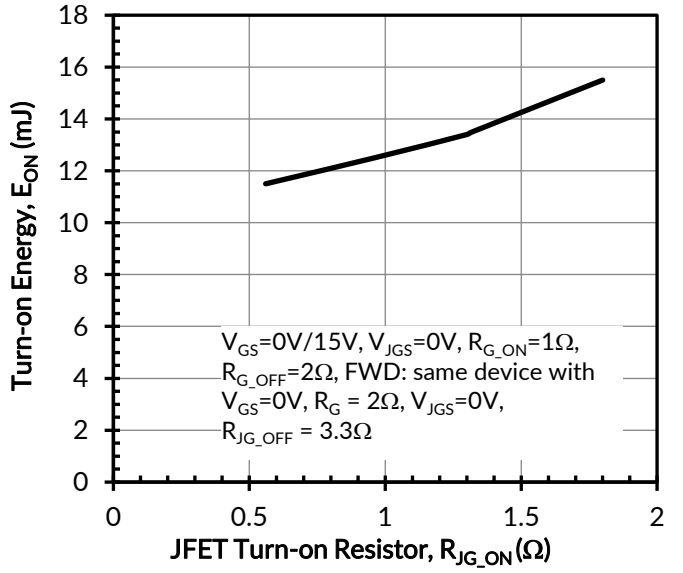



Figure 21. Clamped inductive switching turn-on energy vs. JFET gate resistor $R_{JG\_ON}$ at $V_{DS}$ = 800V, $I_D$ = 100A, and $T_J$ = 25°C

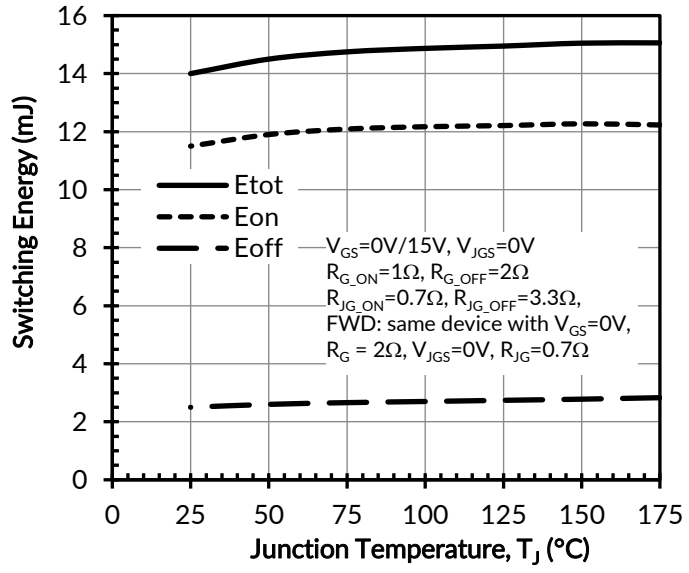



Figure 22. Clamped inductive switching energy vs. junction temperature at $V_{DS}$ = 800V and $I_D$ = 100A

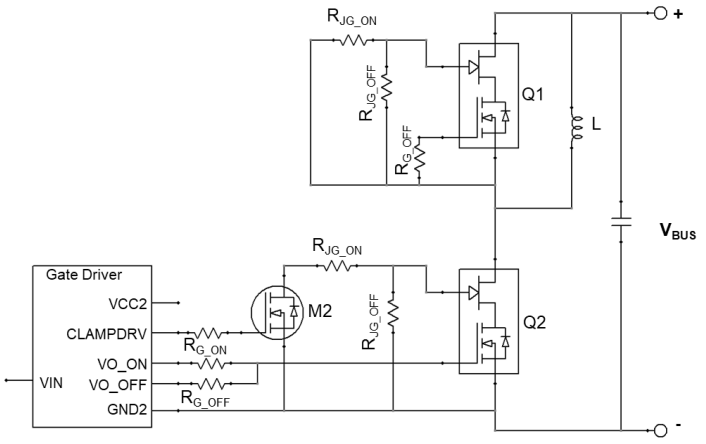



Figure 23. Schematic of the half-bridge mode switching test circuit with ClampDRIVE method.

## Typical Performance Diagrams - JFET gate as control terminal and $V_{GS}$=+12V

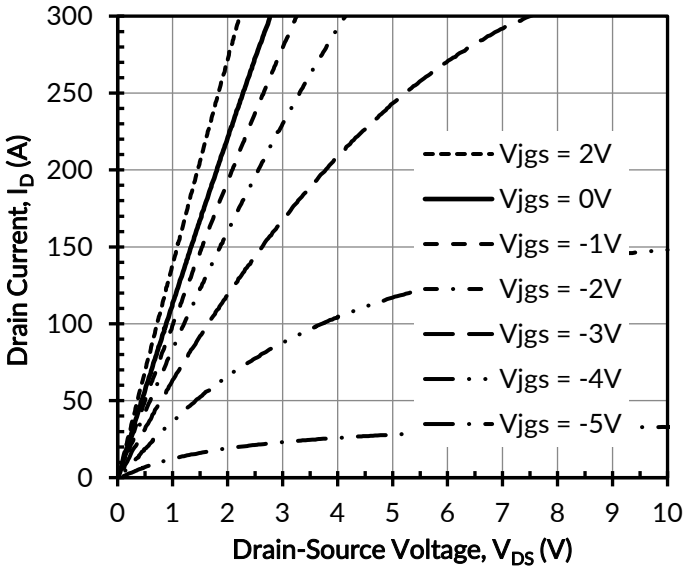



Figure 24. Typical output characteristics with JFET gate as control at $T_J$ = - 55°C, $t_p$ < 250µs

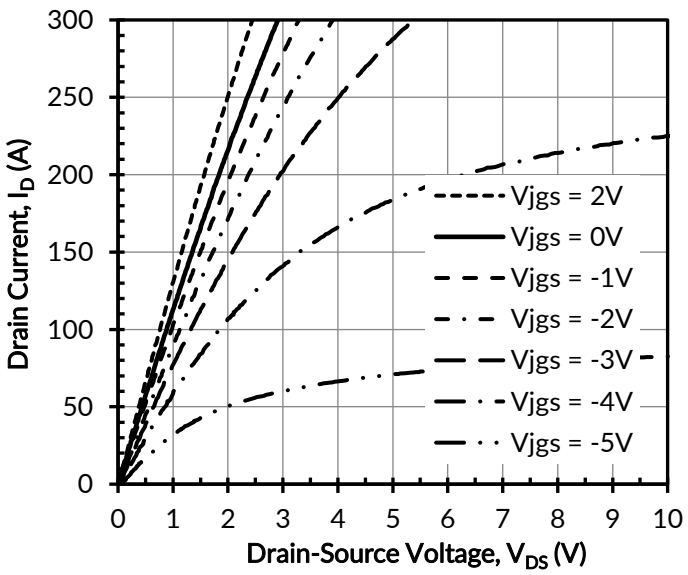



Figure 25. Typical output characteristics with JFET gate as control at $T_J$ = 25°C, $t_p$ < 250µs

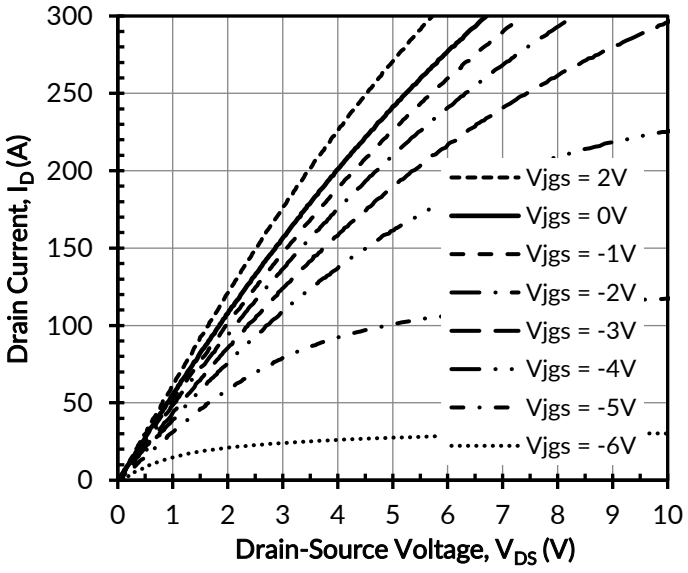



Figure 26. Typical output characteristics with JFET gate as control at $T_J$ = 175°C, $t_p$ < 250µs

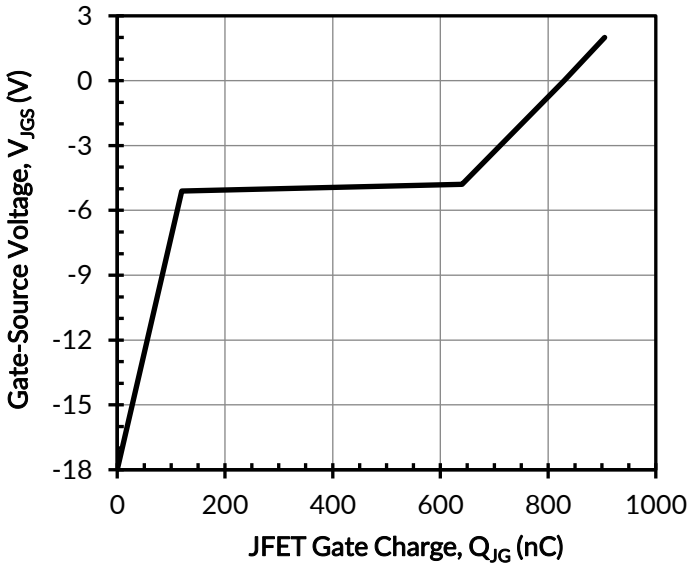



Figure 27. Typical JFET gate charge at $V_{DS}$ = 800V and $I_D$ = 100A

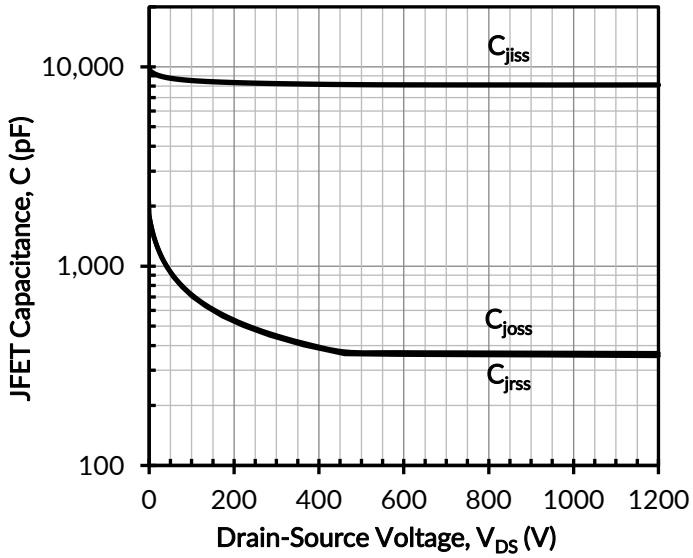



Figure 28. Typical JFET capacitances at f = 100kHz and $V_{JGS}$ = -20V

## Recommended Gate Drive Approach: ClampDRIVE method

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behaviors of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring fast switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value $R_{JG}$ such that, in the off-state, $R_{JG}$ is small enough not to cause a reverse recovery issue, and during turn-off transient, $R_{JG}$ is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure A. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is $R_{JG\_OFF}$. During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is $R_{JG\_OFF}$ during the turn-off process, and $R_{GJ\_OFF}$ can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of $R_{JG\_OFF}$ and $R_{JG\_ON}$. $R_{JG\_ON}$ can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and $R_{JG\_ON}$ into the JFET gate, so, the turn-on process is also determined by $R_{JG\_ON}$.

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors $R_{JG\_ON}$ and $R_{JG\_OFF}$

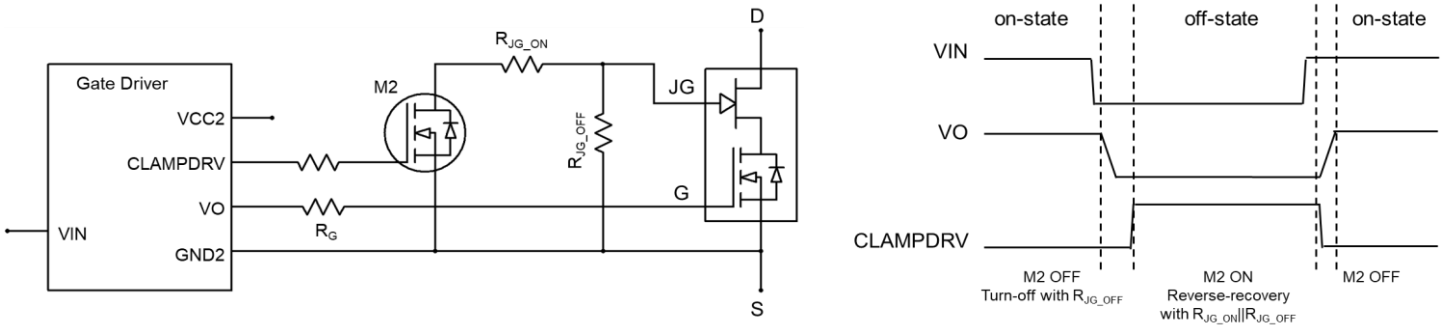



Figure A. Circuit schematic and timing diagram of the ClampDRIVE method

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