QPA1314

13.75 – 14.5 GHz 40 Watt GaN Power Amplifier

Product Overview

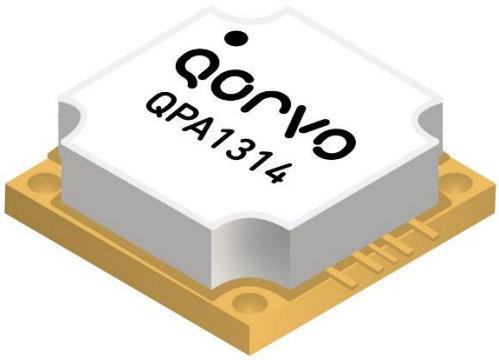
Qorvo's QPA1314 is a packaged high power MMIC amplifier, fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). QPA1314 is targeted for 13.75 – 14.5 GHz Satcom band. Linear power is 20 W with 25 dBc third order intermodulation distortion products. It provides 40 W of output power with 27 dB of large signal gain while achieving 30% power-added efficiency. Operating frequency can extend to 12.75 – 15.35 GHz if desired.

The QPA1314 is packaged in a 10-lead 15 x 15 mm bolt-down with a Cu base for superior thermal management. To simplify system integration, the QPA1314 is fully matched to 50 ohms with DC grounded I/O ports for optimum ESD performance.

The QPA1314 is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA1314 is 100% DC and RF tested to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

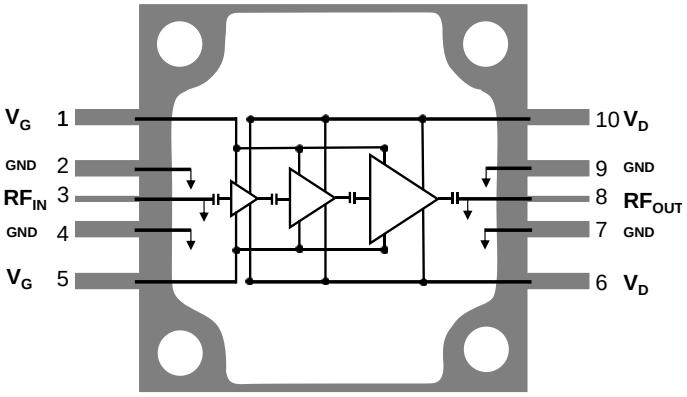


Key Features

- Frequency Range: 13.75 – 14.5 GHz
- Extended Frequency Range: 12.75 – 15.35 GHz
- Linear P_{OUT}: 43 dBm
- P_{OUT} (P_{IN} = 19 dBm): 46 dBm
- PAE (P_{IN} = 19 dBm): 30 %
- IM3 (P_{OUT}/Tone = 40 dBm): -25 dBc
- Small Signal Gain: 29 dB
- Bias: CW, V_D = 24 V, I_{DQ} = 680 mA, V_G = -2.3 V typical range
- Package Dimensions: 15.24 x 15.24 x 3.53 mm
- Package base is pure Cu offering superior thermal management.

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Satellite Communications
- Datalinks

Ordering Information

Part No.	Description
QPA1314	13.75 - 14.5 GHz 40 Watt GaN PA
QPA1314EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-6 V to 0 V
Drain Current Total (I_D), T_{BASE} = 85 °C	20 A
Gate Current (I_G)	See plot p. 23
Power Dissipation (P_{DISS}), T_{BASE} = 85 °C	140 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 24 V, I_{DQ} = 680 mA, T_{BASE} = 85 °C	32 dBm
Input Power (P_{IN}), 3:1 VSWR, CW, V_D = 24 V, I_{DQ} = 680 mA, T_{BASE} = 85 °C	32 dBm
Mounting Temperature	See Assembly Notes, p. 28
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D), CW (1)		24	24	V
Drain Current Quiescent (I_{DQ})		680		mA
Drain Current, RF (I_{D_Drive})	See plots p. 4,5,9,12,15			mA
Gate Voltage Typ. Range (V_G)	−1.9 to -3.1			V
Gate Current, RF (I_{G_Drive})	See plots p. 4,5			mA
Input Power (P_{IN})1/	T_{BASE} -40°C: 25			dBm
	T_{BASE} +25°C: 25			
	T_{BASE} +85 °C: 19			
Operating Temp. Range (T_{BASE}) (2)	−40		+85	ºC

1. Limited by channel temperature T_{CH}. For pulsed applications P_{IN} can be handled up to 21 dBm for 85^{0}C T_{BASE}. For P_{SAT} applications, see Electrical Specifications' note 4.

2. T_{BASE} is back side of QPA1314 (see p. 25 Offset Temperature based on Qorvo's EVB design for reference)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

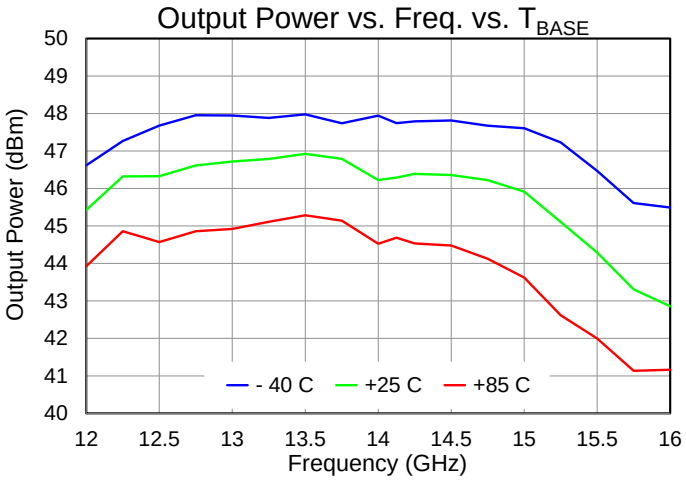
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		13.75 (3)		14.5 (3)	GHz
Output Power (4), P_{OUT}	P_{IN} = 19 dBm (4), Frequency = 13.75 – 14.5 GHz		46 (4)		dBm
	P_{IN} = 19 dBm (4), Frequency = 12.75 – 15.35 GHz (3)		45 (4)		
Power Added Efficiency (4), PAE	P_{IN} = 19 dBm (4), Frequency = 13.75 – 14.5 GHz		30		%
	P_{IN} = 19 dBm (4), Frequency = 12.75 – 15.35 GHz (3)		25		
Large Signal Gain	P_{IN} = 19 dBm (4)		27		dB
3RD Intermodulation Products, IM3	P_{OUT}/Tone = 40 dBm (4dBm backoff from P_{SAT} (4))		-25		dBc
5RD Intermodulation Products, IM5	Tone Spacing = 20 MHz		-35		
Small Signal Gain, S21	P_{IN} = -30 dBm		29		dB
Input Return Loss, IRL			15		
Output Return Loss, ORL			7		
P_{SAT} Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC; P_{IN} = 19 dBm		-0.04		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC		-0.19		dB/ºC

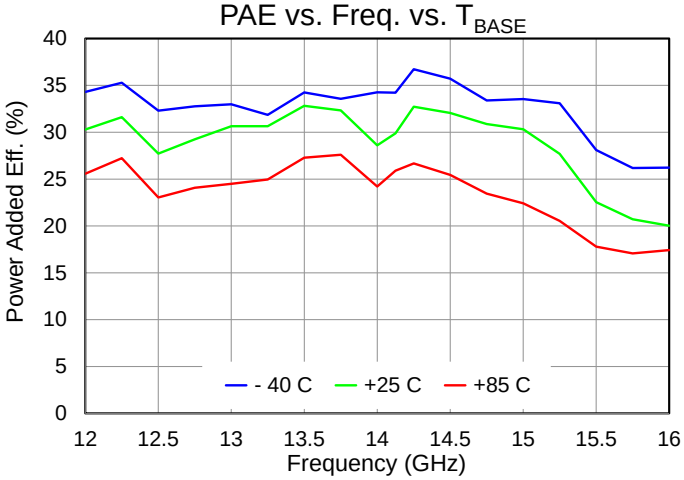
Notes:

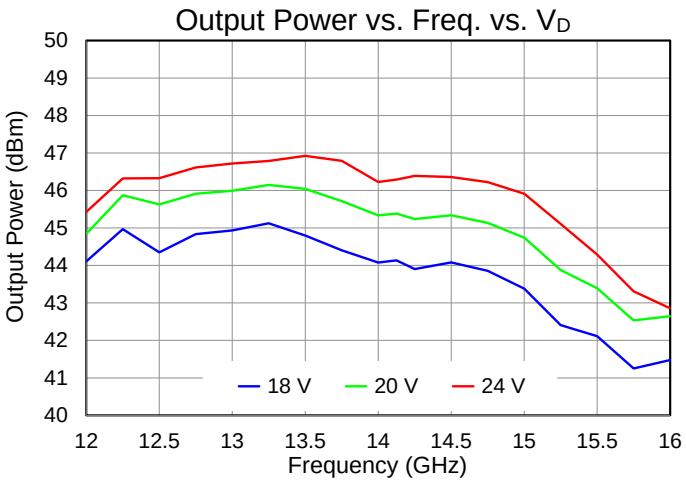
1. Test conditions unless otherwise noted: CW, V_D = 24 V, I_D = 680 mA, V_G = -2.3 V +/- 0.6V typical, T_{BASE} = +25ºC, Z_0 = 50 Ω (RF reference planes are at QPA1314')
2. T_{BASE} is back side of QPA1314 (see p. 25 Offset Temperature based on Qorvo's EVB design for reference)
3. Extended frequency range: 12.75 – 15.35 GHz
4. Limited by T_{CH}, for P_{SAT} applications where P_{IN} ≥ 25dBm the T_{BASE} must be reduced to ≤ 25^{0}C, resulted P_{SAT} = 47.5 dBm (55W), see plots page 6.

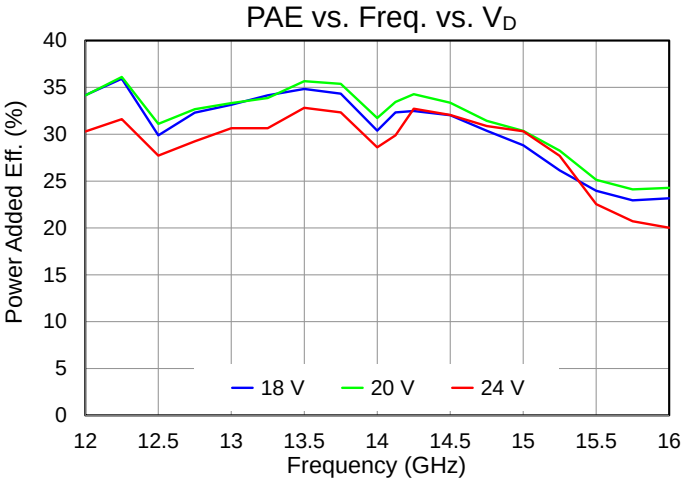
Performance Plots – Large Signal (CW)

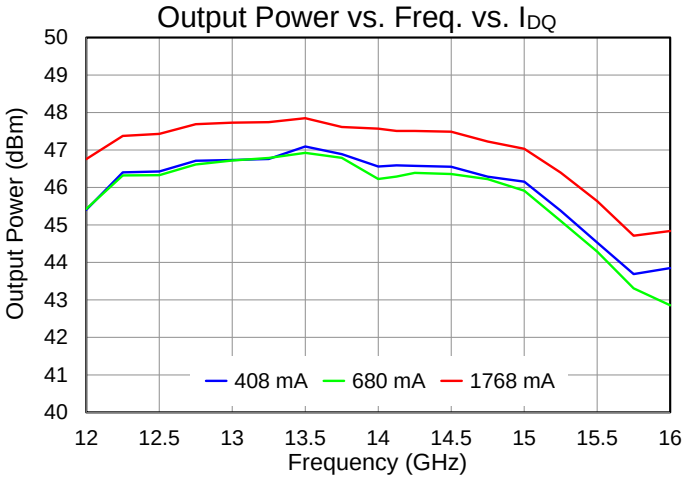
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, P_{IN} = 19 dBm (P_{IN} P_{OUT} are limited by T_{CH}, 19 dBm is not at P_{SAT} level), T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

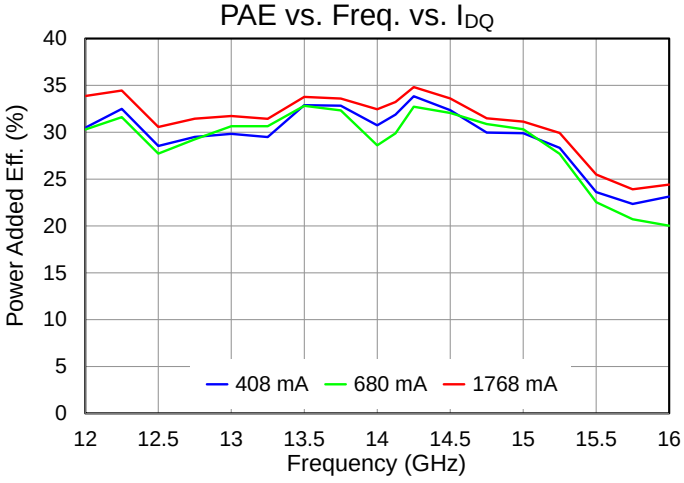








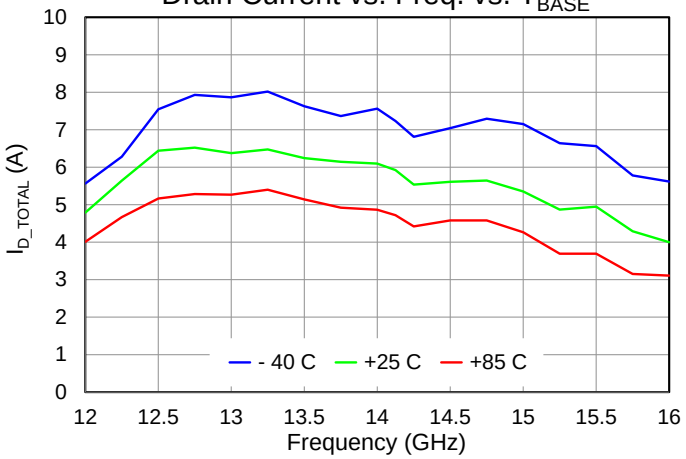




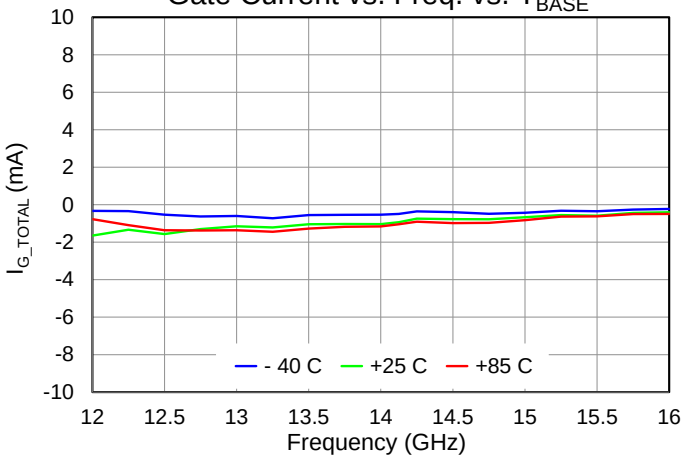
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, P_{IN} = 19 dBm (P_{IN} P_{OUT} are limited by T_{CH}, 19 dBm is not at P_{SAT} level), T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

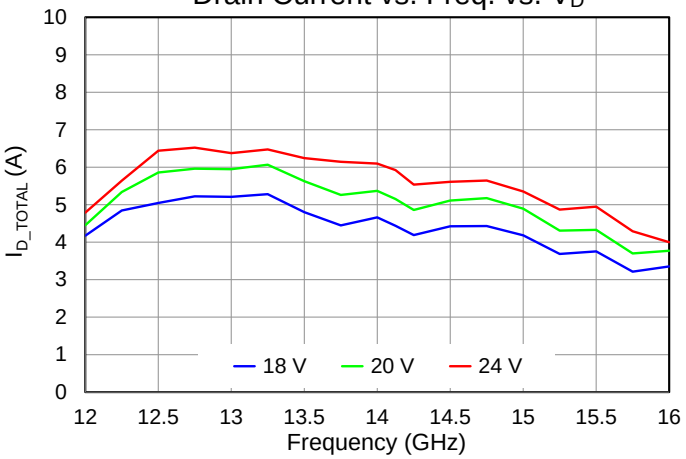
Drain Current vs. Freq. vs. T_{BASE}



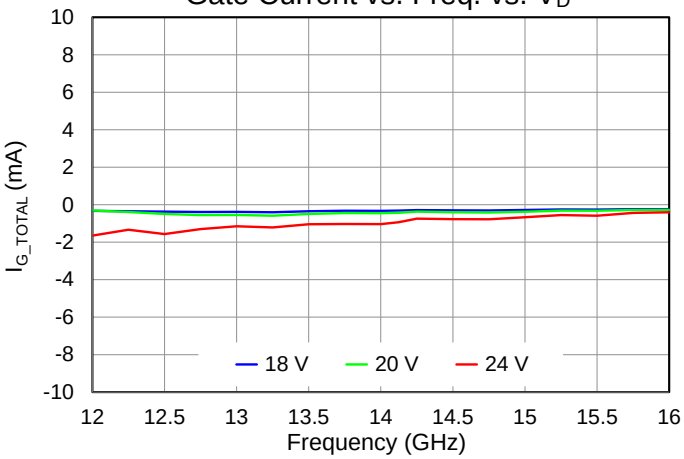
Gate Current vs. Freq. vs. T_{BASE}



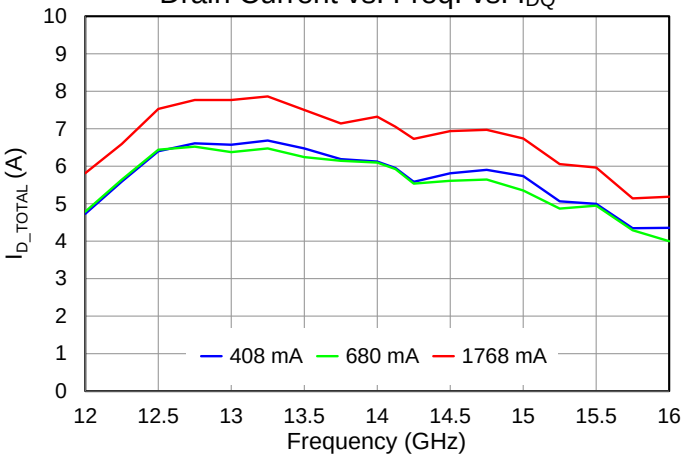
Drain Current vs. Freq. vs. V_D



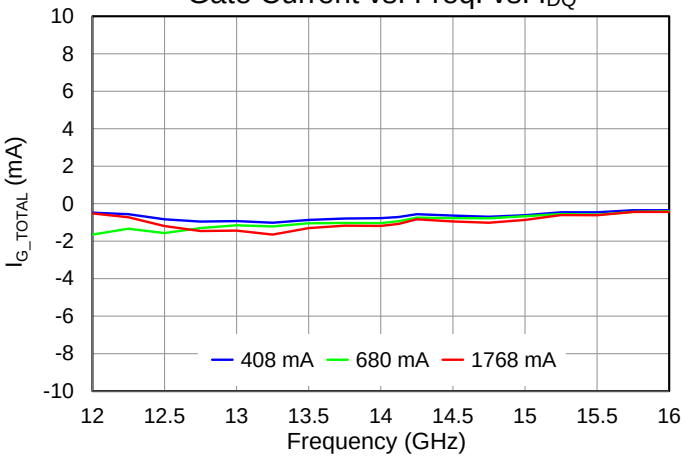
Gate Current vs. Freq. vs. V_D



Drain Current vs. Freq. vs. I_{DQ}



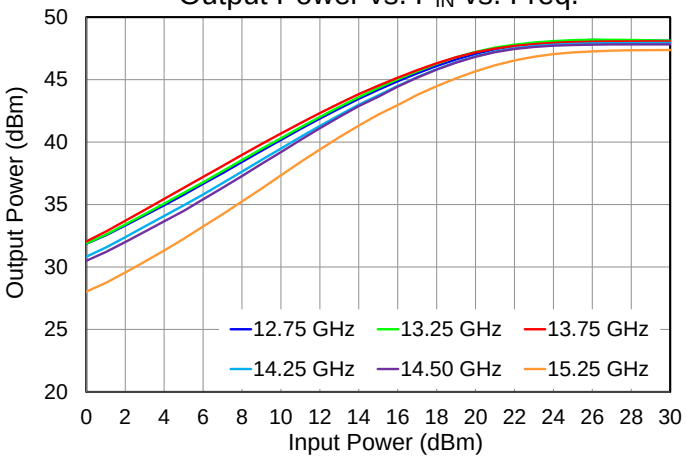
Gate Current vs. Freq. vs. I_{DQ}



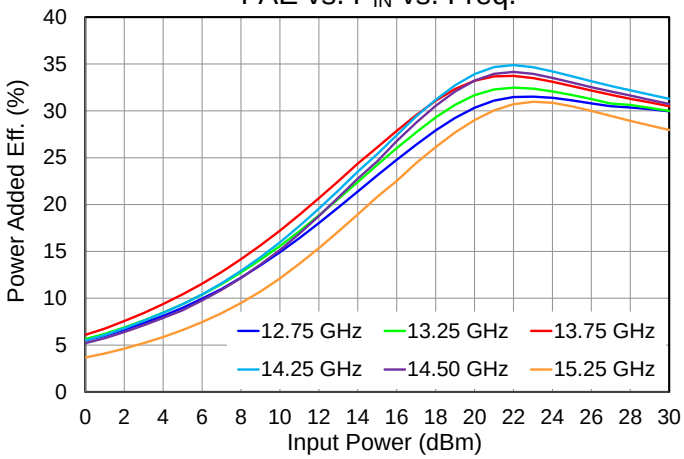
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, P_{IN} = 19 dBm (P_{IN} P_{OUT} are limited by T_{CH}, 19 dBm is not at P_{SAT} level), T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

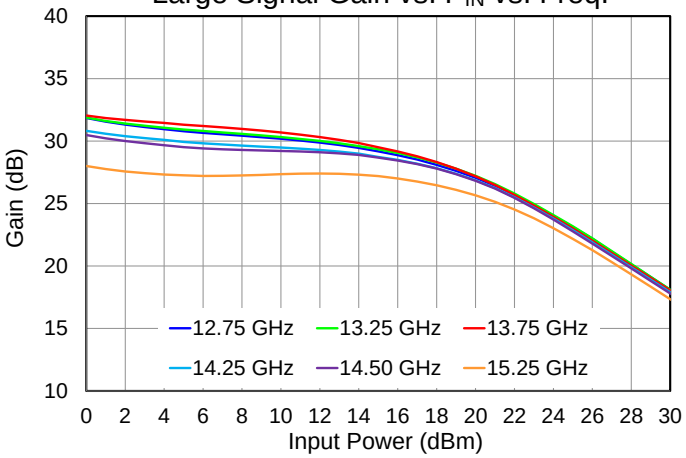
Output Power vs. P_{IN} vs. Freq.



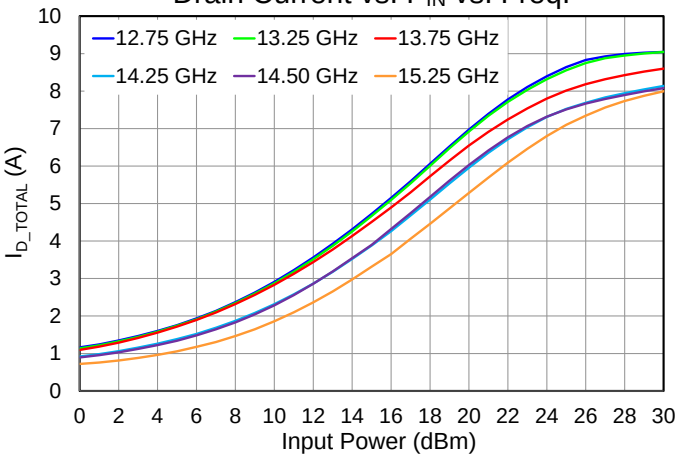
PAE vs. P_{IN} vs. Freq.



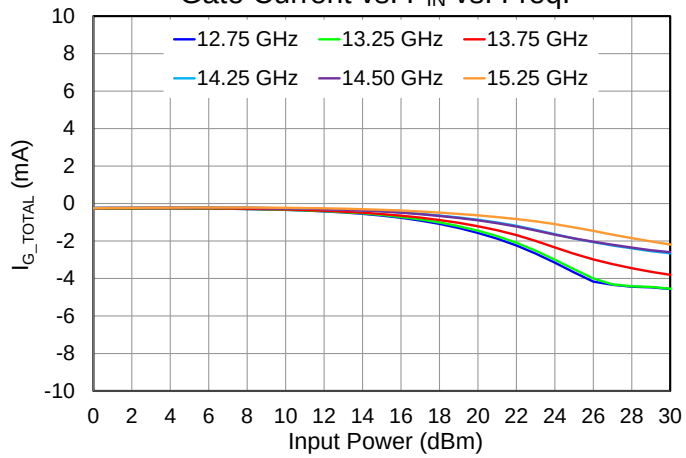
Large Signal Gain vs. P_{IN} vs. Freq.



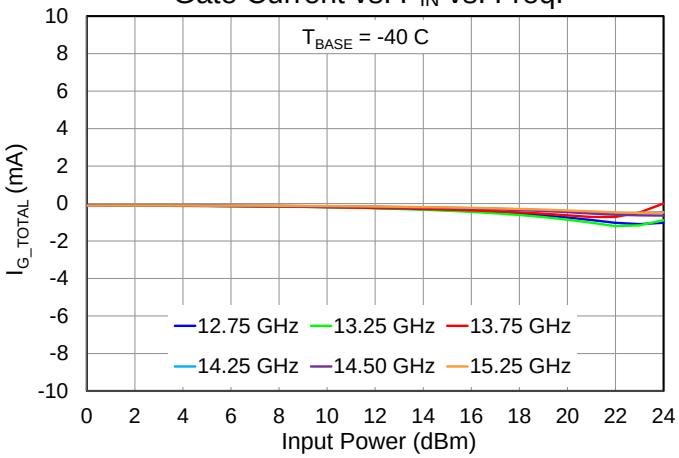
Drain Current vs. P_{IN} vs. Freq.



Gate Current vs. P_{IN} vs. Freq.



Gate Current vs. P_{IN} vs. Freq.



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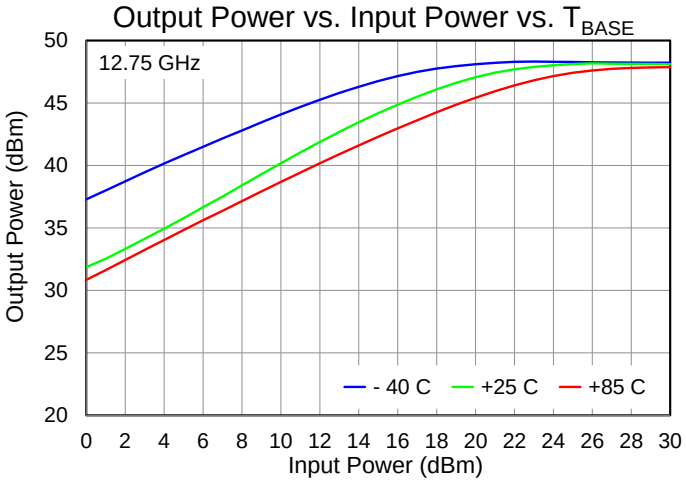

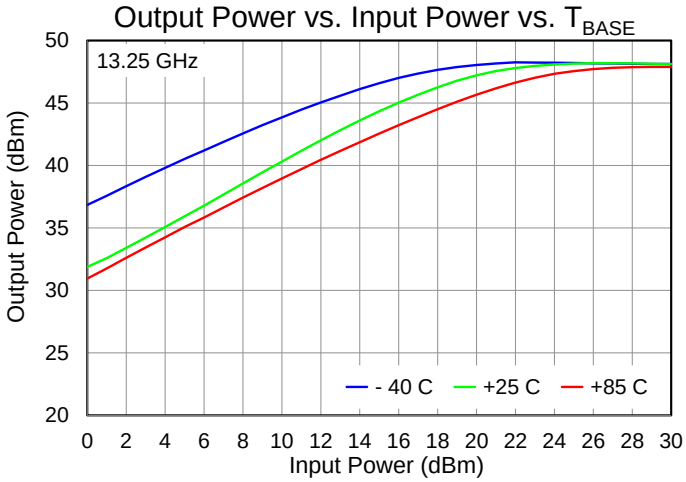

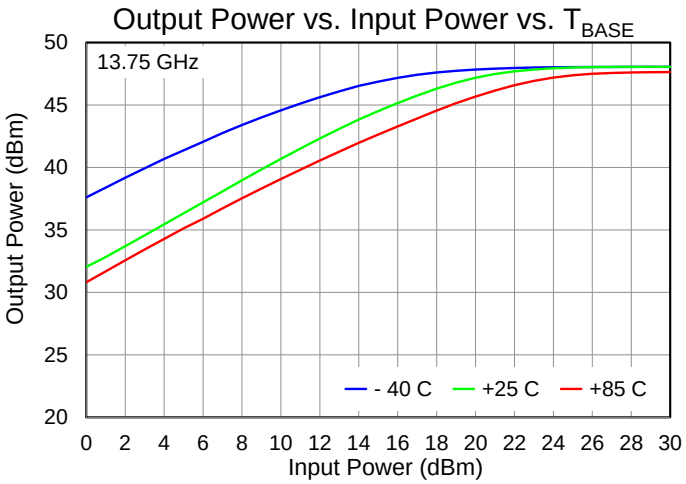

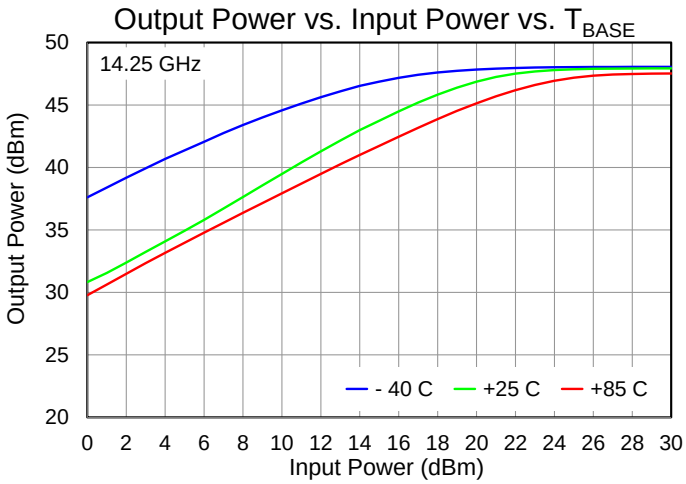

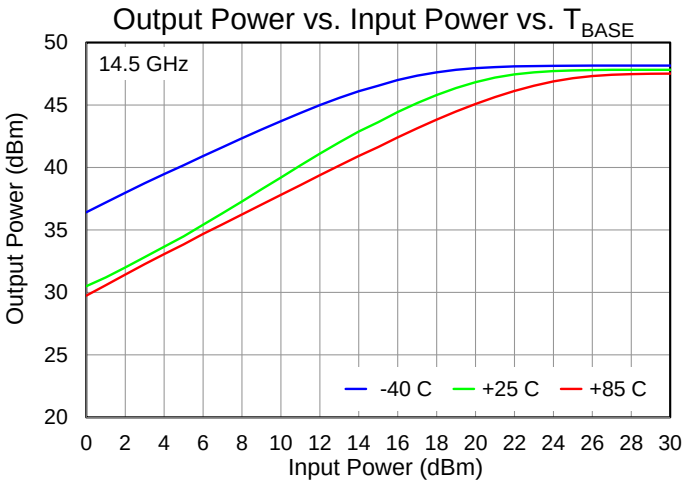

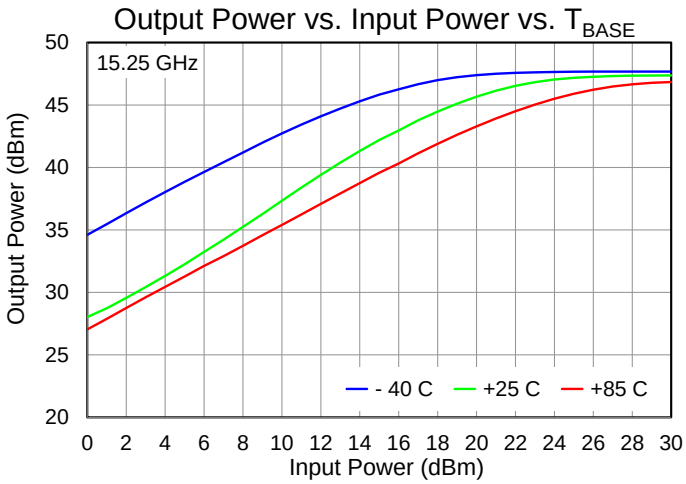

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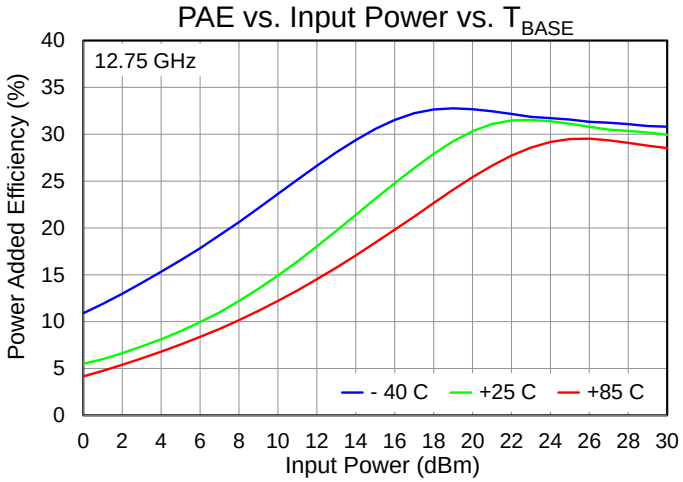

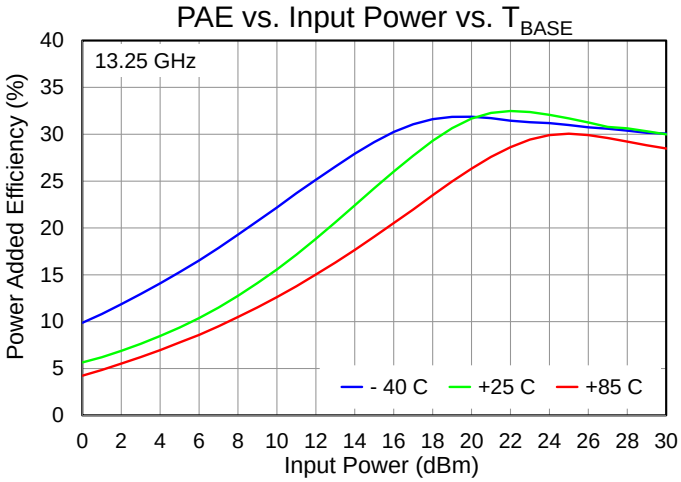

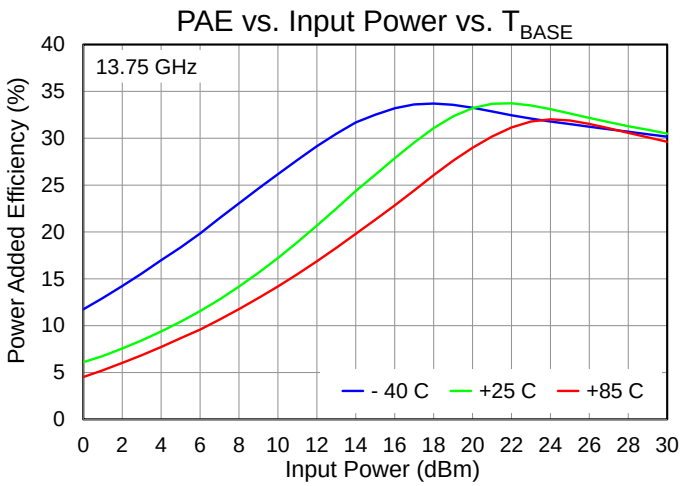

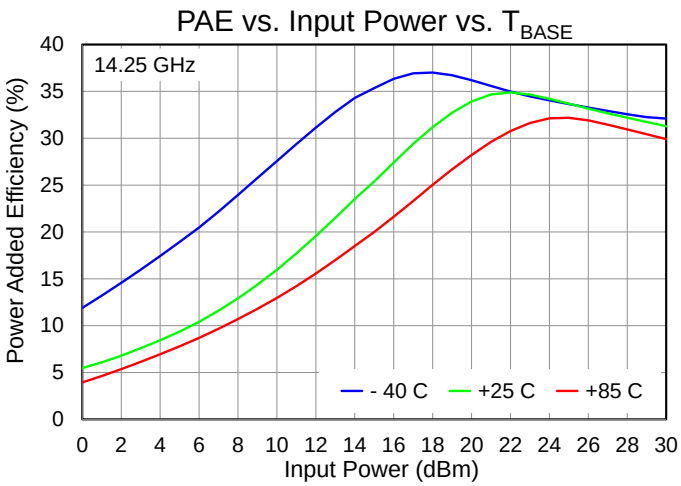

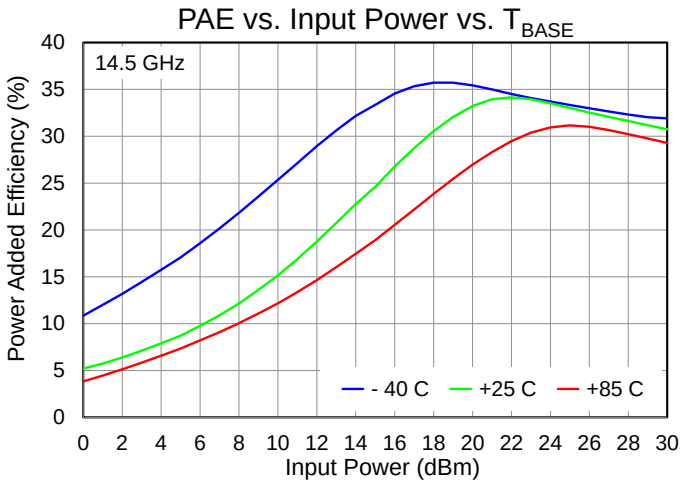

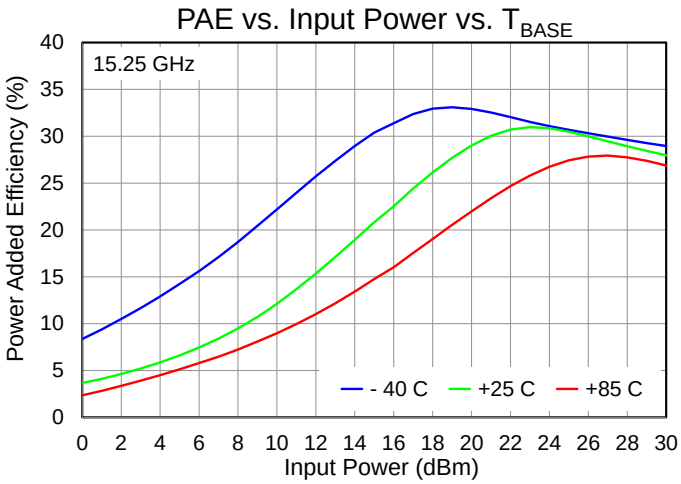

Performance Plots – Large Signal (CW)

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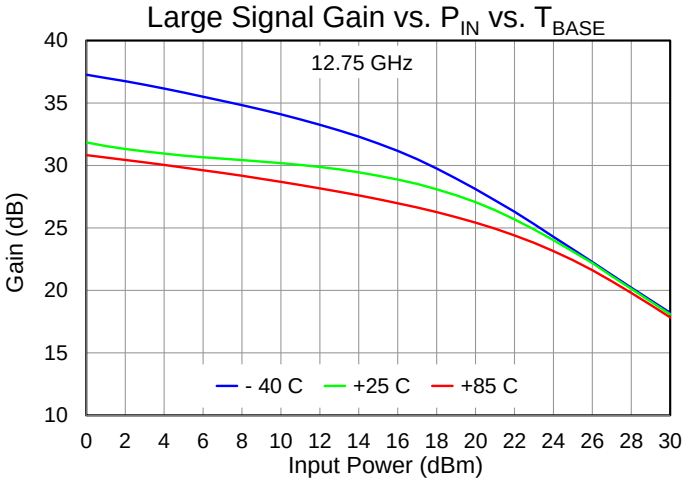
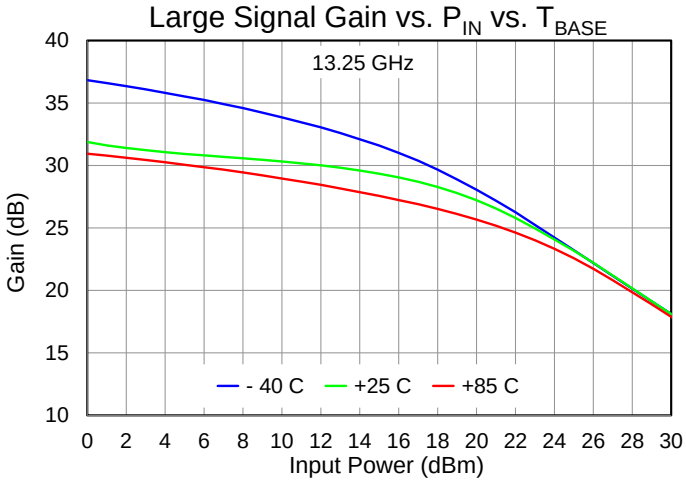
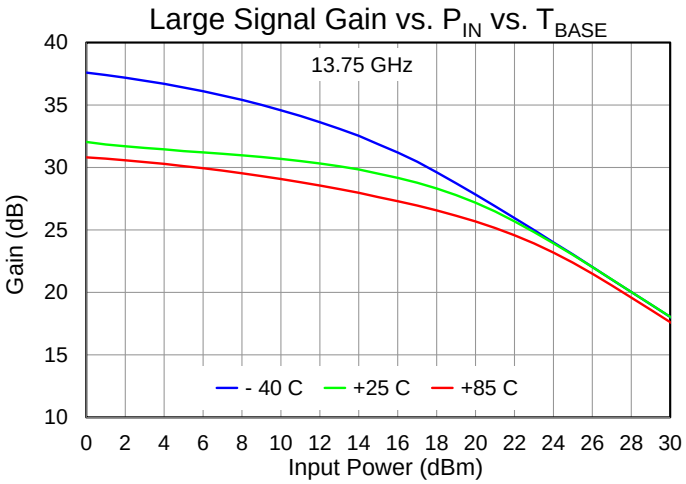
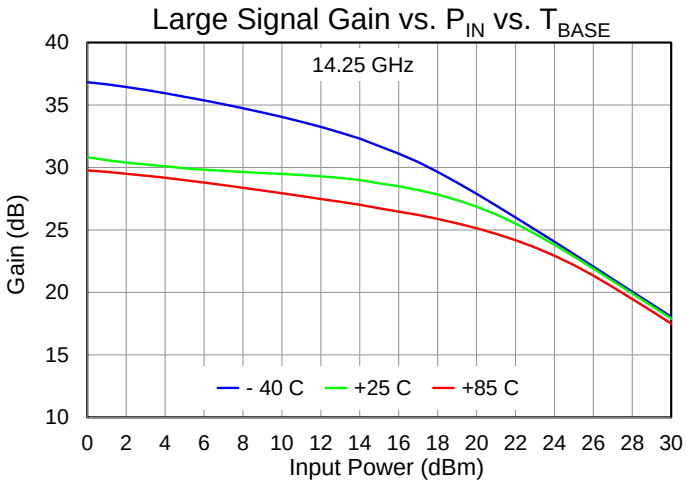
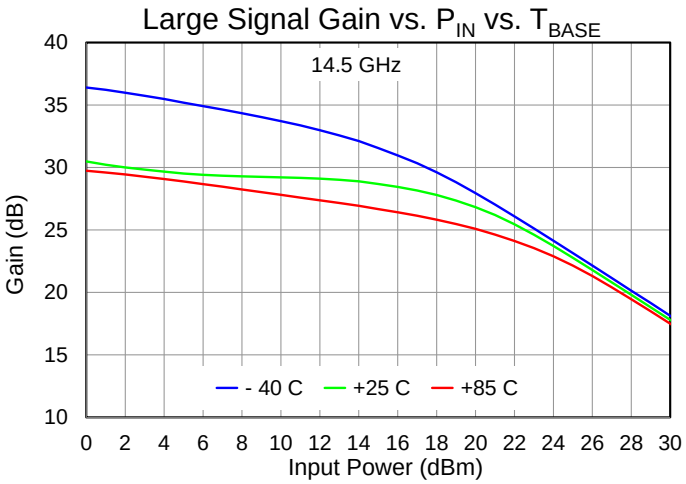
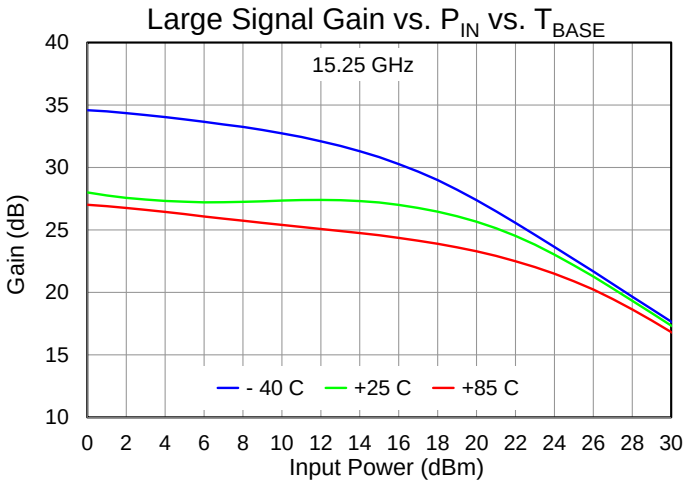






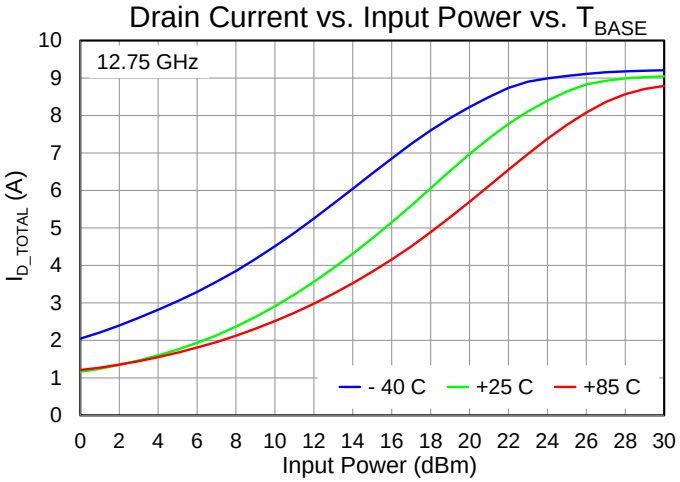


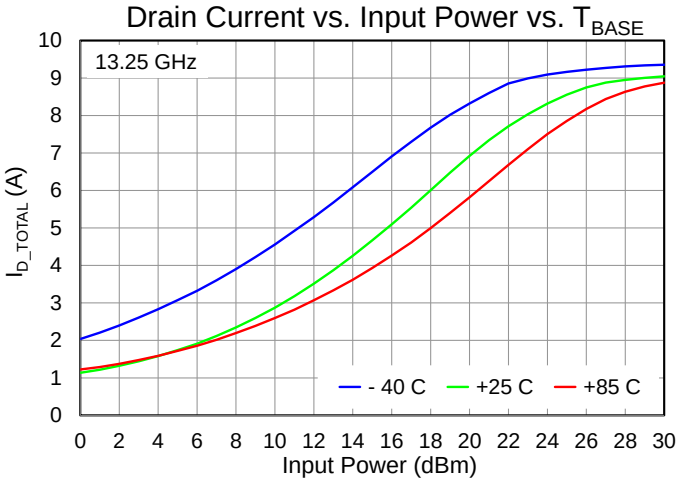


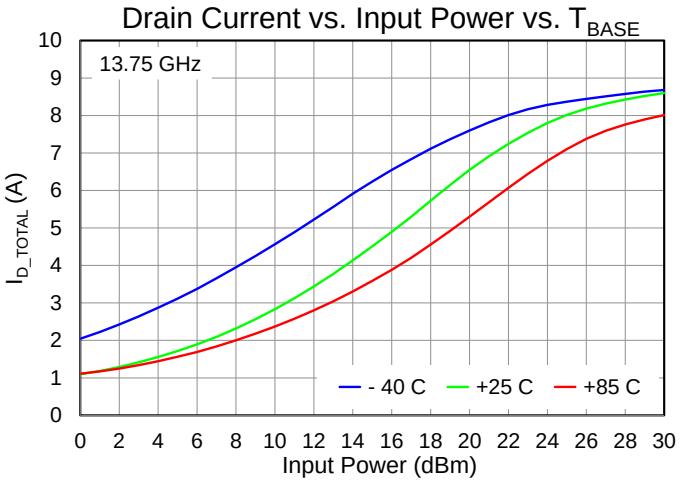


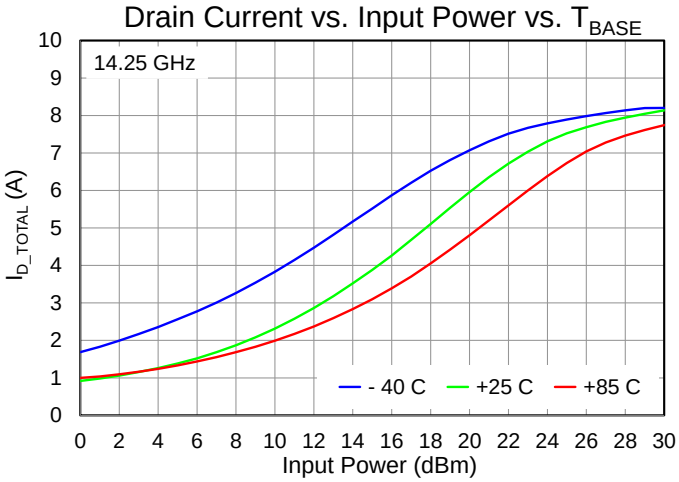
Performance Plots – Large Signal (CW)

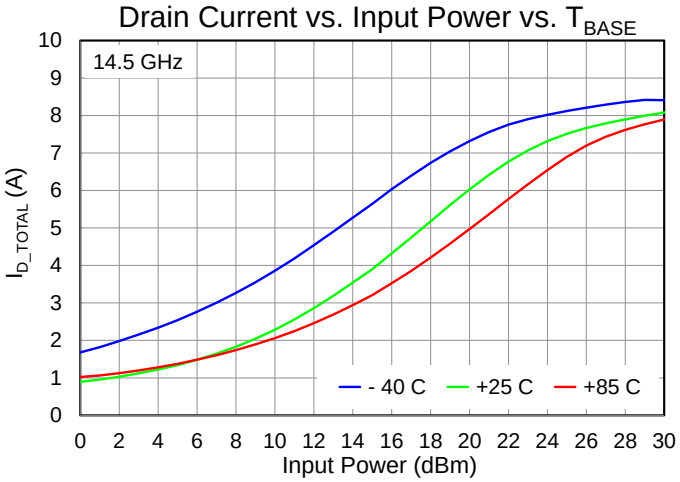
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

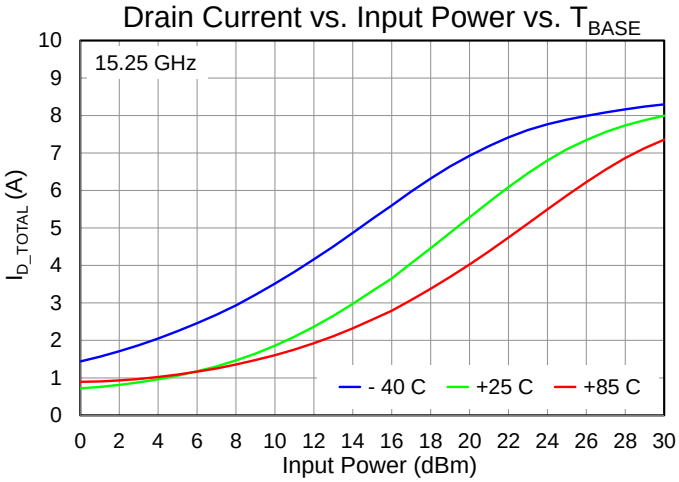








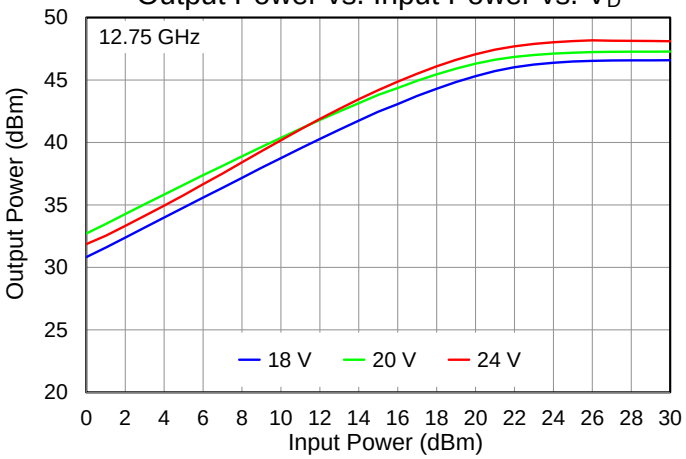




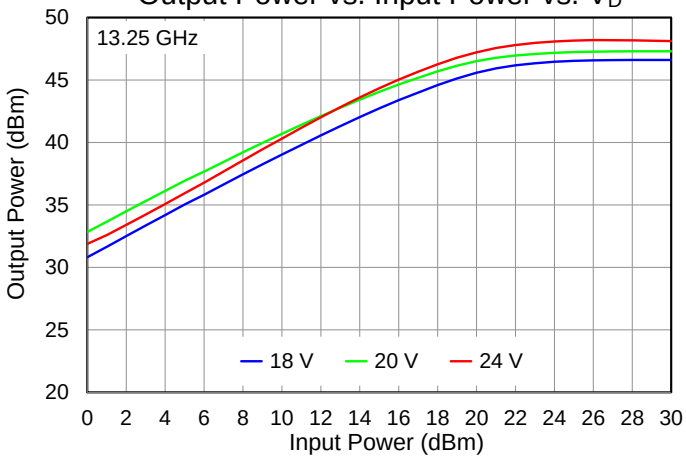
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 °C (T_{BASE} is backside of QPA1314).

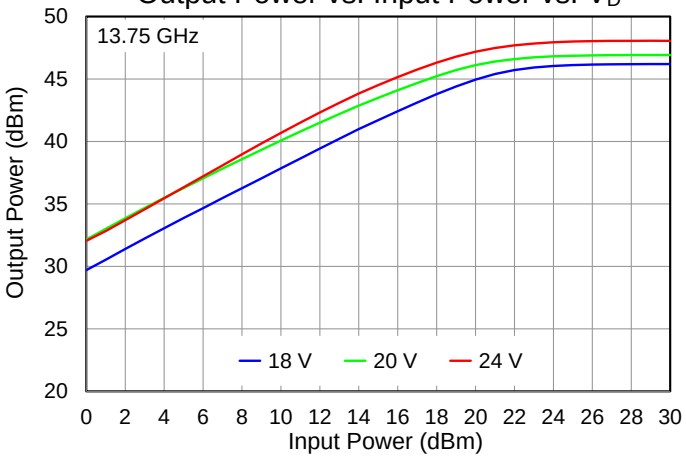
Output Power vs. Input Power vs. V_D



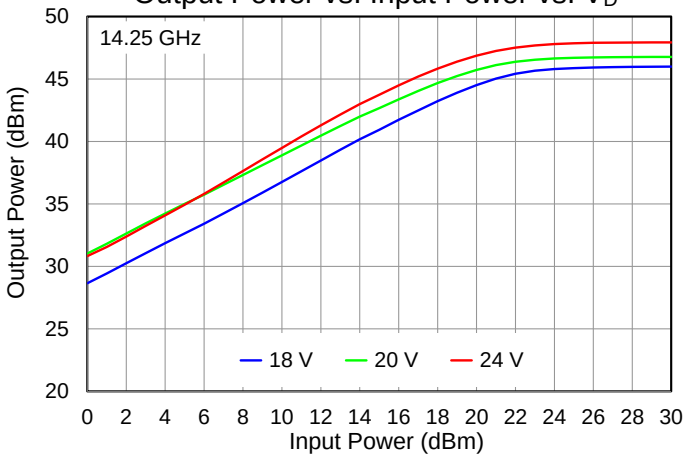
Output Power vs. Input Power vs. V_D



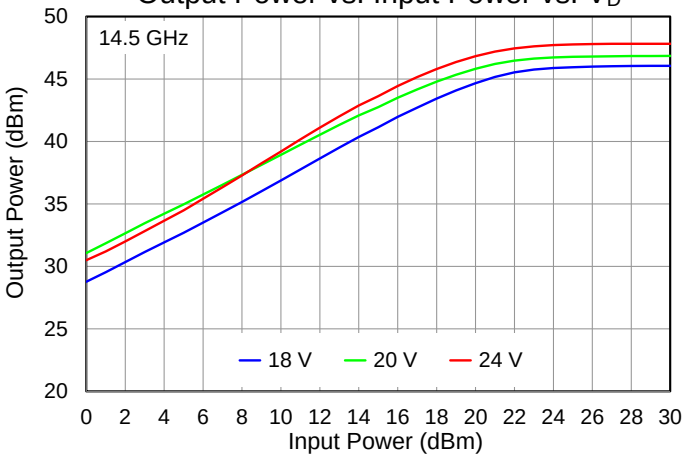
Output Power vs. Input Power vs. V_D



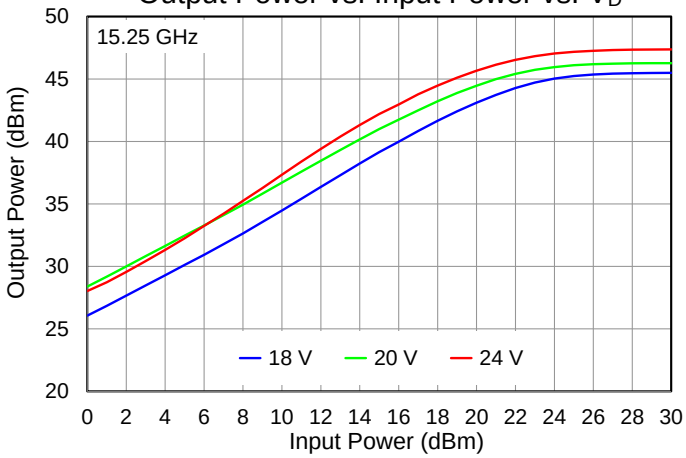
Output Power vs. Input Power vs. V_D



Output Power vs. Input Power vs. V_D



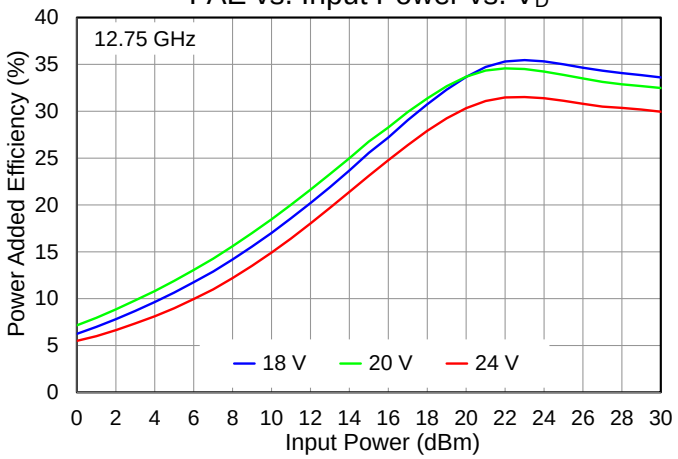
Output Power vs. Input Power vs. V_D



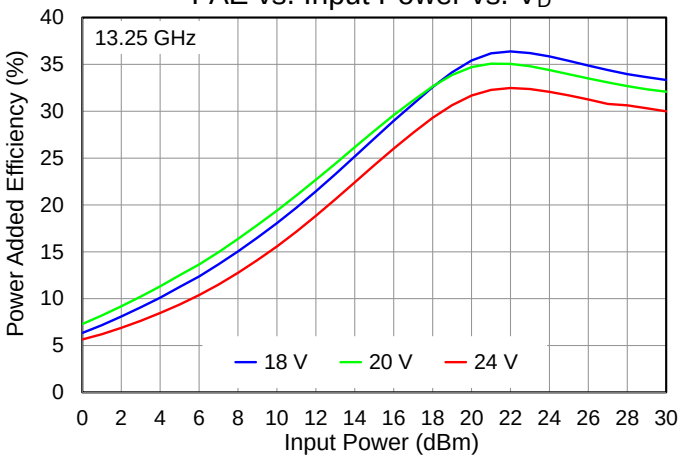
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 °C (T_{BASE} is backside of QPA1314).

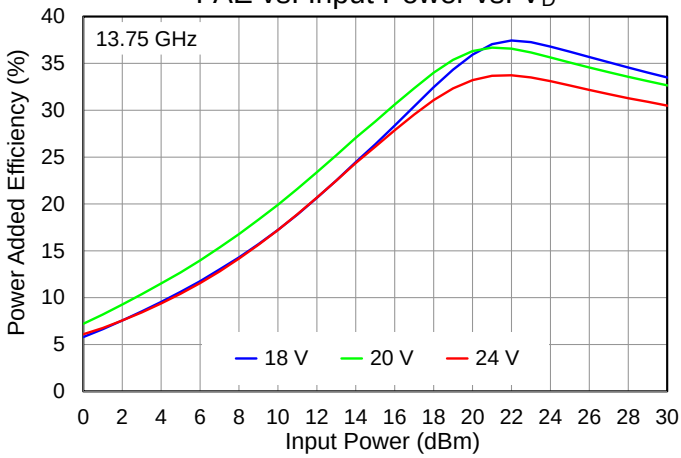
PAE vs. Input Power vs. V_D



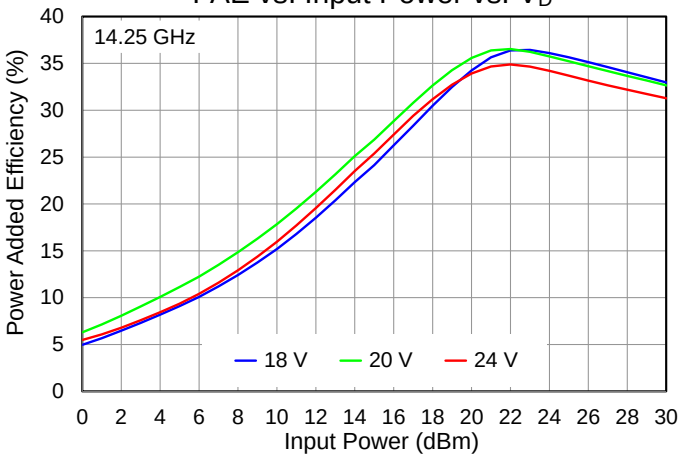
PAE vs. Input Power vs. V_D



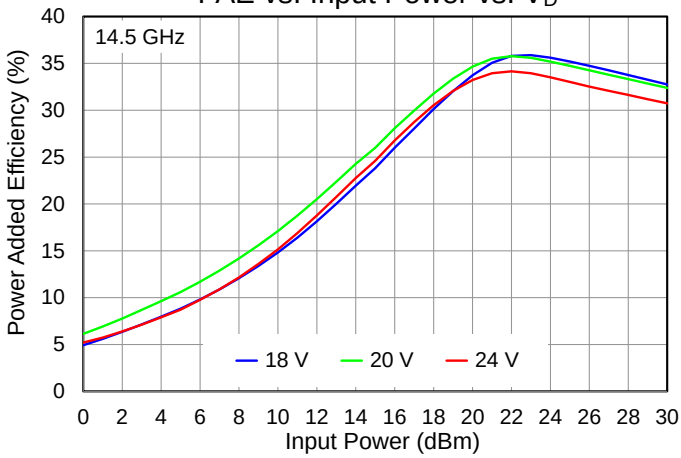
PAE vs. Input Power vs. V_D



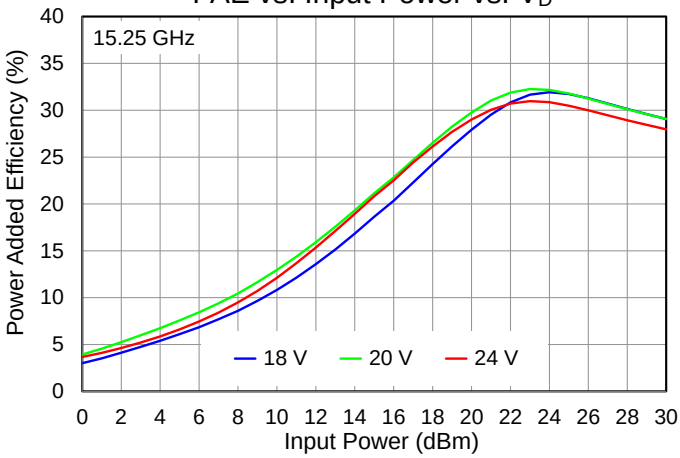
PAE vs. Input Power vs. V_D



PAE vs. Input Power vs. V_D

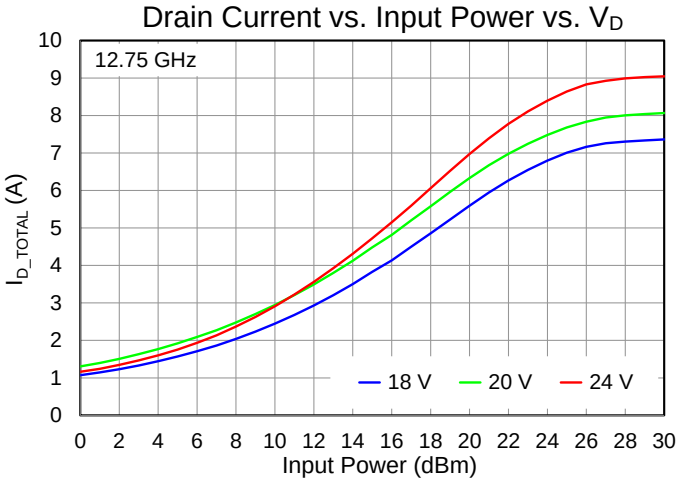


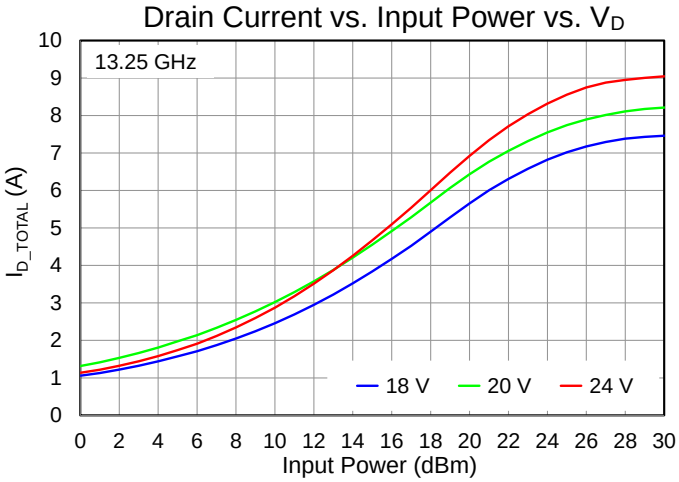
PAE vs. Input Power vs. V_D

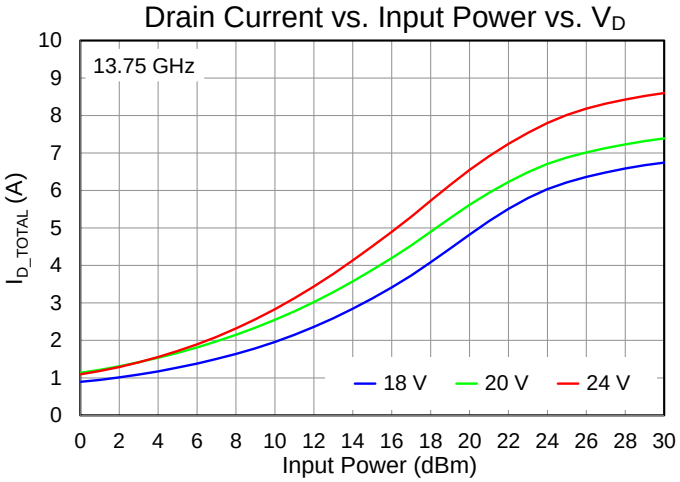


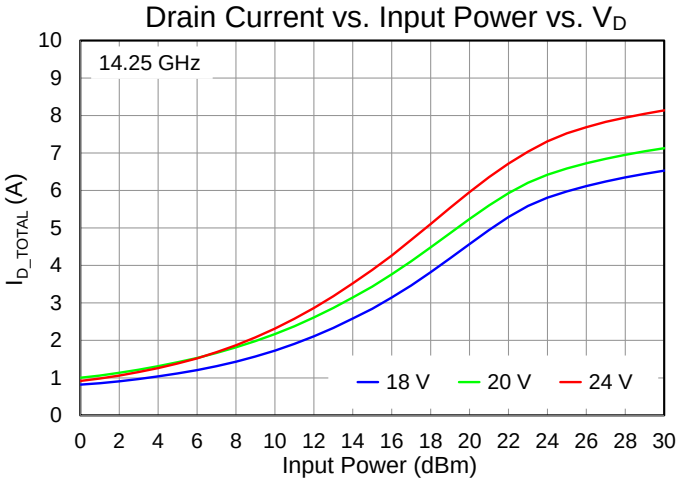
Performance Plots – Large Signal (CW)

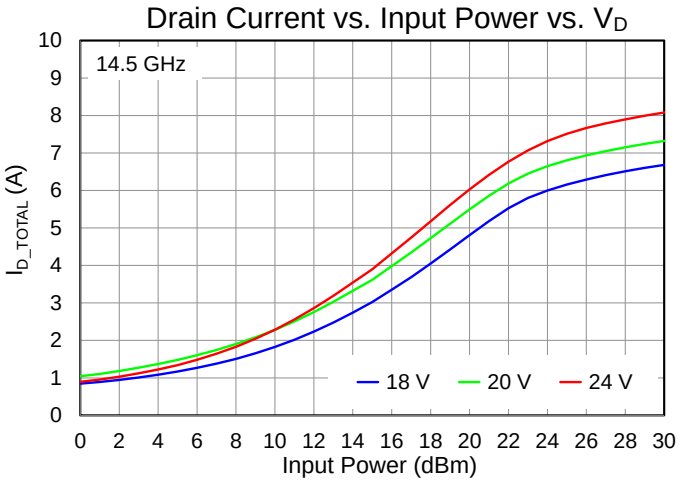
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

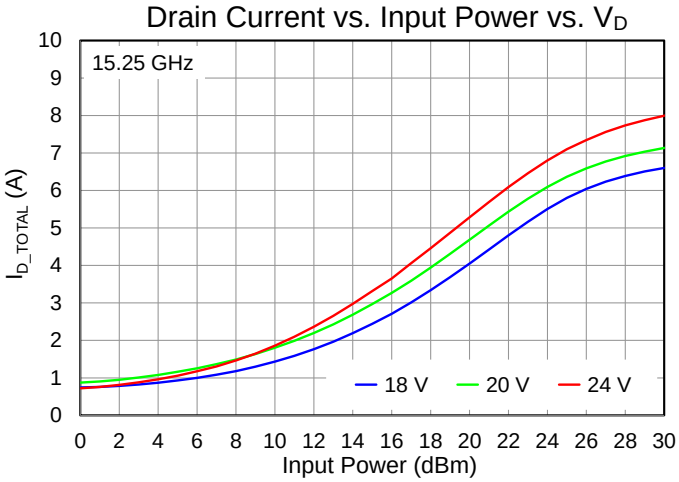






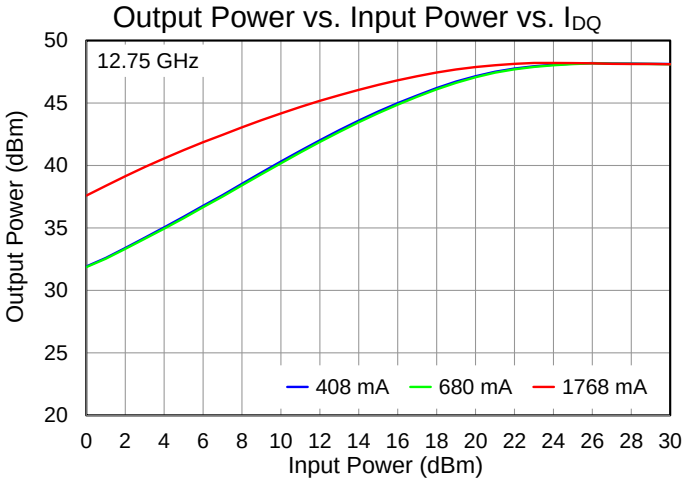


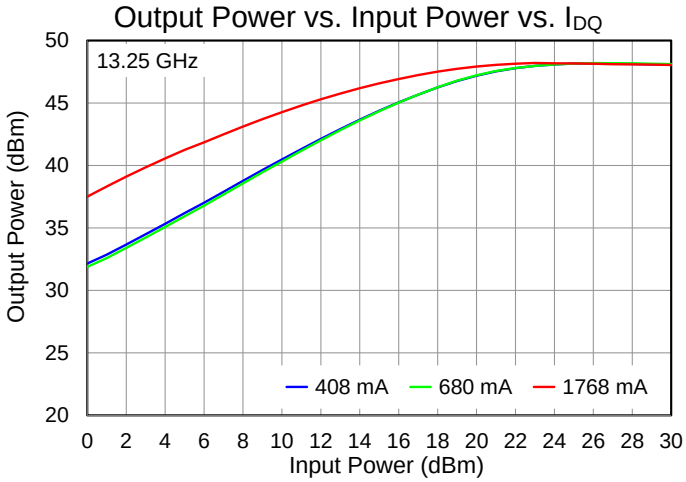


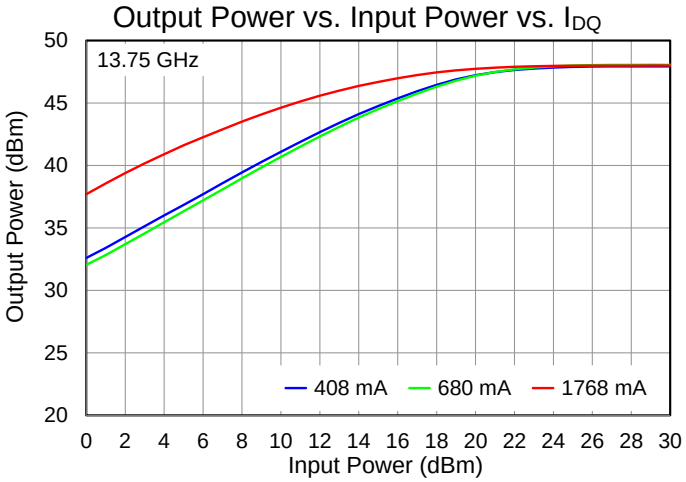


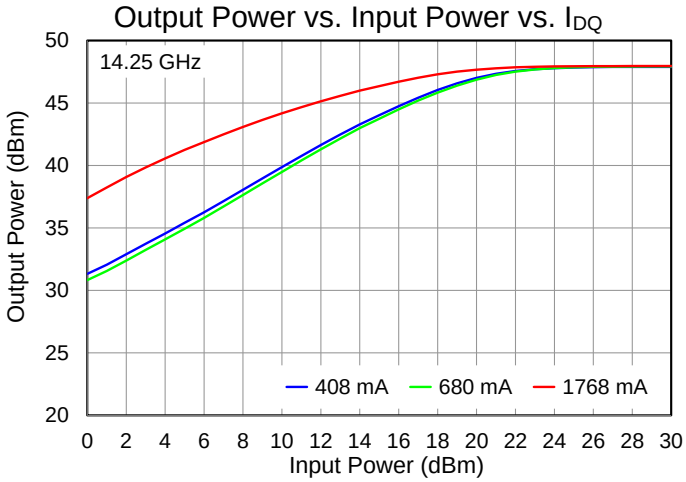
Performance Plots – Large Signal (CW)

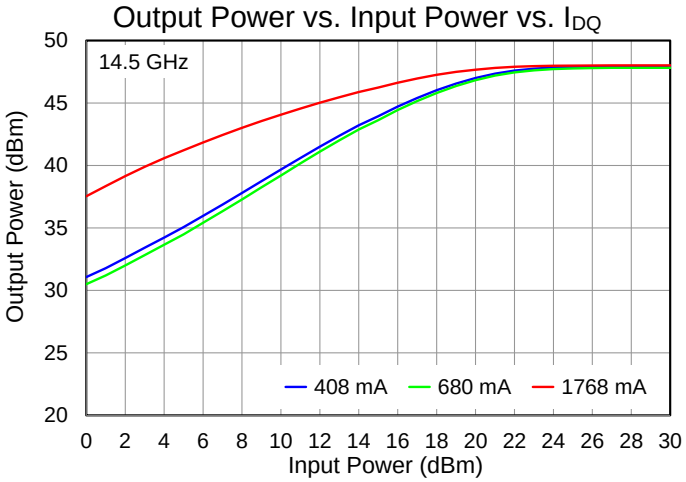
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

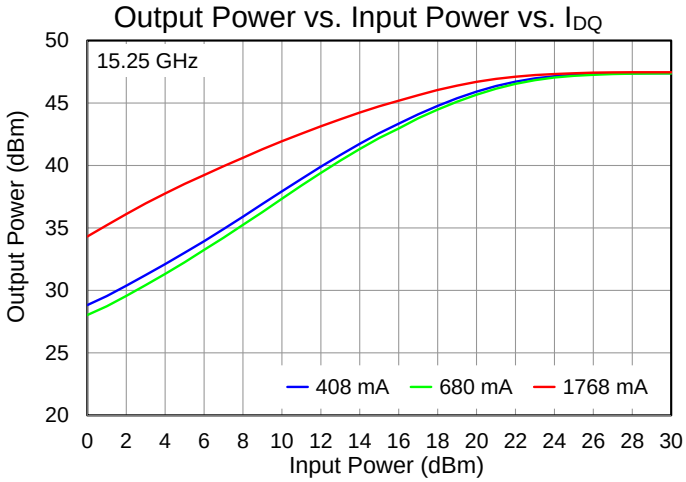








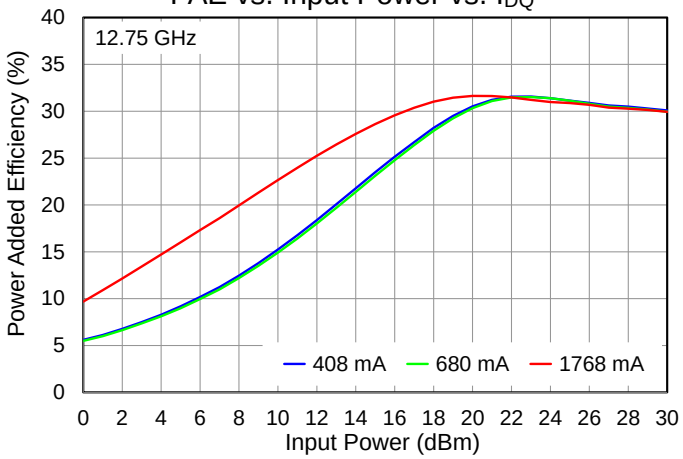




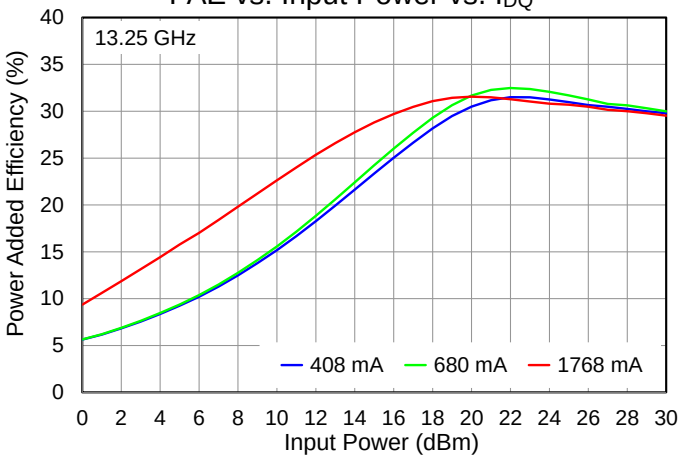
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

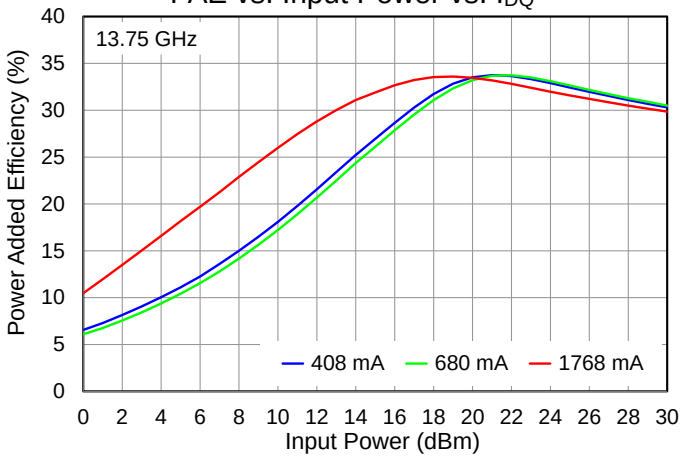
PAE vs. Input Power vs. I_{DQ}



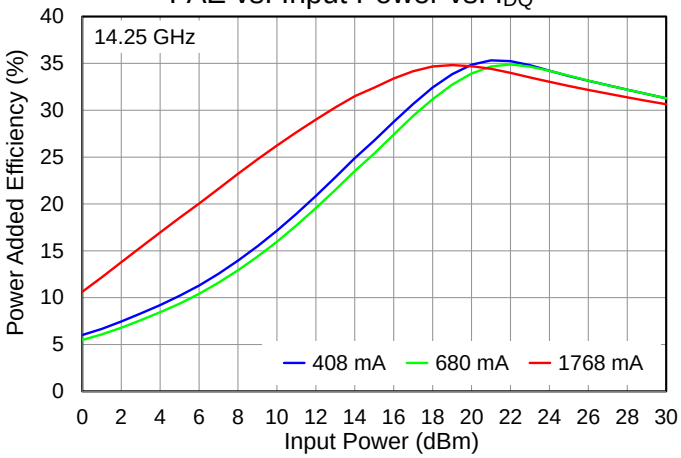
PAE vs. Input Power vs. I_{DQ}



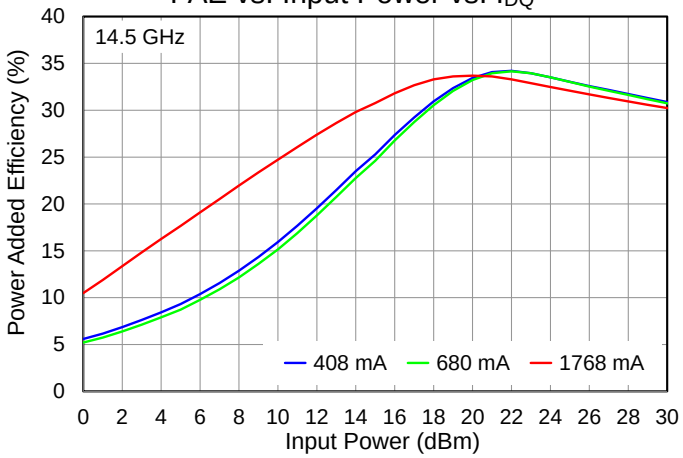
PAE vs. Input Power vs. I_{DQ}



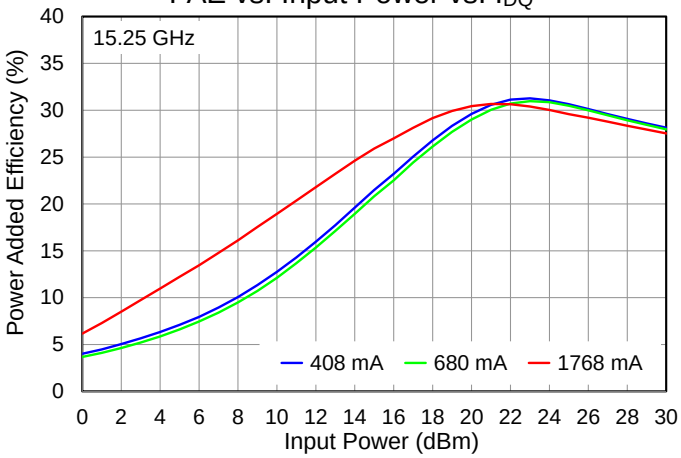
PAE vs. Input Power vs. I_{DQ}



PAE vs. Input Power vs. I_{DQ}



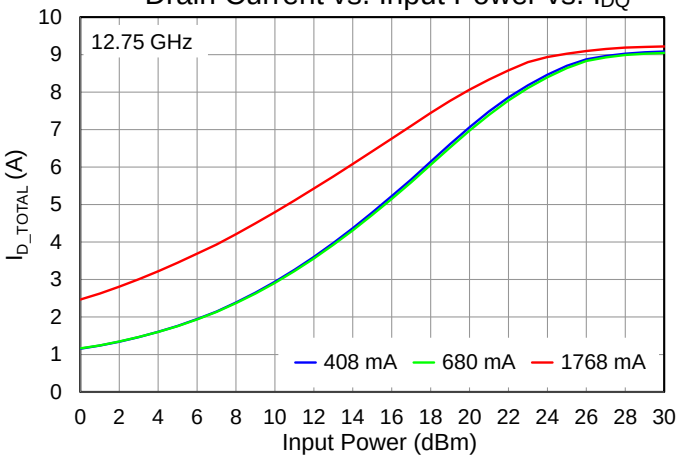
PAE vs. Input Power vs. I_{DQ}



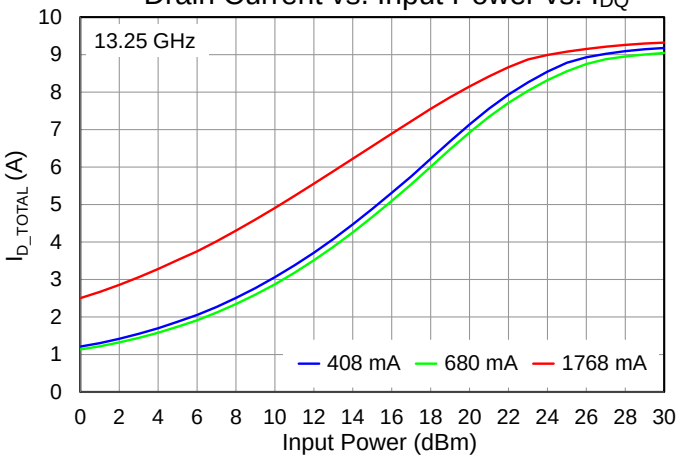
Performance Plots – Large Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, see Recommended Operating Conditions on page 2 for P_{IN}, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

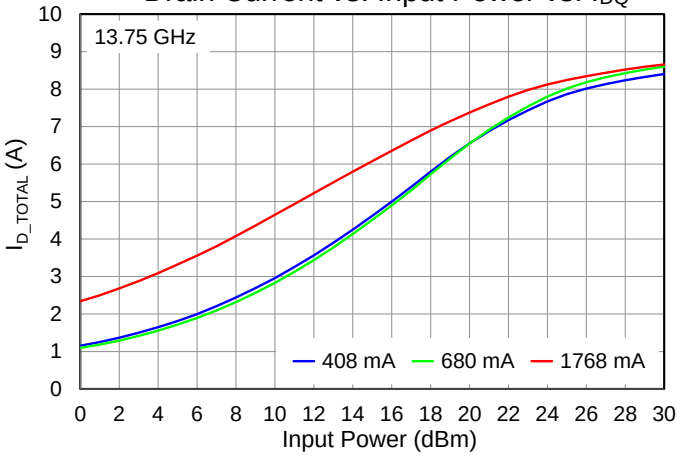
Drain Current vs. Input Power vs. I_{DQ}



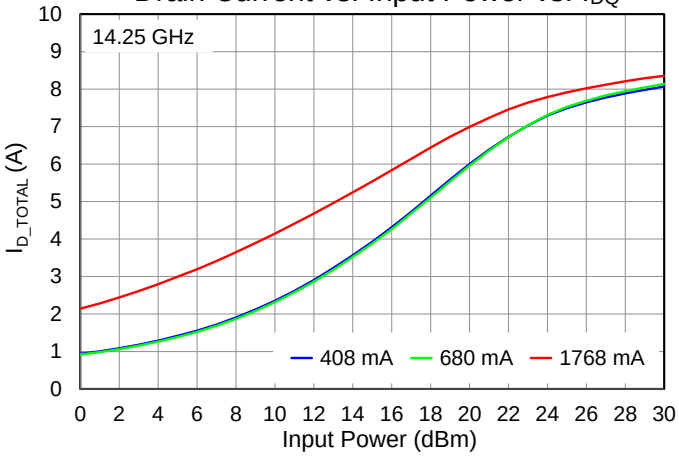
Drain Current vs. Input Power vs. I_{DQ}



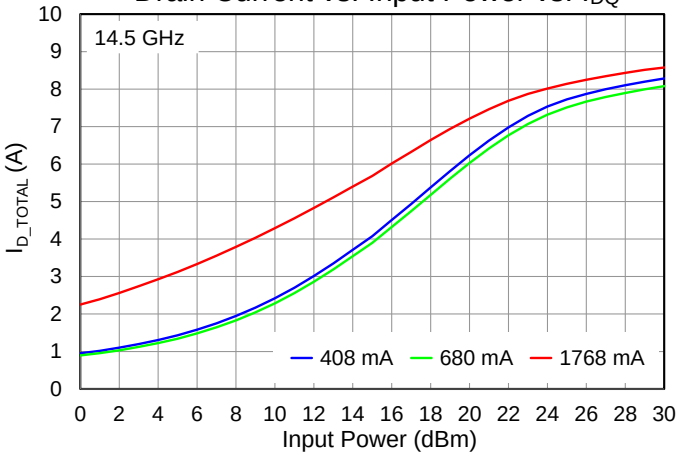
Drain Current vs. Input Power vs. I_{DQ}



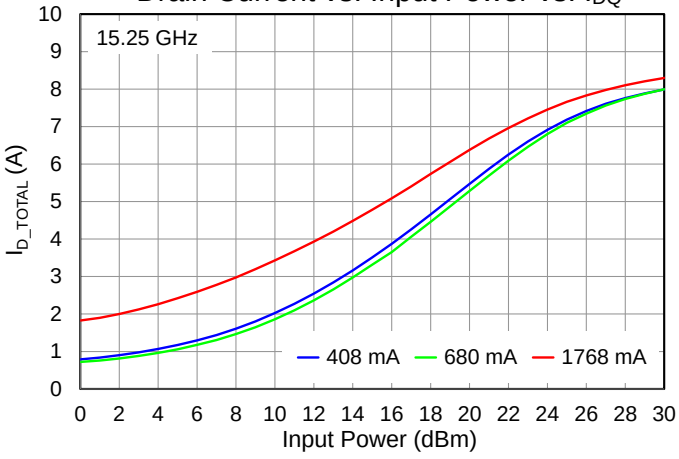
Drain Current vs. Input Power vs. I_{DQ}



Drain Current vs. Input Power vs. I_{DQ}

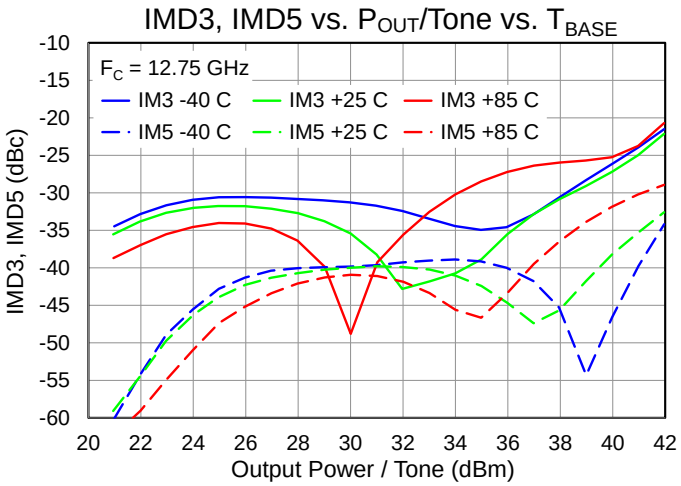


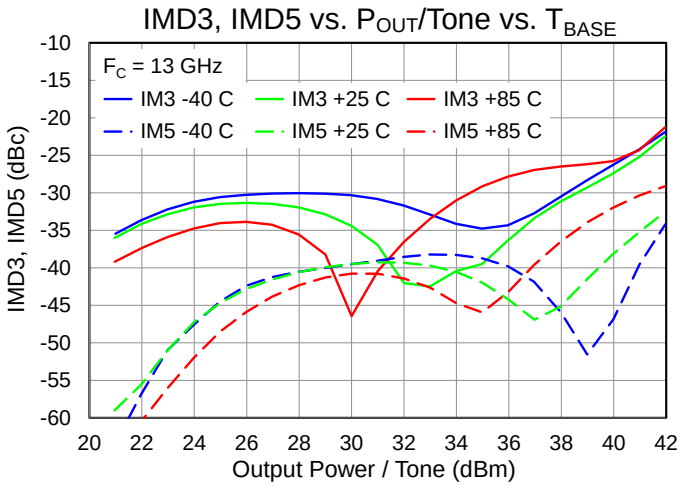
Drain Current vs. Input Power vs. I_{DQ}

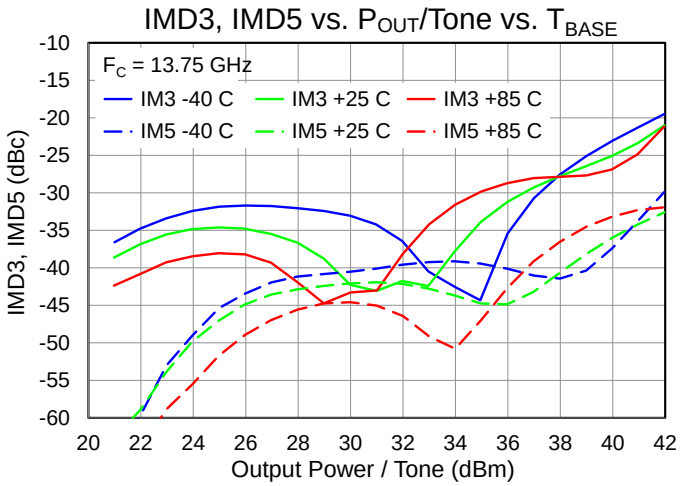


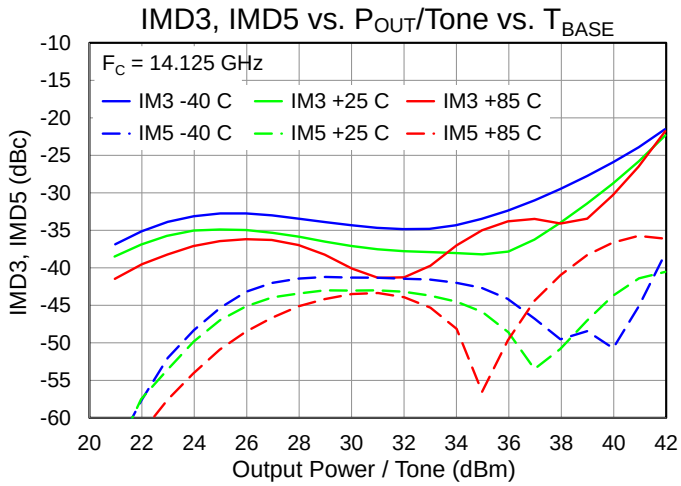
Performance Plots – Linearity (CW)

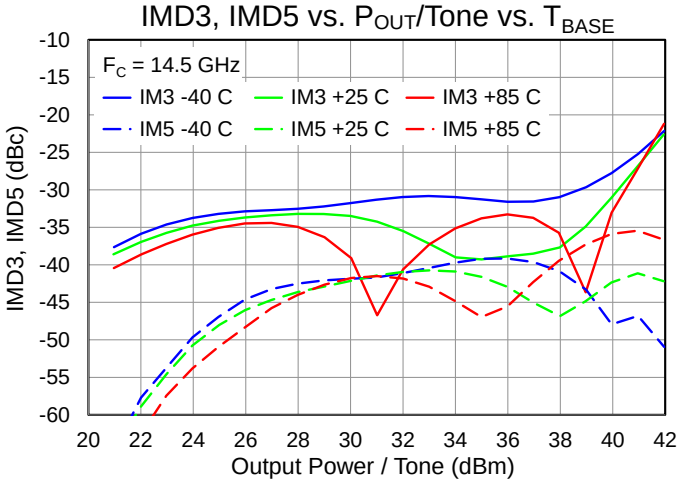
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, Tone Spacing = 20 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

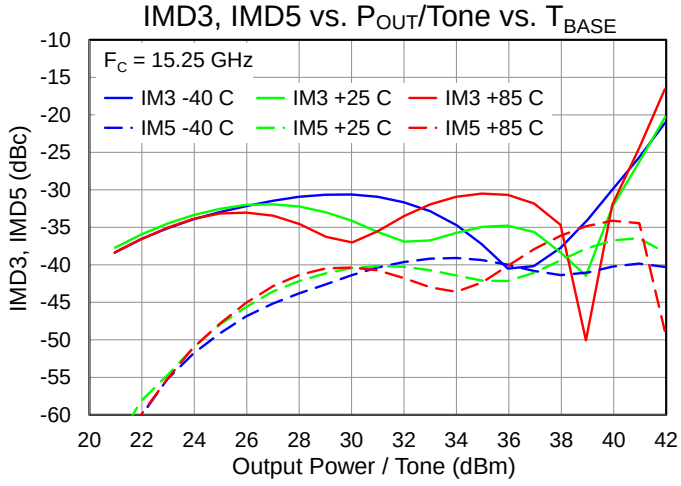








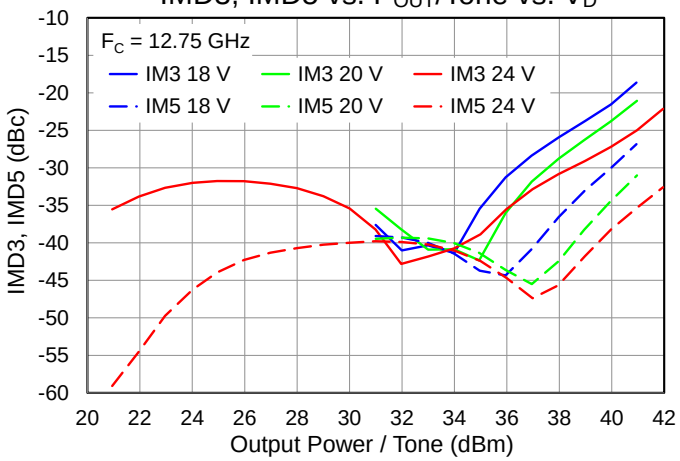




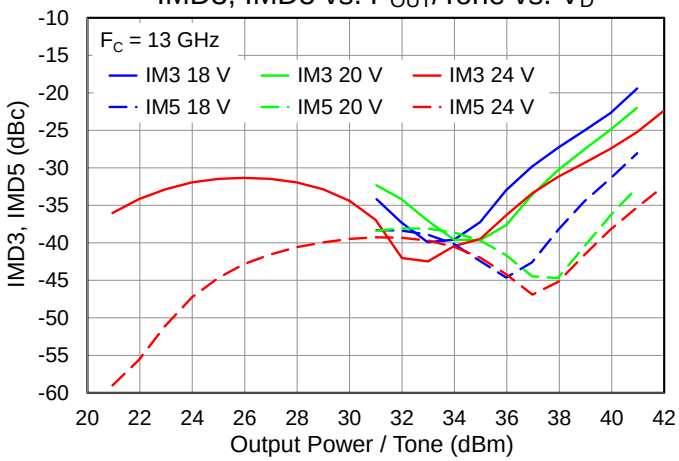
Performance Plots – Linearity (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, Tone Spacing = 20 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

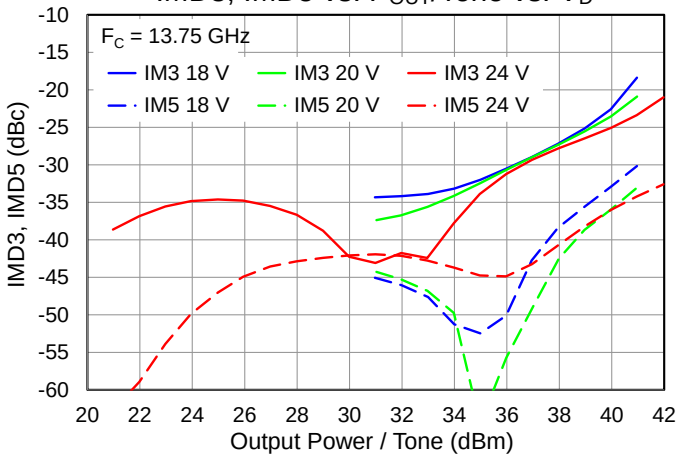
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



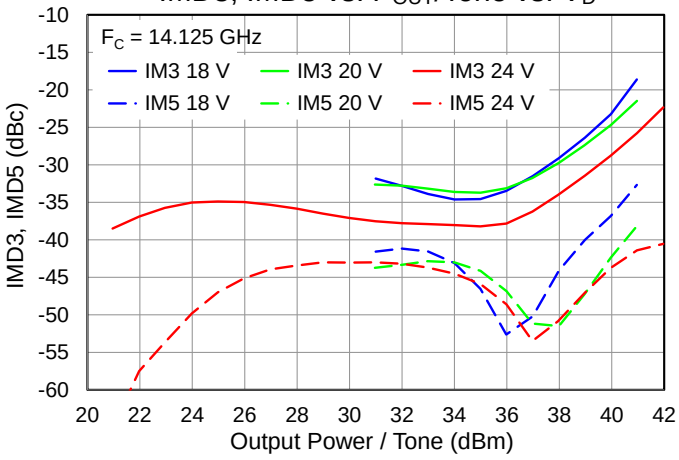
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



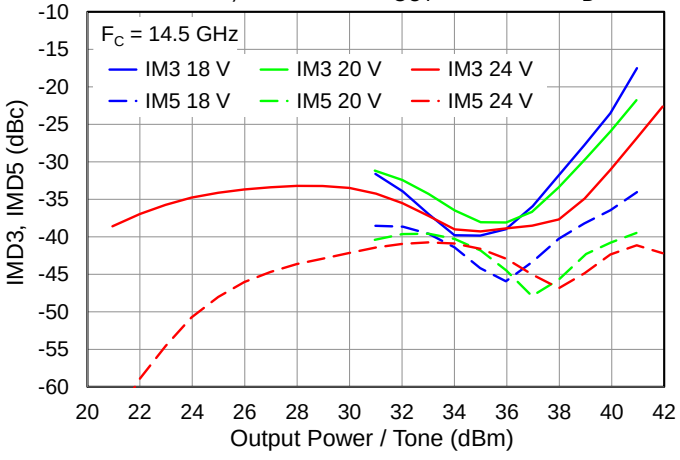
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



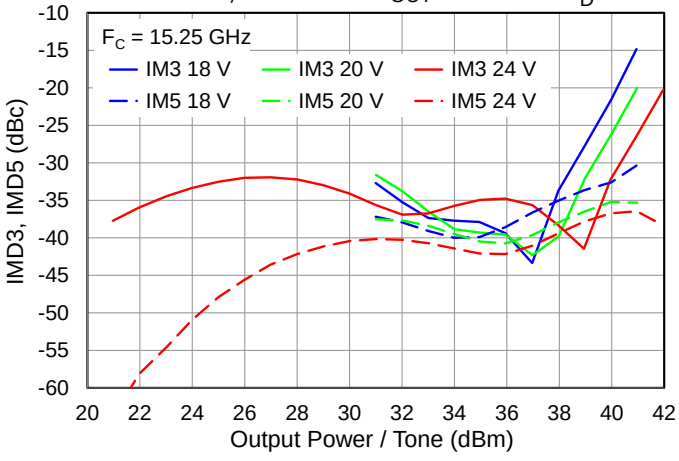
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D

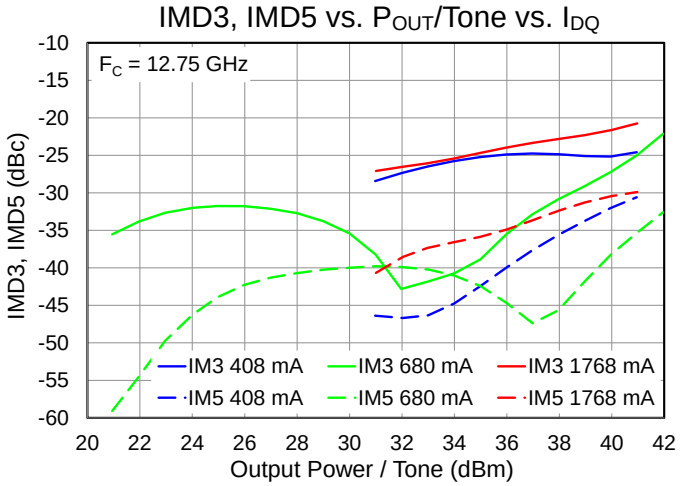


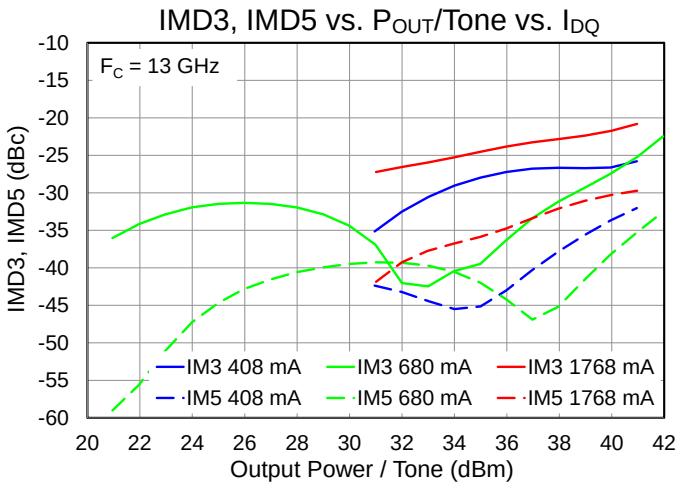
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D

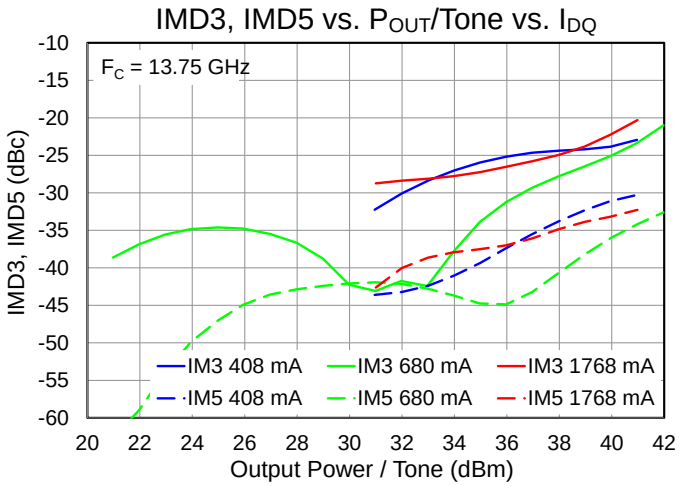


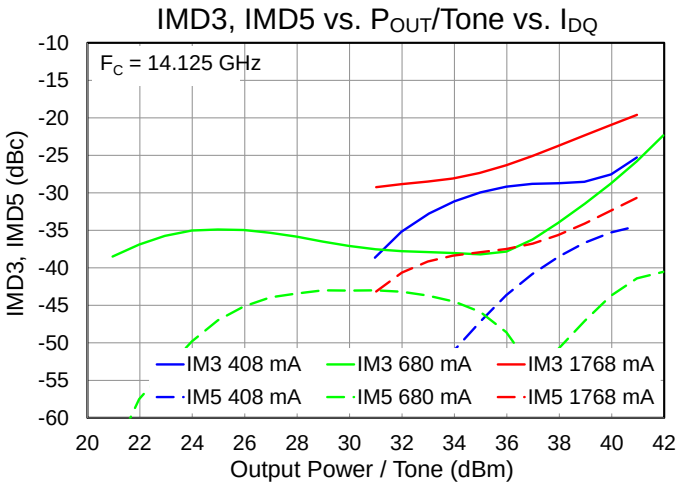
Performance Plots – Linearity (CW)

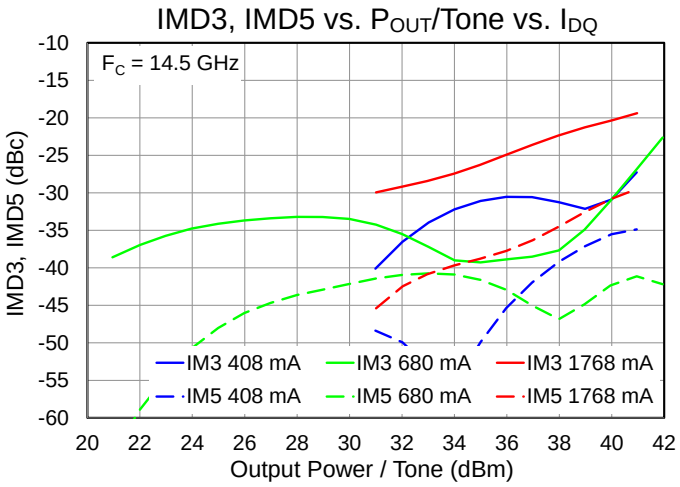
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, Tone Spacing = 20 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

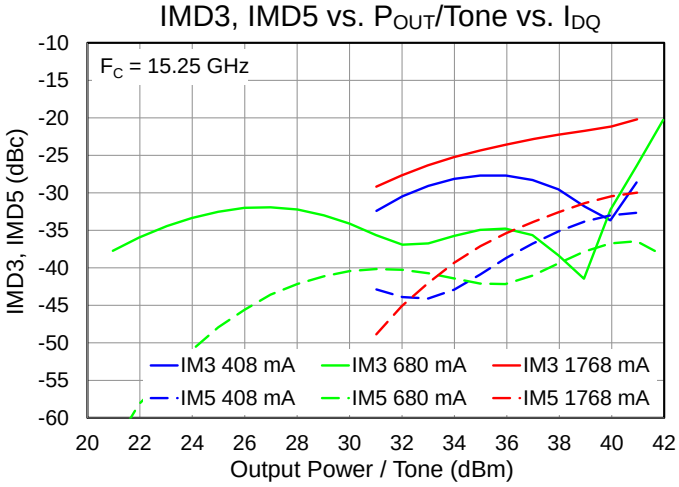








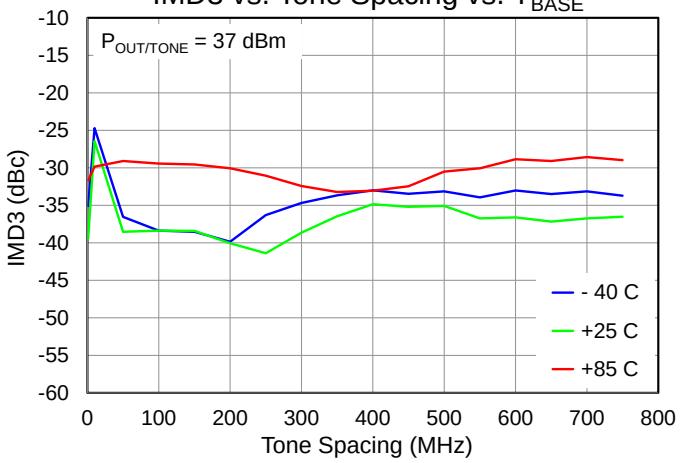




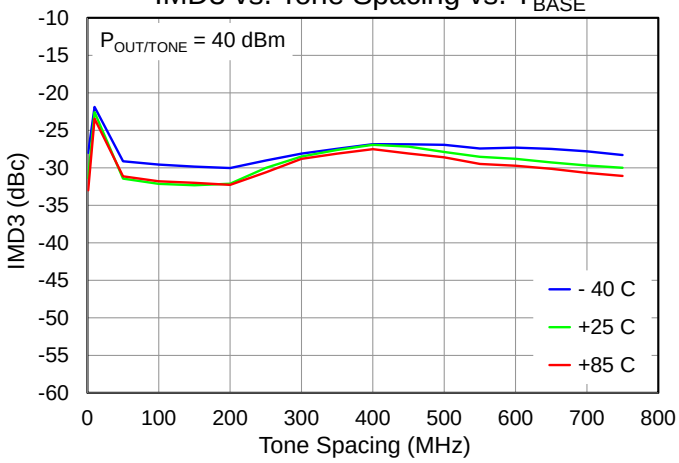
Performance Plots – Linearity (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

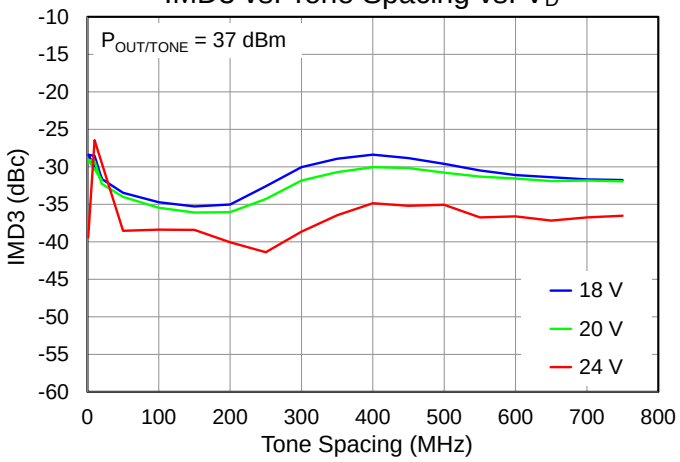
IMD3 vs. Tone Spacing vs. T_{BASE}



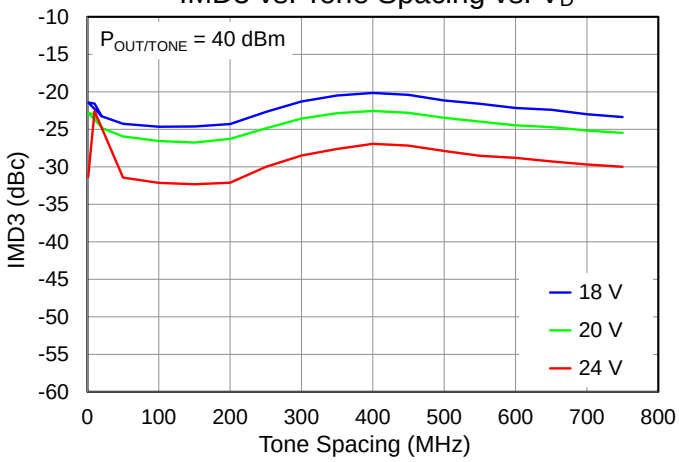
IMD3 vs. Tone Spacing vs. T_{BASE}



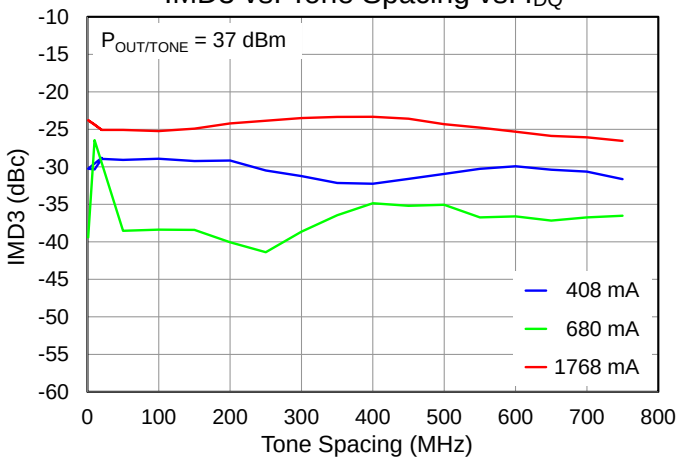
IMD3 vs. Tone Spacing vs. V_D



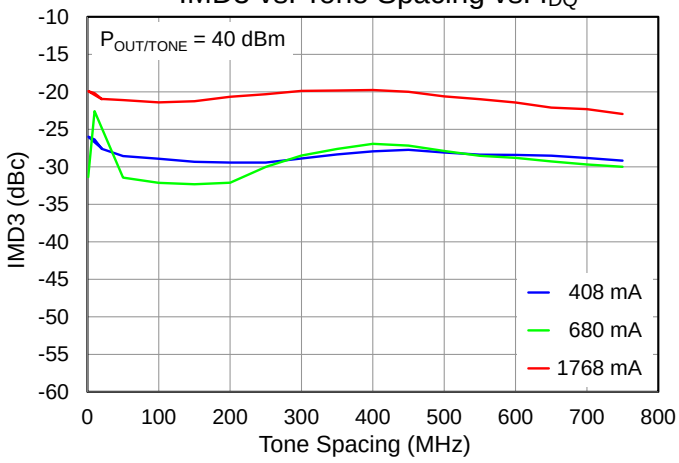
IMD3 vs. Tone Spacing vs. V_D



IMD3 vs. Tone Spacing vs. I_{DQ}



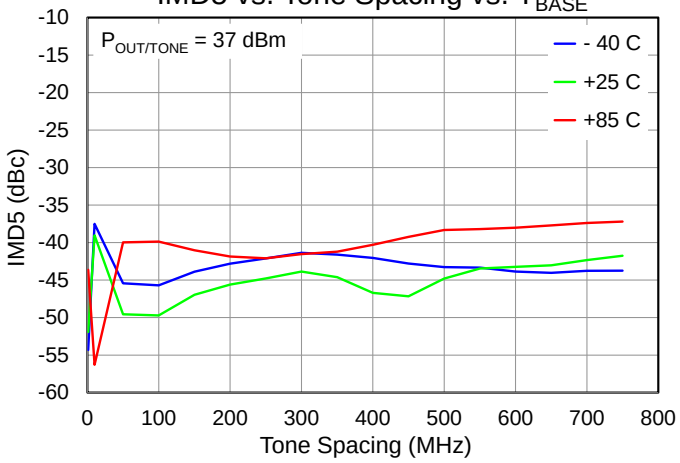
IMD3 vs. Tone Spacing vs. I_{DQ}



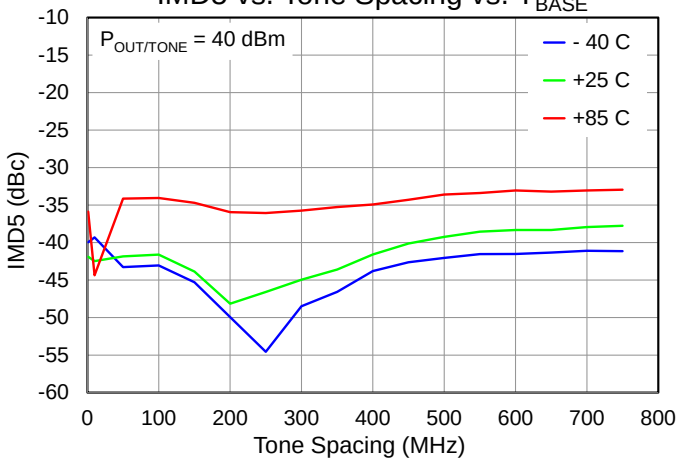
Performance Plots – Linearity (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

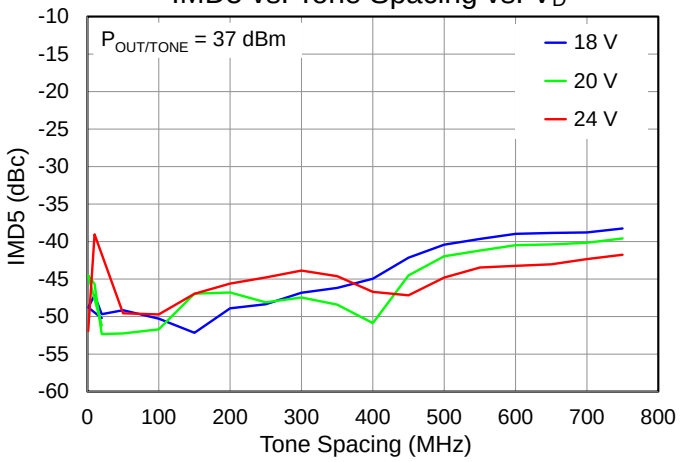
IMD5 vs. Tone Spacing vs. T_{BASE}



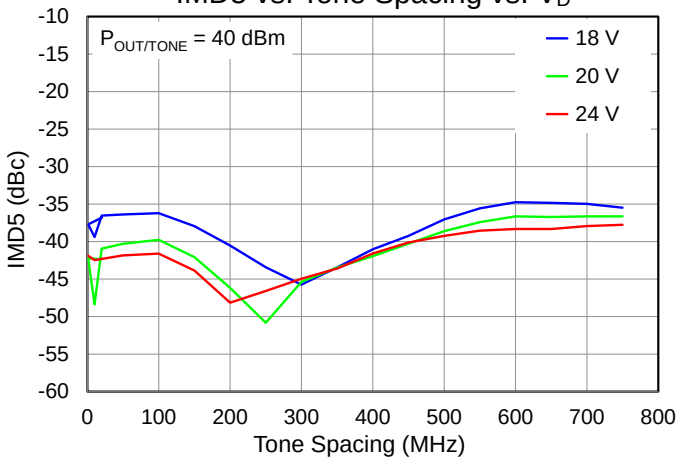
IMD5 vs. Tone Spacing vs. T_{BASE}



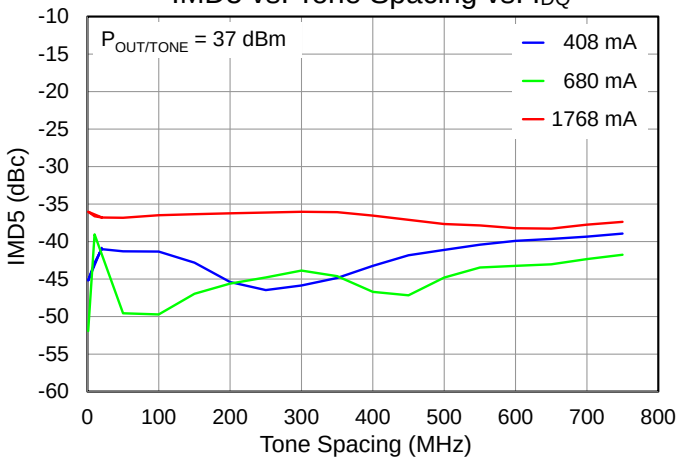
IMD5 vs. Tone Spacing vs. V_D



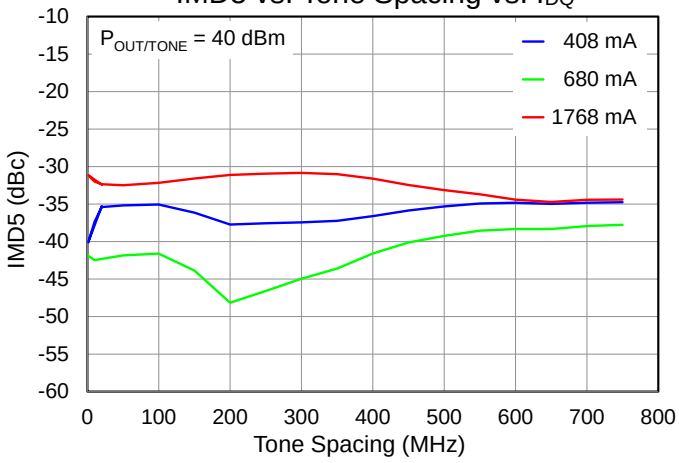
IMD5 vs. Tone Spacing vs. V_D



IMD5 vs. Tone Spacing vs. I_{DQ}



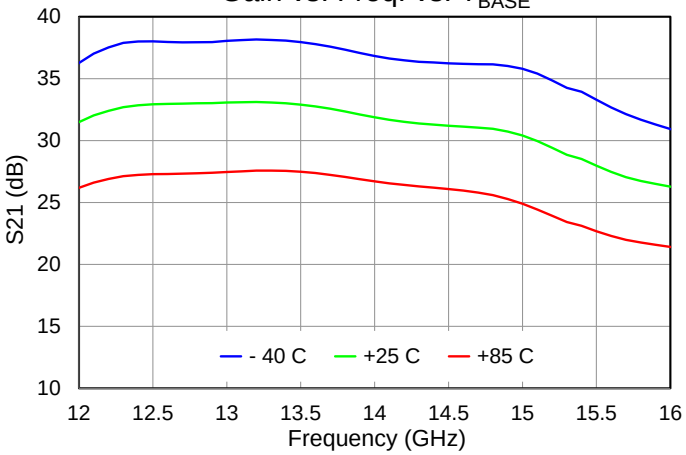
IMD5 vs. Tone Spacing vs. I_{DQ}



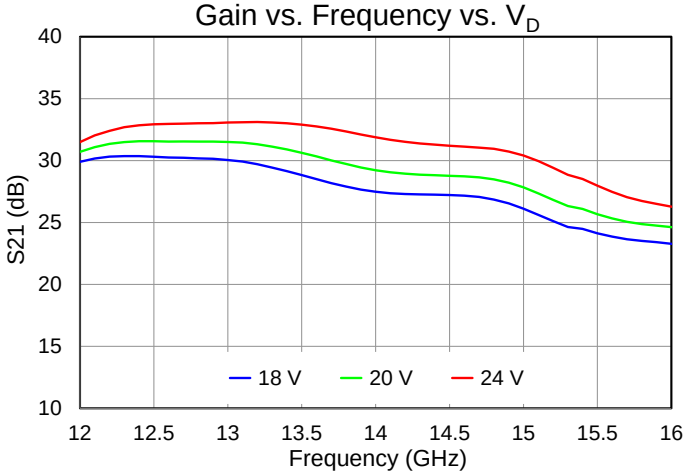
Performance Plots – Small Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).

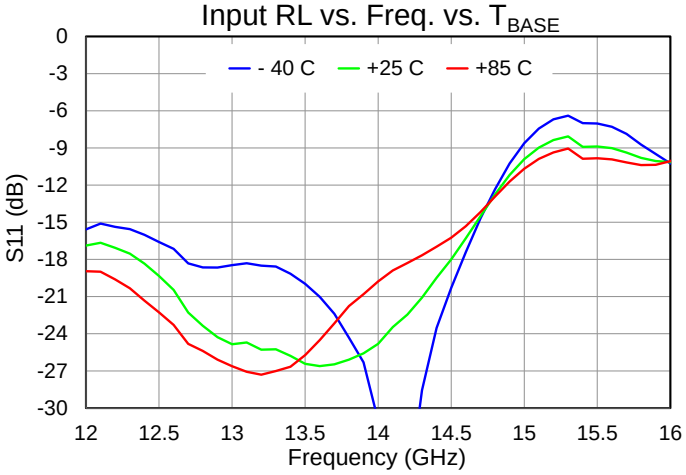
Gain vs. Freq. vs. T_{BASE}



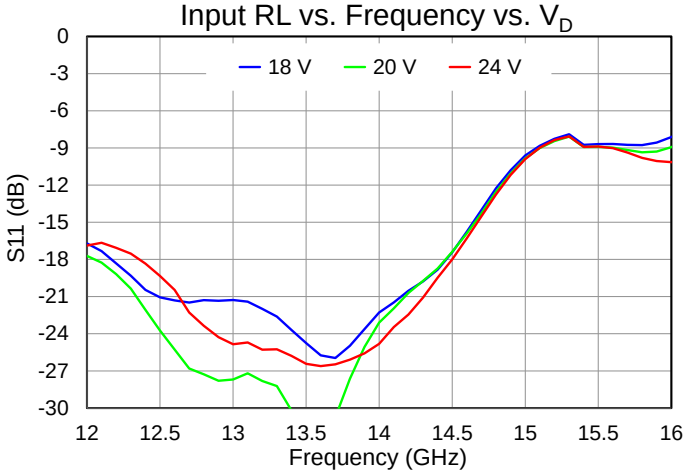
Gain vs. Frequency vs. V_D



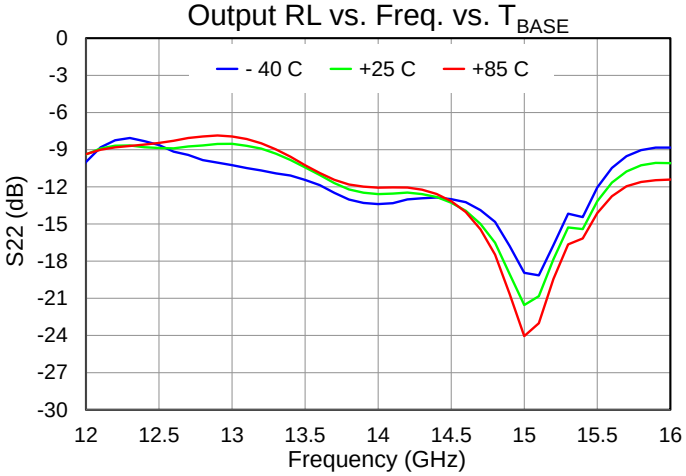
Input RL vs. Freq. vs. T_{BASE}



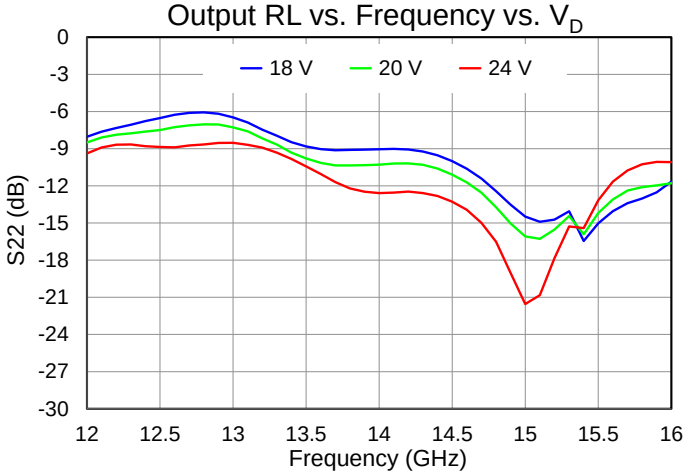
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. T_{BASE}

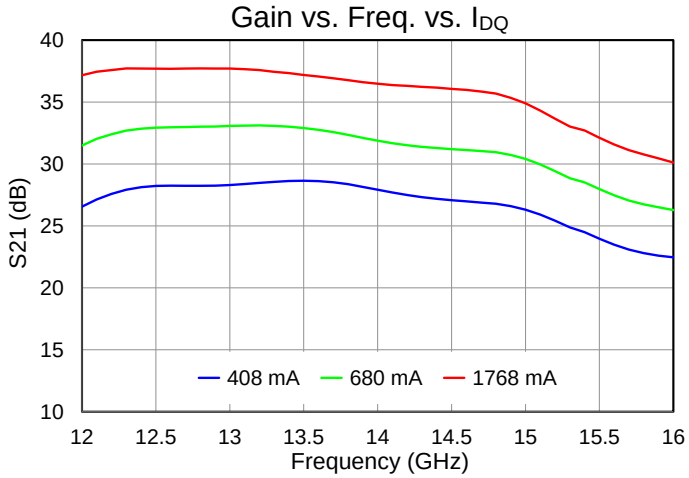


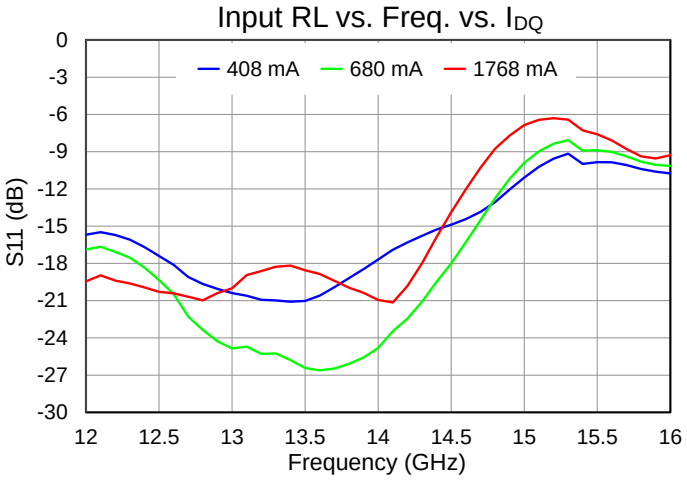
Output RL vs. Frequency vs. V_D

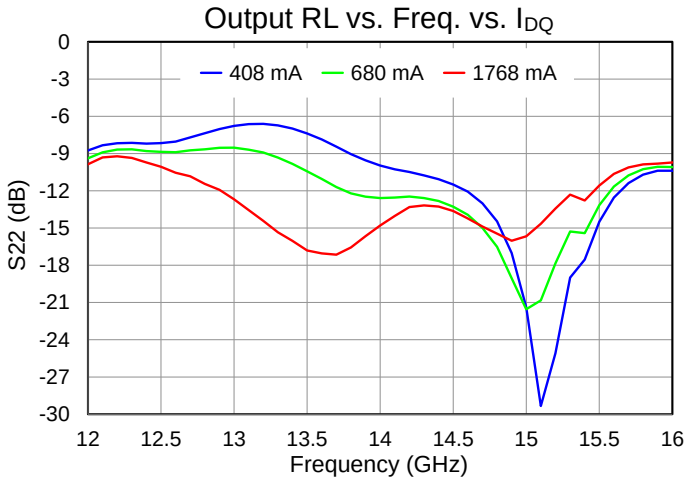


Performance Plots – Small Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 680 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1314).







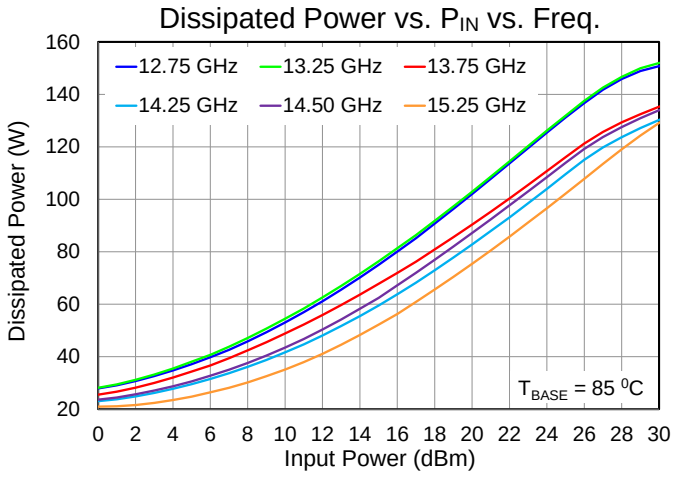
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC}	Quiescent, no RF T_{BASE} = 85 °C, V_D = 24 V, I_{DQ} = 680 mA P_{DISS} = 16.32 W	0.73	ºC/W
Channel Temperature, T_{CH}		97	°C
Thermal Resistance, θ_{JC}	For 13.75 – 14.5 GHz: P_{IN} = 19 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{DQ} = 680mA, Freq = 14 GHz (frequency at highest P_{DISS}), I_{D_DRIVE} = 4.87 A, P_{OUT} = 44.5 dBm, P_{DISS} = 88.5 W	0.75	ºC/W
Channel Temperature, T_{CH}		151	°C
Thermal Resistance, θ_{JC}	For extended 12.75 – 15.35 GHz: P_{IN} = 19 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{DQ} = 680 mA , Freq = 13.25 GHz (frequency at highest P_{DISS}), I_{D_DRIVE} = 5.4 A, P_{OUT} = 45.1 dBm, P_{DISS} = 97.3 W	0.76	ºC/W
Channel Temperature, T_{CH}		159	°C

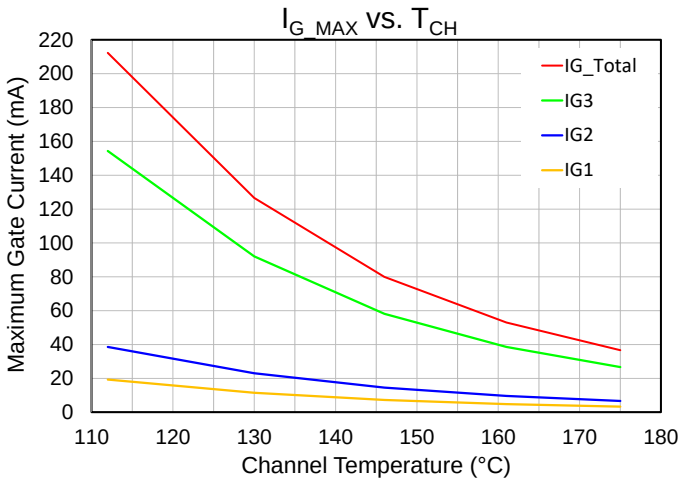
Notes:

1. Thermal resistance determined to T_{BASE} (T_{BASE} is backside of package QPA1314)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

Dissipated Power and Maximum Gate Current

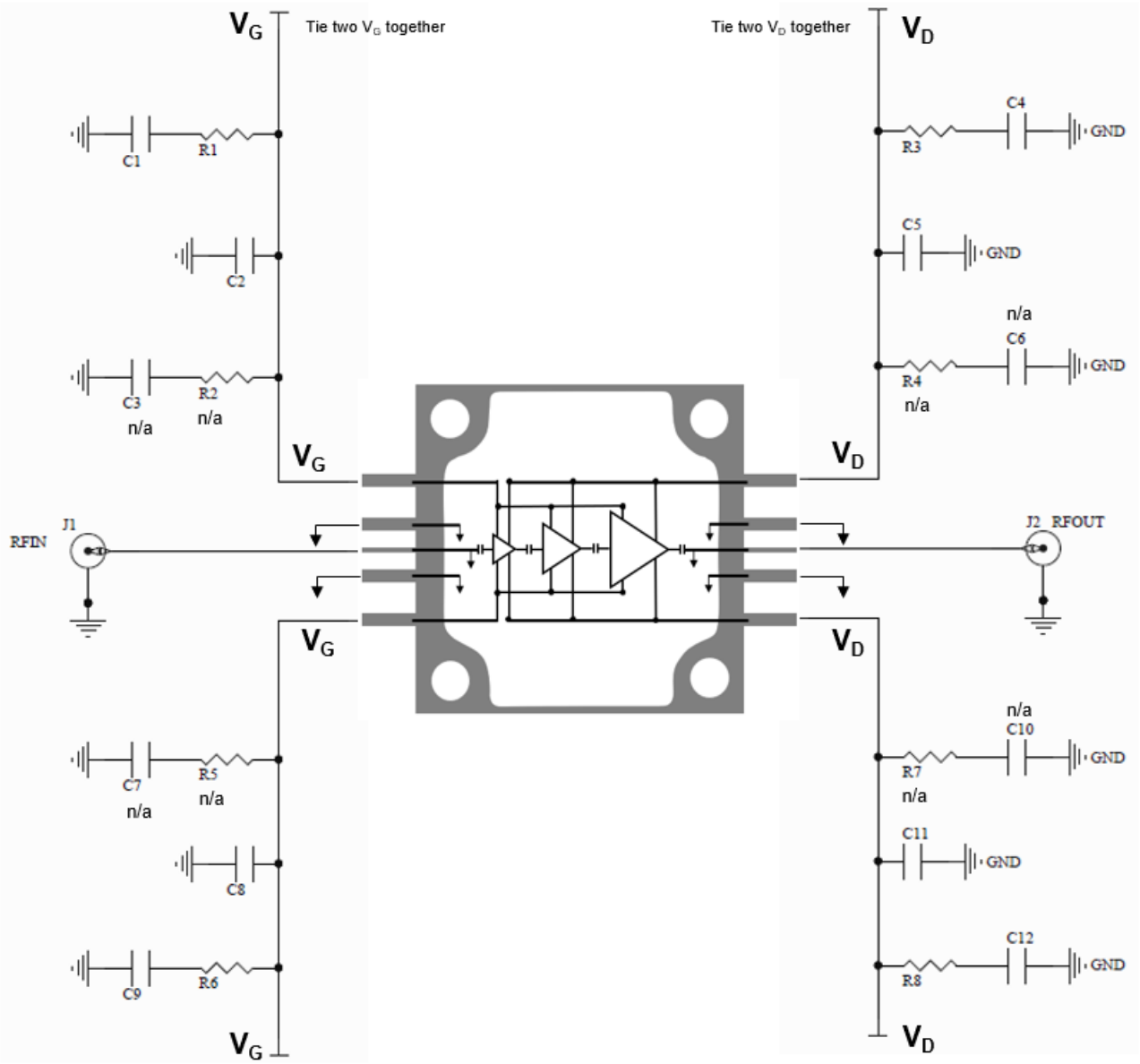


Test conditions: CW, V_D = 24 V, I_{DQ} = 680 mA, T_{BASE} = 85 ºC
T_{BASE} is back side of QPA1314



Channel Temperature is an IR scan equivalent

Applications Information



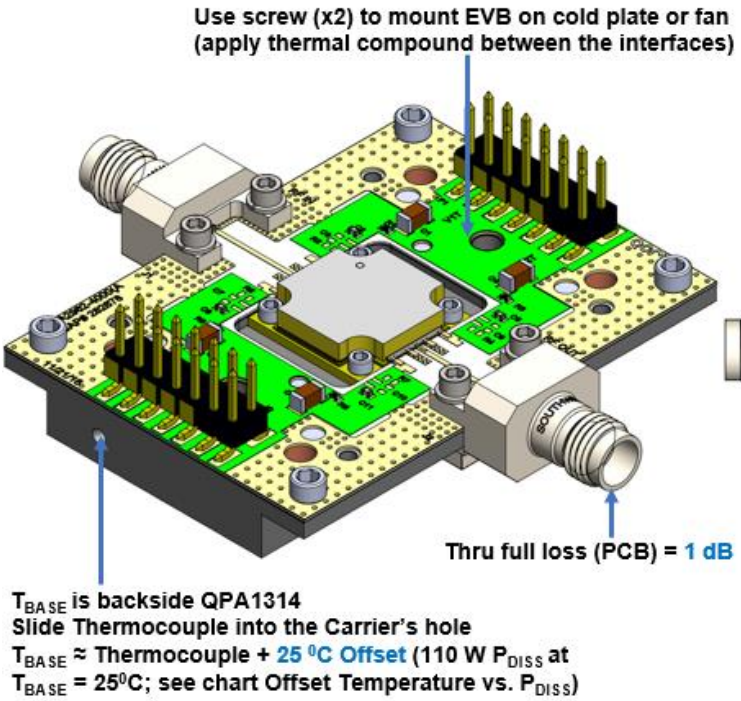
Bias-Up Procedure

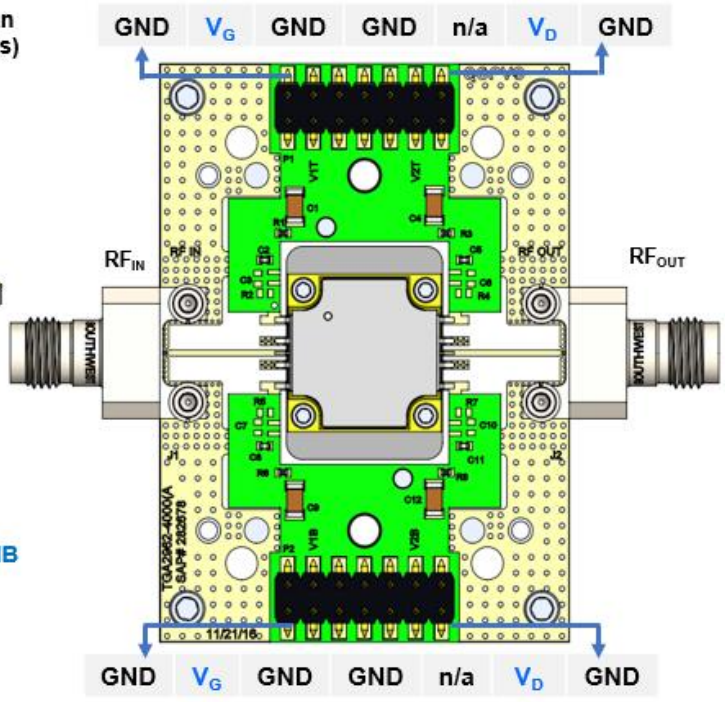
1. Set I_D limit to 10 A, I_G limit to 15 mA
2. Apply V_G to −5 V
3. Apply V_D to 24 V; ensure I_{DQ} ~ 0 mA
4. Adjust V_G more positive until I_{DQ} = 680 mA; $V_G \approx$ -2.3 +/-0.6 V typical range
5. Apply RF signal

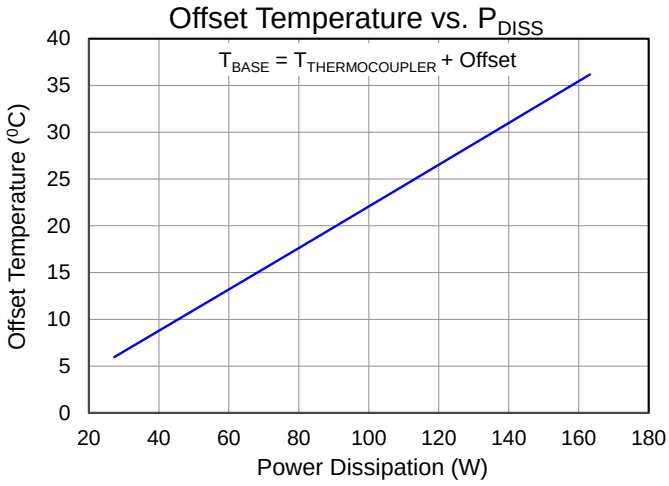
Bias-Down Procedure

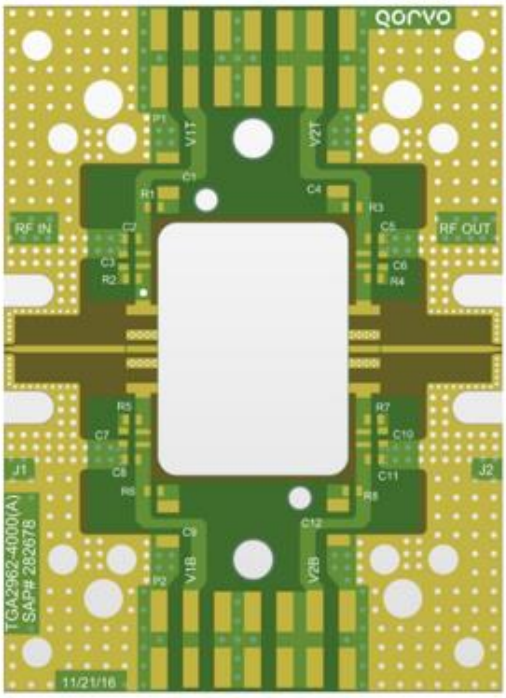
1. Turn off RF signal
2. Reduce V_G to −5 V; ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout









Layer Stack Legend (Copper Thickness is Finished Copper Thickness)

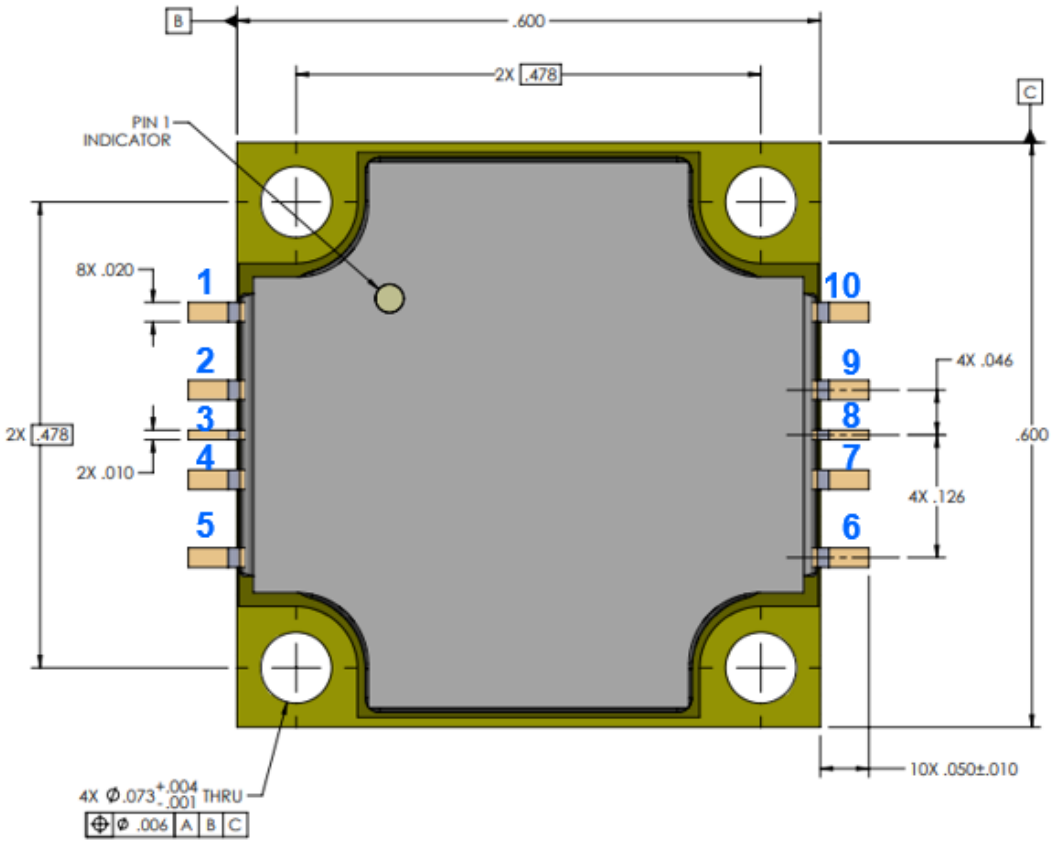
Material	Layer	Thickness	Dielectric Material	Type
	Silkscreen_Top			Legend
Surface Material	Soldermask_Top	0.10mil	Solder Resist	Solder Mask
Copper	Metal1_Top	1.40mil		Signal
Core		10.00mil	ROGERS 6035HTC	Dielectric
Copper	Metal2_Bot	1.40mil		Signal

Total thickness: 12.90mil

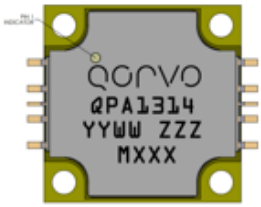
Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C4, C9, C12	4	10 uF	CAP, 10uF, ±20%, 50V, X5R, 1206	
C2, C5, C8, C11	4	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	
R1, R3, R6, R8	4	0.5 Ω	RES, 0.5 Ohm, ±1%, 1/8W, 0402	
PCB	1		PCB for QPA1314, see above	Qorvo, Custom
H1, H2	2		DC Header, 2x7, SMD	
J1, J2	2		RF Connector, SMA, Female	Southwest Microwave
H-Block	1		H-Block, Copper C110, 1.594 x 2.200 x 0.275 in	Qorvo, Custom
S1 – S4	4		Screw, Cap, Socket Head,0-80X3/32”	
S5 – S8	4		Screw, Cap, Socket Head, 2-56X1/8”	
Epoxy	-		Epoxy, preform, 5025E, 0.003” thickness	
Thermal Compound	-		Thermal Compound, Arctic Silver	
Solder	-		Solder, paste, Sn63Pb37	
Solder	-		Solder, wire, Sn96.5Ag3Cu.5, 0.020”	

Mechanical Information



NOTES:
1. MATERIALS
   LID: LAMINATE
   BASE: COPPER; FINISH: GOLD
   LEADS: ALLOY 194; FINISH: GOLD
2. PART IS EPOXY SEALED
3. UNITS: INCHES
4. TOLERANCES (UNLESS NOTED):
   .XX = ± .01
   .XXX = ± .005
   ANGLES = 0.5 °
5. MARKINGS
   QPA1314: PART NUMBER
   YY: ASSEMBLY YEAR
   WW: ASSEMBLY WEEK
   ZZZ: SERIAL NUMBER
   MXXX: BATCH ID



Pin Description

Pin Number	Symbol	Description
1, 5	V_G	Gate voltage (1). Must be biased on both pins
2, 4, 7, 9	Ground	Ground. Must be grounded on PCB
3	RF_{IN}	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
6, 10	V_D	Drain voltage (1). Must be biased on both pins
8	RF_{OUT}	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground

1. External bypassing required; refer to page 24 for recommendation.

Assembly Notes

1. Carefully clean the PC board, base plate, and package leads with alcohol. Allow it to dry fully.

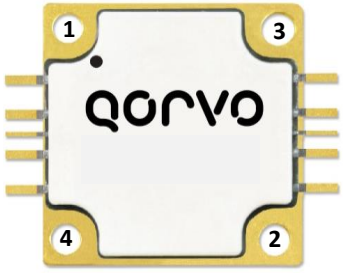
2. To improve the thermal and RF performance, Qorvo recommends attaching a heat sink to the bottom of the package and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch (maximum thickness) Indium shim between the heat sink and the package. Refer to the applications note Application of Arctic Silver 5 Thermal Compound and Indium Shims for Qorvo CP-style Packaged Components for more information.

3. The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the QPA1314. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. The package lead temperature should not exceed 260 deg C. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.

4. The leads should be soldered in a staggered or star pattern from side to side, and never solder two adjacent leads. This allows the heat to dissipate on each lead, and not cause the adjacent leads to become de-soldered and damaged or displaced.

5. The packaged part should not be subjected to conventional SMT automated solder reflow processes.

6. (The following is for information only. There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.) Use screws to attach the component to the heat sink. A suggested final torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value. Use the following tightening pattern:



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	N/A	

Caution!

ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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