USER'S GUIDE

ACT43950/43850/43750 EVK User's Guide

Description

The ACT43950 is a constant-current capacitor charger. The ACT43850 is a high-voltage and high-power buck regulator. The ACT43750 controls a drain switch and provides a negative voltage for an RF PA device. This three-chip combination forms a compact, complete power supply system for radio frequency (RF) power amplifiers (PAs) that demand fast transient, high-current, pulsed loads.

The three-chip combination can be evaluated with one, two, or three ICs on an EVK. These EVKs are referred to as Combo Boards or CB. This document describes the characteristics and operation of Qorvo's three-chip ACT43950/43850/43750 Combo Board. It also describes how to use the Combo Board when it is separated into smaller boards. It provides setup and operation instructions, schematic, layout, BOM, GUI, and test data. Refer to the section of this document that matches the EVK you are testing.

ACT43X50PCKCB1: This Combo Board contains the ACT43750, ACT43850, and ACT43950 ICs.

ACT43X950PCKCB1: This Combo Board contains ACT43950 ICs.

ACT43850PCKCB1: This Combo Board contains the ACT43750 and ACT43850 ICs.

Functions

The first stage ACT43950 accepts a DC input voltage up to 400V and converts it into a regulated DC constant current to charge bulk capacitors. The second stage ACT43850 takes up to 150V DC input to generate programmable output voltage from 20V to 65V at up to 20A. The last stage is the ACT43750 which has two main functions. The first is to provide proper turn on sequencing for RFPAs. The second is to control pulsed drain voltage switching for the RFPA.

Qorvo recommends that the user connect EVK to a PC and use the graphical user interface (GUI) software. The GUI allows the user to enable/disable devices and program the exact voltage and current for the specific RF PA being tested. AC43950 does not have registers but can be enabled/disabled by a GPIO from the Dongle when using the ACT43850 GUI. The ACT43850 GUI gives the user full control over the drain voltage, protection features, and gate voltage. The user can use the ACT43750 GUI to set the Idq bias current requirement, and the design autonomously finds and stores the optimal gate voltage for the Idq bias current. After the optimal gate bias voltage is found, the user can then apply an RF signal to test the RF PA functionality.

EVK Contents

The EVK contents vary depending on the configuration shipped.

Figure 1 shows the ACT43X50PCKCB1. The board you are testing will be this full PCB or a subset of this PCB.

The board you are testing should be shipped pre-configured for the user's requirements. If the user modifies the board, Qorvo recommends they separate the boards and test each section individually before recombining them to perform system-level testing.

Skip to the User's Guide section that matches the board you are testing. This document contains instructions to setup and test the following combinations.

APPENDIX

Application Note 2: How to Configure Bias Current and Current Limit

Application Note 3: How to Configure Drain Switching Time

Application Note 4: Drain Capacitance for RFPA Drain Switching Operation

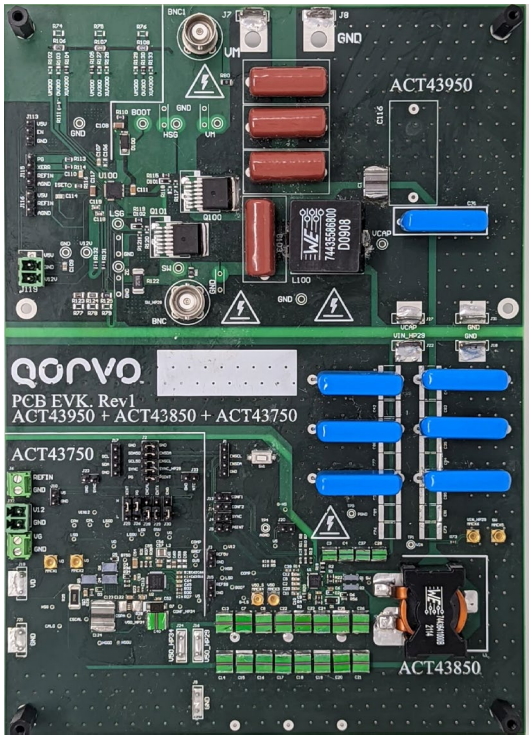


Figure 1. ACT43X50PCKCB1 Combined Board

ACT43950PCKCB1 - ACT43950 Standalone Combo Board Overview

This board may be shipped as a standalone board (cut out portion) from the 3-chip Combo Board, or it may be shipped as a full 3-chip Combo Board with the ACT43950 section disconnected from the rest of the PCB. The ACT43950 converts 320V dc input to the programmable constant current to charge the output capacitor. The full charge voltage is set to 135V. The IC starts the refresh charging when the output voltage drops below 125V. During normal operation in the 3-chip Combo Board configuration, the output voltage typically drops to ~80V during the high current pulse to the RFPA, then charges back up to 135V before the next pulse starts.

Required Equipment

- ACT43950PCKCB1
- DC power supply - 180~400V @ 5A for full power operation
- DC power supply – 12V@ 1A
- Oscilloscope - 100MHz, 4 channels
- High voltage probe (>300V)
- Digital Multi-meters (>300V) for input voltage and DMM (<300V) for VCAP

- Windows compatible PC with spare USB port
- Qorvo I²C USB cable

Hardware Setup

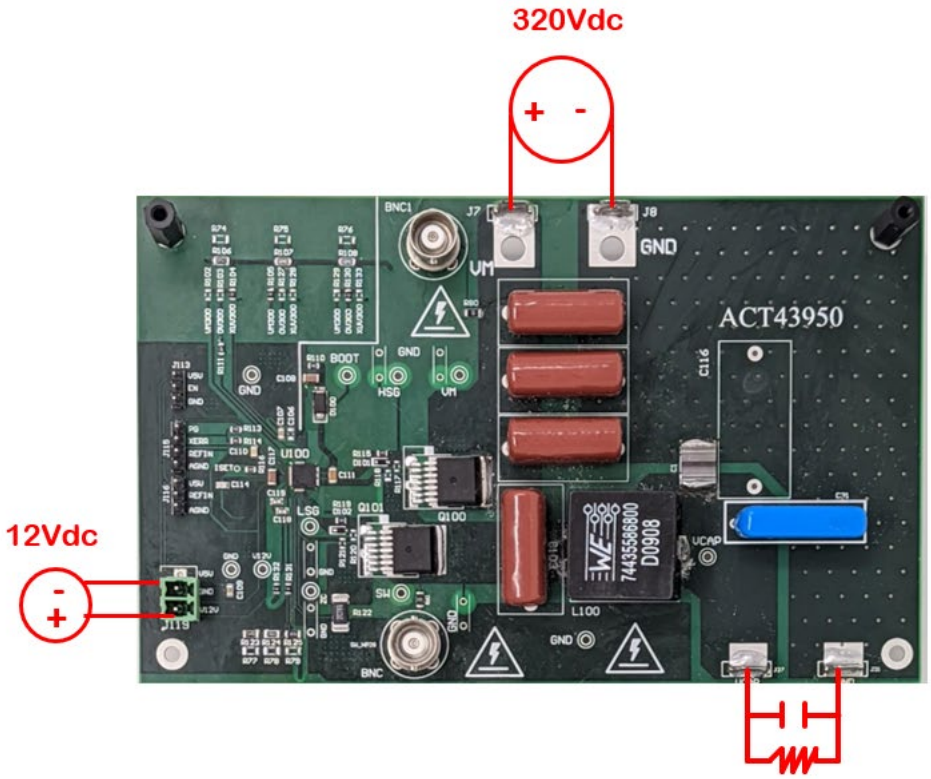


Figure 2. ACT43950PCKCB1 Setup

Quick Start

Hardware Connections

Refer to Figure 2 for hardware connections.

1. Make all connections with power off.
2. Separate the ACT43950 part of the PCB from the ACT43850 part of the PCB.
    a. If installed, remove the jumpers between J27 (VCAP) and J22 (VIN_HP29)
    b. If installed, remove the jumpers between J31 (GND) and J18 (GND)
3. Connect a 320VDC power supply to connector J7 (VM) and J8 (GND). Please ensure the correct power supply polarity.
4. The user may add additional optional aluminum capacitors at the J7 to J8 input to help average the 320V supply current
5. Connect a 12VDC supply between V12V and GND at J119.
6. If the PCB is shipped as the full PCB (all three ICs), the user can use the GUI to enable and disable the ACT43950. Connect the USB-TO-I2C Dongle cable from the Qorvo USB- I²C dongle to J17. The black wire connects to the GND pin. The dongle controls the ACT43950 using the unlabeled GPIO pin on the connector.

    Note: J17 is located on the PCB in the ACT43750 board area.
7. If the PCB is shipped with only the ACT43950 IC, the user must use the EN pin on J113 to enable and disable the ACT43950.
8. (Optional) connect an extra Resistor load and Capacitor as needed between J27 and J31
9. Connect Digital Multi-Meters to VM and VCAP to monitor the input voltage and output capacitor voltages.
10. Add a digital Multi-Meter in series with the VM input wire and the VCAP output wire if you want to observe input and output current.
11. Be careful to keep the input voltages within the specifications.

Figure 3. USB-TO-I2C PCB Connection Location

ACT43950 Standalone Test GUI Operation

GUI Setup

1. Refer to the end of this document for detailed instructions to install the ACT43750 GUI.

Note: ACT43950 doesn't have an I²C function. The ACT43750 GUI controls the dongle GPIO to enable the ACT43950. The ACT43950 can also be enabled and disabled using its EN pin.

GUI Operation

In the ACT43750 GUI. Refer to Figure 4 for GUI interface.

1. Select Tool, this is to access the GPIO, not I2C function.

Enable

2. Before turning ON the DC supplies, Refer to figure 4
   Click on "ID0 = LOW" in the "Set GPIO" box. This sets the I2C-TO-GPIO dongle GPIO output to a logic level low to disable the ACT43950. When the GPIO is low, the "ID0 = LOW" box is grayed out.

3. After all supplies are turned on and the user is ready to enable the ACT43950
   Click on "ID0 = HIGH" in the "Set GPIO" box. This sets the I2C-TO-GPIO dongle GPIO output to a logic level high to enable the ACT43950. When the GPIO is high, the "ID0 = HIGH" box is grayed out.

Disable

4. Click on "ID0 = LOW" in the "Set GPIO" box

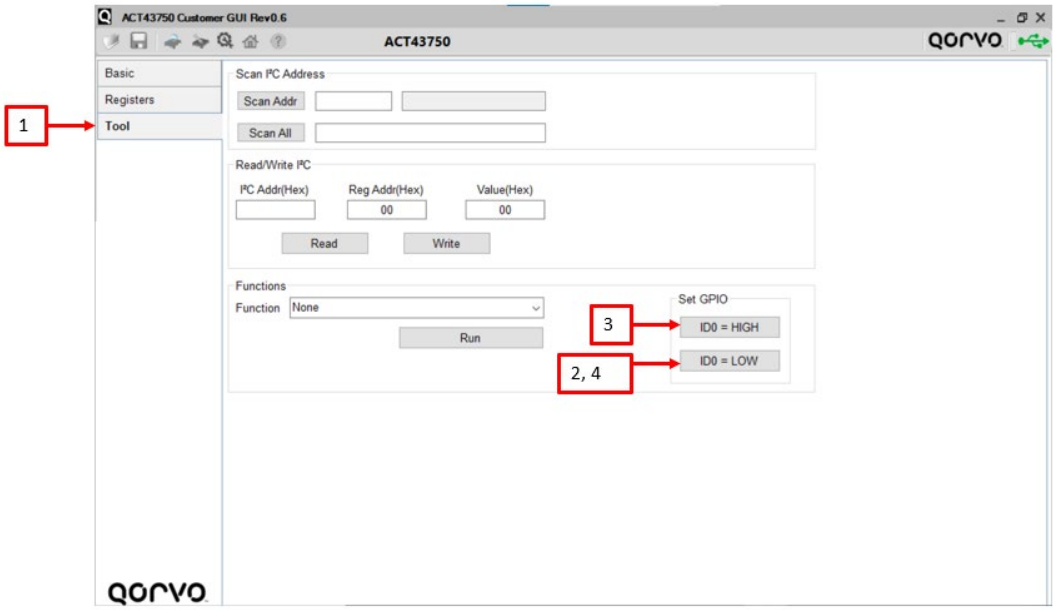


Figure 4. ACT43750 GUI interface to set GPIO

Recommended Operating Conditions

The ACT43950 is designed for a 180V-400V input voltage. The maximum operating voltage is determined by the IC's maximum input voltage rating of 400V. The minimum operating voltage is determined by the IC's output voltage setting. See the ACT43950 datasheet for details on modifying this output voltage. The maximum charge current is configured by external components. The default hardware design is rated at 4A. The customer can easily reconfigure the EVK for different output voltages and currents after referring to the datasheet for the required component changes.

Table 1. Recommended Operating Conditions for ACT43950

Parameter	Description	Min	Typ	Max	Unit
VIN	Input voltage	180	-	400	V
VCAP	Output capacitor voltage	125	130	140	V
Icharge	Charge current	1	-	4	A
V12V	12V dc bias voltage	10.8	12	13.2	V

ACT43950 Standalone Test Probing

Use DMM meter (>300V) to measure input and DMM meter (<300V) to measure VCAP at the available test points

Use high voltage probes (>300V) to measure input voltage and switching node voltage waveforms at BNC or test points.

Use a current probe to measure the inductor current waveforms.

Use voltage probe to measure VCAP waveforms at test pins

ACT43950 Standalone Test Procedure

Power up

Warning:

- Devices may be damaged if the power up/power down procedure are not strictly followed.
- Don't touch the high voltage potentials: input & output voltage terminals, test points, capacitors, and inductors.

1. Make sure the ACT43950 is disabled.
   - Using GUI to enable or disable the ACT43950, confirm that ID0 = LOW to disable the ACT43950. Make sure J113 does not have a shorting jumper installed.

   Note: Read/write function doesn't work for the GPIO function. Measure EN pin voltage to confirm enable or disable.
2. Power on the12V bias supply
   - The waveform at the SW test point should not be switching, and the 12V current should be ~1mA.
3. Power on 320V supply

- The waveform at SW should still not be switching and the 320V current should be <1mA.

4. Enable the ACT43950
   - Using the GUI, click on the ID0 = HIGH button.
5. ACT43950 should be enabled.
6. Compare the operating waveforms to those below to confirm proper operation.

Power down

1. Using the GUI, click on the ID0 = LOW button to disable the ACT43950. Refer to figure 4 for the detail
   - ACT43950 should be disabled and not switching
2. For safety, let the VCAP output voltage decay below 30V before touching the probes connected to the PCB or handling the PCB.
3. Power off 320V
   - VCAP should be lower than 30V before turning off the 320V supply.
4. Power off 12V bias

ACT43950 is standalone board, which is separated from combo board

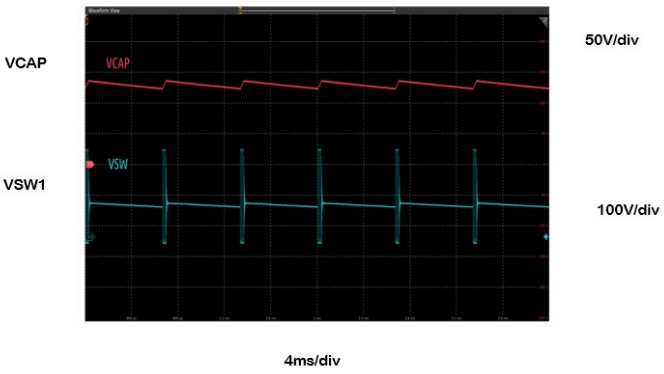
Power up and power down are the same as above description except using EN pin.

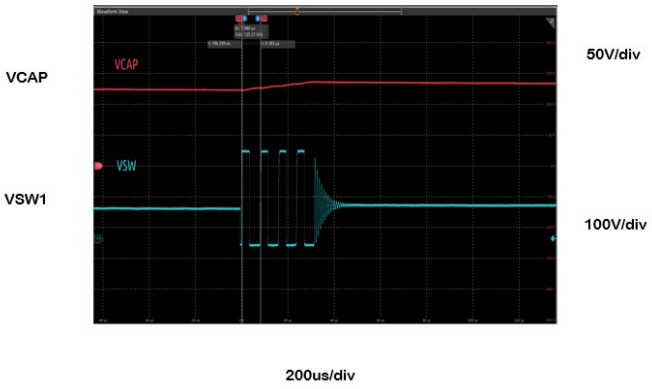
ACT43950 can be enabled or disabled by EN pin at J113. No GUI is available because there is no GPIO port.

There is an internal pull-up resistor at EN pin. Opening EN pin is to enable ACT43950. Shorting EN pin to ground is to disable ACT4395. The details of enable pin function can refer to the datasheet.

Test Results

Test condition, Input voltage=320V, output voltage=124V, load=600 ohm





ACT43850 Standalone Combo Board Overview

The ACT43850 converts a 150VDC input to the programmable output voltage of 20V to 55V. The output current is up to 20A. The ACT43850 stores its programming setpoints in on-board non-volatile memory (NVM) memory cells. The default values are loaded into working memory at startup, but can be modified through an I²C interface on-the-fly by Qorvo's GUI.

Required Equipment

- ACT43850
- DC power supply - 70~145V @ 20A for full power operation
- DC power supply – 12V@ 1A
- Oscilloscope - 100MHz, 4 channels
- Digital Multi-meters (DMM)
- Windows compatible PC with spare USB port
- Qorvo I²C USB cable

Hardware Setup

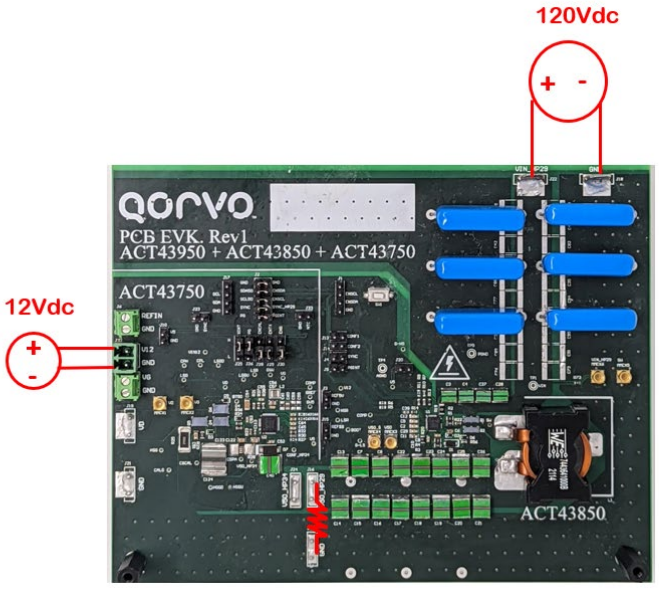


Figure 5. ACT43850 Setup (always shipped with ACT43750 circuitry)

Quick Start

Hardware Connections

Refer to Figure 5 for hardware connections.

1. Make all connections with power off.
2. Separate the ACT43850 part of the PCB from the ACT43950 part of the PCB.
    a. If installed, remove the jumpers between J27 (VCAP) and J22 (VIN_HP29)
    b. If installed, remove the jumpers between J31 (GND) and J18 (GND)
3. Separate the ACT43850 part of the PCB from the ACT43750 part of the PCB.
    a. If installed, remove the jumpers between J16 (V50_HP29) and J24 (V50_HP34)
4. Remove all the shorting jumpers at the J2 connector
5. Connect a 120V DC power supply between J22 (VIN_HP29) and J18 (GND)
    - Add additional capacitors between J22 & J18 when running heavy load transients without the ACT43950 being used as the input supply.
6. Connect a 12VDC power supply between V12 and GND at J32.
7. Connect the USB-TO-I2C Dongle cable from the Qorvo USB- I^2C dongle to J1. The black wire connects to the GND pin.
8. (Optional) connect dummy resistor load, as needed, between J16 and J9
9. (Optional) connect an RF PA between J16 and J9. Ensure the RF input to the RF PA is disabled.

ACT43850 Standalone Test GUI Operation

GUI Setup

Refer to the end of this document for detailed instructions to install the ACT43850 GUI and Figure 6 for GUI interface.

GUI Operation

1. Select Regulator
2. Click on the "Read" icon and confirm the GUI returns "Success"

Steps to Enable the ACT43850

3. Click Setting
4. Select "Enable" from Enable REG50
5. Click on the "Write" icon and confirm the GUI returns "Success"

Steps to Disable the ACT43850

6. Select "Disable" from Enable REG50,
7. Click on the "Write" icon and confirm the GUI returns "Success"

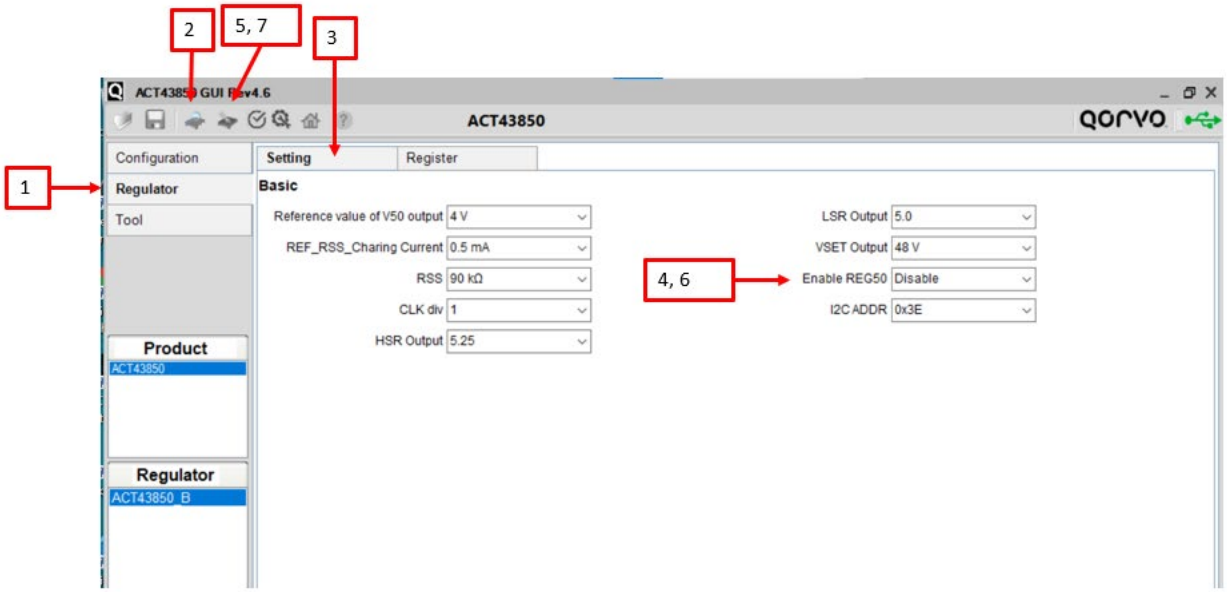


Figure 6. ACT43850EVK GUI

Recommended Operating Conditions

The ACT43850 is designed for up to 150V input voltage. The maximum operating voltage is determined by the IC's maximum input voltage rating of 150V. The default ACT43850 output voltage is 48V, so the design should be operated with Vin greater than 80V by default. See ACT43850 datasheet for details on modifying this output voltage. The maximum output current is 20A. The switching frequency is set to 500kHz to optimize efficiency. The customer can easily reconfigure the EVK for different switching frequencies and output voltages after referring to the datasheet for the required component changes.

Table 2. Recommended Operating Conditions for ACT43850

Parameter	Description	Min	Typ	Max	Unit
VIN	Input voltage	See note1	-	150	V
Vdrain	Drain voltage	20	48	55	V
Idrain	Drain current	0	-	20	A
Frequency	Switching frequency	450	500	900	kHz
V12V	12V DC bias	10.8	12	13.2	V

Note1, Minimum input voltage requirement can be found in ACT43850 datasheet Figure 60 to Figure 63.

ACT43850 Standalone Test Probing

Use DMM meter to measure input and output voltages at test points

Use a voltage probe with to measure input voltage, switching node voltage waveforms at the test points.

Use current probe to measure the inductor current waveforms if desired. This requires lifting the output voltage side of the inductor.

ACT43850 Standalone Test Procedure

Warning:

- Devices may be damaged if the power up/power down procedure are not strictly followed.
- Don't touch the high voltage potentials: input & output voltage terminals, test points, capacitors, and inductor.

Power up

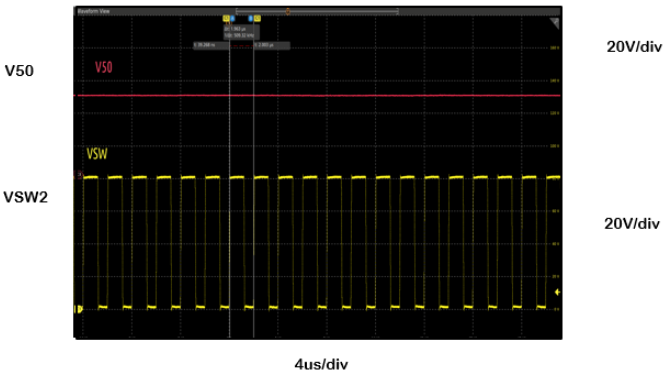
1. Power on the 12V bias supply.
    a. The waveform at the SW test point should not be switching and the 12V current is about 5mA.
2. Power on the 120V supply
    a. The waveform at SW test point should still not be switching and the 120V current should be about 0mA.
3. Enable the ACT43850
    a. Using GUI, click "setting".
    b. Select the output voltage from "Vset output" pull-down menu, then click the "write" icon.
    c. Click "Enable REG50" button to select "enable". Then click on the "write" icon to enable the ACT43850. Refer to figure 6
4. ACT43850 should be enabled. Check the output voltage.
5. Compare the operating waveforms to those below to confirm proper operation.

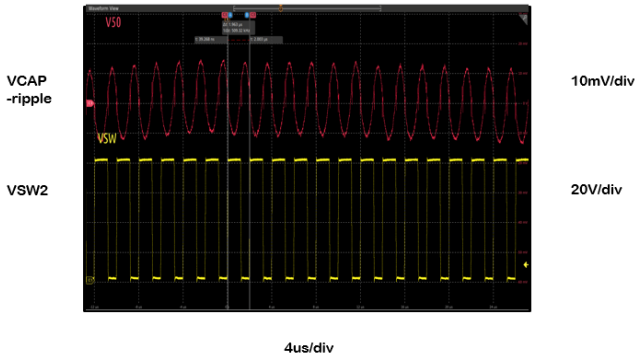
Power down

1. Disable the ACT43850
    a. Using the GUI, click on "disable " from "Enable REG50". Then click on the "write" icon to disable the ACT43850. Refer to Figure 6.
2. ACT43850 should be disabled and not switching.
3. Power off 120V DC power supply. Note that the 120V DC supply must be turned off before the 12V bias supply.
4. Power off 12V bias power supply.

Test Results

Test condition, Input voltage=80V, output voltage=48V, load=300 ohm





ACT43850PCKCB1 - ACT43750 and ACT43850 Combo Board Overview

This board may be shipped as a full 3-chip Combo Board or it may be shipped with the ACT43750 and ACT43850 sections disconnected (cut out) from the rest of the PCB. The ACT43850 converts a 150VDC input to the programmable output voltage of 20V to 55V. The output current is up to 20A. The ACT43850 stores its programming setpoints in on-board non-volatile memory (NVM) memory cells. The default values are loaded into working memory at startup but can be modified through an I2C interface on the fly by Qorvo's GUI.

The ACT43750 provides the negative voltage to drive a GaN FET RF PA, and it provides the proper turn on sequencing between the gate and drain voltages. When Vg is commanded to turn on, it starts at -4.5V and then steps higher to find the RF PA's Idq target. The ACT43750 also provides a fast switching circuit to enable RF PA drain switching. The ACT43750 does not generate the Vd drain voltage but only passes it through from the ACT43850 to the RF PA. The Vd output voltage can be turned on and off by a hardware enable input, or by a PWM signal.

The ACT43750 portion of the board is not intended to be operated separately from the ACT43850 section. Qorvo recommends testing the ACT43750 and ACT43850 together to take advantage of the built-in sequencing and protection circuitry between the two ICs.

Required Equipment

- ACT43850PCKCB1
- DC power supply - 70~145V @ 20A for full power operation
- DC power supply – 0-12V@ 1A
- Oscilloscope - 100MHz, 4 channels
- Digital Multimeters (DMM)
- Windows compatible PC with a spare USB port
- Qorvo I^2C USB cable

Hardware Setup

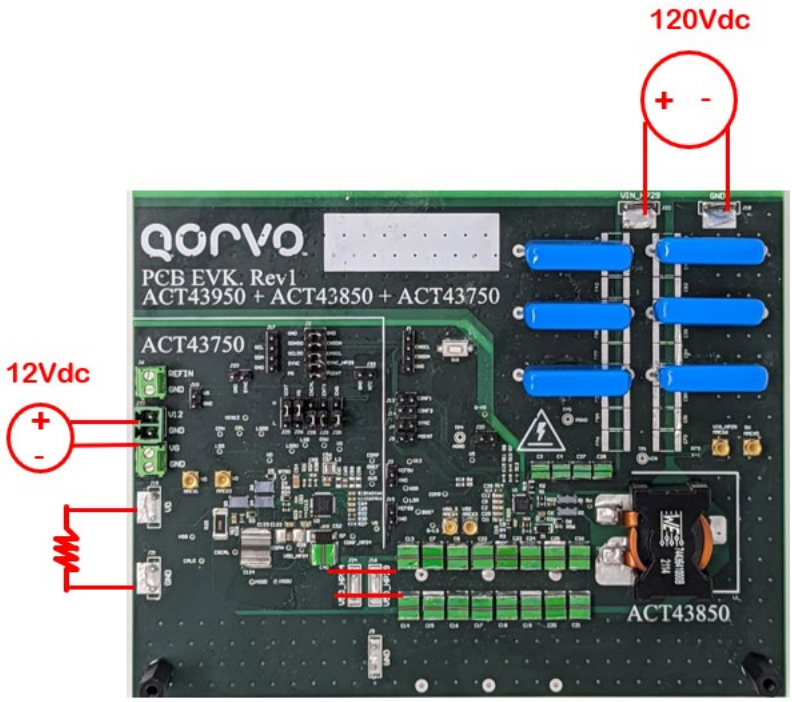


Figure 7. ACT43850PCKCB1

Quick Start

Hardware Connections

Refer to Figure 7 for hardware connections.

1. Make all connections with power off.
2. Separate the ACT43850 part of the PCB from the ACT43950 part of the PCB.
    a. If installed, remove the jumpers between J27 (VCAP) and J22 (VIN_HP29)
    b. If installed, remove the jumpers between J31 (GND) and J18 (GND)
3. Make sure the shorting jumper across J24 and J16 is installed.
4. Install all five shorting jumpers across the J2 header.
5. Install the J25 (XINT) shorting jumper to connect the center pin to H
6. Install the J26 (PG) shorting jumper to connect the center pin to H
7. Install the J28 (ENCAL) shorting jumper to connect the center pin to L
8. Connect a PWM generator to the J29 (ENTX) center pin. The voltage level must be from 0V to 5V. Make sure the PWM generator is turned off.
9. Install the J30 (ENG) shorting jumper to connect the center pin to L
10. Connect a 120V DC power supply between J22 (VIN_HP29) and J18 (GND)

- Add additional capacitors between J22 & J18 when running heavy load transients without the ACT43950 being used as the input supply.

11. Connect a 12VDC power supply between V12 and GND at J32.
12. Connect the Qorvo dongle USB-TO-I2C cable to J17. The black wire connects to the GND pin.
13. If testing a dummy resistor load
    a. Connect the resistor between J19 (VD) and J21 (GND).
14. If testing an RF PA
    a. Connect the RF PA Drain between J19 (VD) and J21 (GND).
    b. Connect the gate to J11.
    c. (Optional) connect an RF input source between J16 and J9. Ensure the RF signal to the RF PA is disabled.

ACT43750 GUI Operation

ACT43750 GUI can control both the ACT43750 and the ACT43850

GUI Setup

Refer to the end of this document for detailed instructions to install the ACT43x50 GUI.

ACT43750 GUI Operation

1. Select Basic for normal operation, see Figure 4.
2. Select Registers to view or change the register content
3. Click on the "Read" icon and confirm the GUI returns "Success"
4. Select Tool for I2C address

Configure the Settings

OCP current sense resistor setting

- Default current sense resistor is 1mΩ for typical 35A overcurrent protection.

Calibration current sense resistor setting

- Default calibration current sense resistor is 2Ω for 750mA bias current.

By entering the proper resistance (R2), the resulting bias current will display.

Note 1: Bias current can adjust +/- 31% digitally, Idq offset (%) button can do this function.

Note 2: If the bias current adjustment is larger than +/-31%, the calibration resistor must be changed.

Please refer to APP Note 2 for details.

Gate voltage control

- Default gate voltage is –4.5V
- Default min gate voltage is –4.5V and max gate voltage is –1.5V
- Gate voltage can be changed by drop down menu in setting

Note: Gate voltage can be changed when ENTX is low. If ENTX is high, the gate voltage is not allowed to change.

- Auto calibration can be done after enabling Vgate

Drain voltage control

- Turn on /off drain switch by click Enable Vdrain
- "Enable Vdrain" is only for continuous operation of the drain switch
-

Steps to Enable the ACT43750 and the ACT43850

- Push Enable Vgate button
- Confirm the output voltage of the ACT43850 is the default 48V or the selected value
- Confirm the gate voltage is -4.5V

Steps to Enable the ACT43750 Autocalibration

- Push Enable Autocalibration button
- Confirm the gate voltage is around -2.6V

Steps to Enable/Disable the ACT43750 Drain Switch

- Push Enable Vdrain button
- Confirm the drain voltage is present
- Push this button again
- Confirm the drain voltage is zero

Note: The " Enable Vdrain" function is only for continuous operation. For pulse operation, Apply PWM pulse to ENTX pin. Don't push this button.

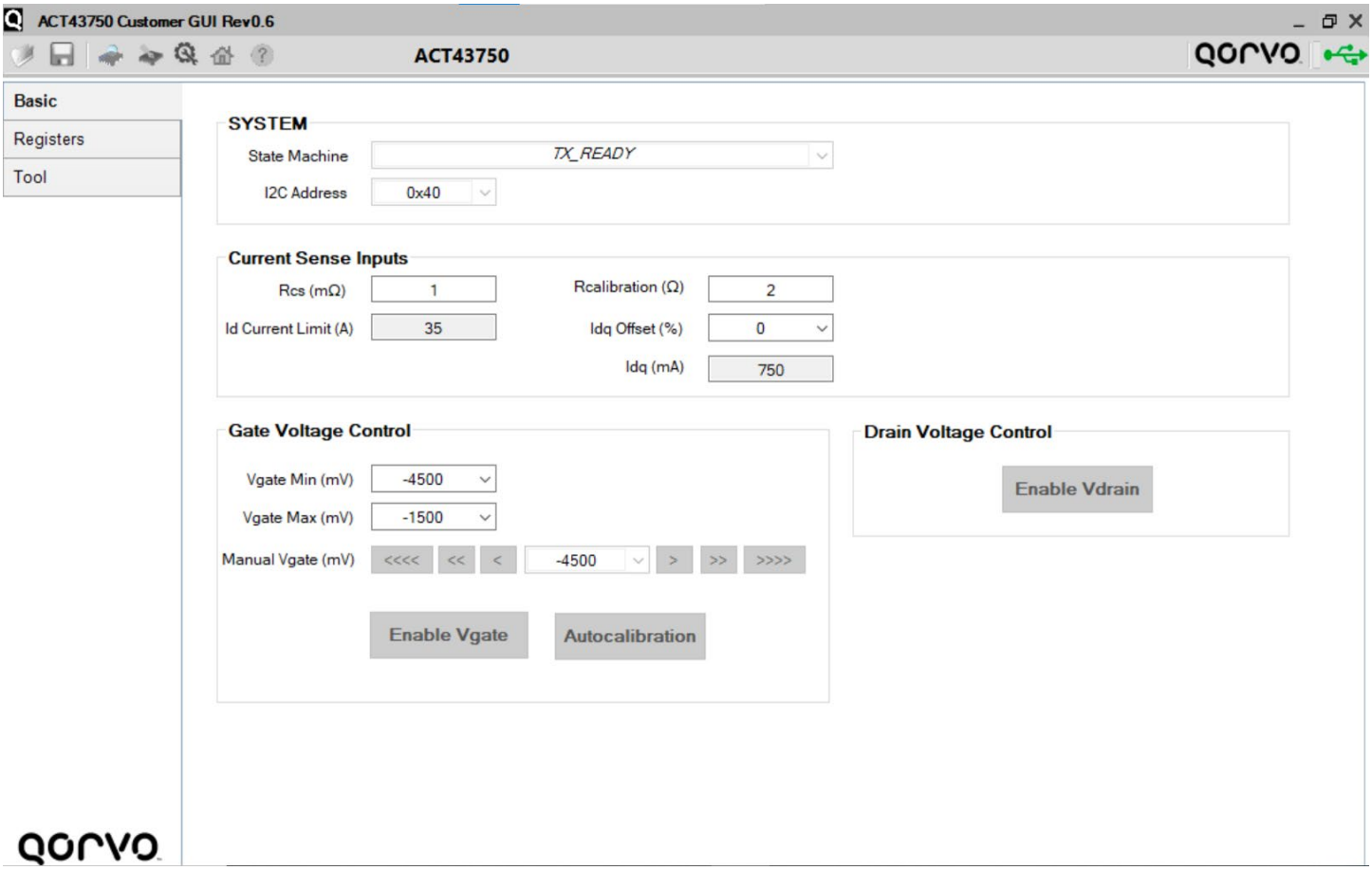


Figure 8. ACT43750EVK GUI interface

Recommended Operating Conditions

The ACT43850 is designed for up to 150V input voltage. The maximum operating voltage is determined by the IC's maximum input voltage rating of 150V. The default ACT43850 output voltage is 48V, so the design should be operated with Vin greater than 80V by default. See the ACT43850 datasheet for details on modifying this output voltage. The maximum output current is 20A. The switching frequency is set to 500kHz to optimize efficiency. The customer can easily reconfigure the EVK for different switching frequencies and output voltages after referring to the datasheet for the required component changes.

The ACT43750 is designed for a 20A load. It can be tested with an RF PA or with a resistive load. The default output drain voltage is 48V, so the minimum default drain resistor value should be 2.45 Ohms. The default gate resistor value is shown in schematics Figure 13.

Table 2. Recommended Operating Conditions for ACT43750 and ACT43850

Parameter	Description	Min	Typ	Max	Unit
VIN	Input voltage	See note1	-	150	V
Vdrain	Drain voltage	20	48	55	V
Idrain	Drain current	0	-	20	A
Frequency	Switching frequency	450	500	900	kHz
V12V	12V DC bias	10.8	12	13.2	V
PWM On-Time		10		tbd	µs
Duty ratio			0.1		

Note1. Minimum input voltage requirement can be found in ACT43850 datasheet Figure 60 to Figure 63.

ACT43750 and ACT43850 Test Probing

Use DMM meter to measure input and output voltages at test points

Use a voltage probe to measure input voltage, switching node voltage waveforms at test points.

Use current probe to measure the inductor current waveforms if desired. This requires lifting the output voltage side of the inductor.

ACT43750 and ACT43850 Test Procedure

Warning:

- Devices may be damaged if the power up/power down procedure are not strictly followed.
- Don't touch the high voltage potentials: input voltage & output voltage terminals, test points, capacitors, and inductor.

Power up

1. Make sure the RF input signal is turned off.
2. Power on the 12V bias supply.
    a. The waveform at the SW test point should not be switching and the 12V current is about 5mA.
3. Power on the 120V supply
    a. The waveform at SW test point should still not be switching and the 120V current should be about 0mA.
4. Using the GUI, enable the ACT43750 and the ACT43850 by clicking "Enable Vgate." This step enables the ACT43750 gate and ACT43850 output by having the ACT43750 IC write an I2C command to turn it on.
5. Confirm the ACT43750 gate voltage is -4.5V (default).
6. Confirm the ACT43850 SW waveform is switching and that its V50 output voltage is 48V.
7. If testing a switching Vd, enable the ACT43750 by applying a pulsed voltage waveform to J29. Note that J29 has a 50 Ohm termination and that the PWM signal should be between 0V-5V. The pulse width on-time should be greater than 10us. To limit power dissipation of devices, typical duty ratio should be less than 1%.

8. Measure the gate and drain voltage and drain current. Gate voltage should be -4.5V. The drain voltage is pulse. The amplitude is the default V50 and pulse width is set by PWM signal. The drain current is determined by drain voltage and load.
9. Take the load resistor power handling capability into consideration when setting the pulse duty cycle. The resistive dummy load supplied by Qorvo is typically capable of 30W average power.
10. If testing with RF Power, apply the RF power.

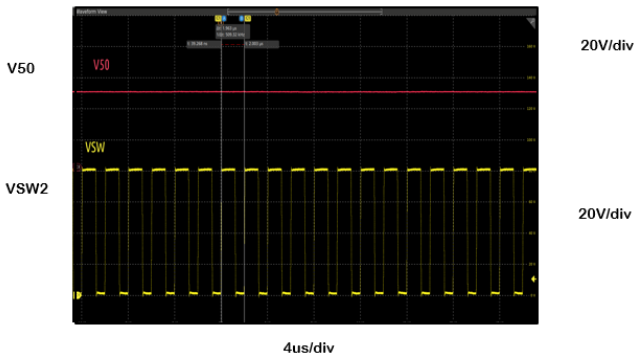
Power down

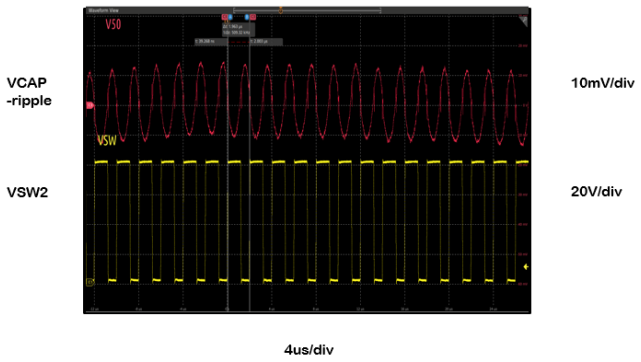
1. If testing an RF PA with an RF input signal, disable the RF input.
2. Disable the drain switch by turning off the ENTX PWM pulses or connecting the ENTX jumper to L.
3. For actual PA load, using the GUI, disable the ACT43850 Vd and ACT43750 Vg by clicking "Disable Vgate".

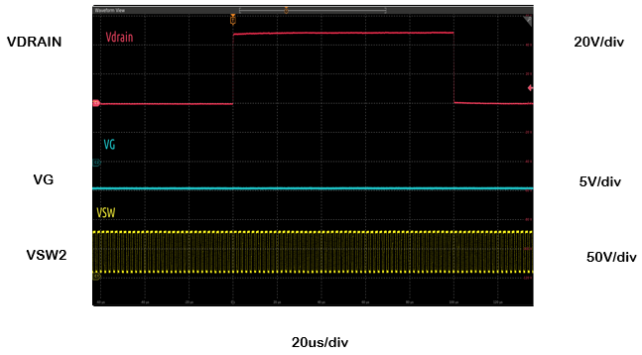
   Note: If dummy load is used, don't click "Disable Vgate". Please skip this step.
4. Power off 120V DC power supply. Note that the 120V DC supply must be turned off before the 12V bias supply
5. Power off 12V DC power supply

Test Results

Test condition, Input voltage=80V, output voltage=48V, load=300 ohm






VDRAIN
Vdrain
20V/div
VG
VG
5V/div
VSW
VSW2
50V/div
20us/div

ACT43X50PCKCB1 3-Chip Combo Board Overview

Qorvo's 3-chip Combo Board contains all three ICs, the ACT43950, ACT43850, and ACT43750. The three individual sections of the PCB are jumped together to form a complete RFPA power solution.

The input voltage for this Combo Board requires 320VDC and 12VDC input voltages.

This configuration requires the Qorvo USB-TO-I2C dongle and the ACT43x50 GUI. The 43750GUI turns on/off the ACT43750/43850 to provide the overall sequencing control and gate and drain voltages for PA. This is accomplished by an I2C connection between the two ICs. The USB-TO-I2C dongle uses a GPIO to control the ACT43950. If testing the ACT43750 pulsed drain function, a PWM generator with a 0V to 5V output with 50 Ohm termination is needed.

Required Equipment

- ACT43950/43850/43750EVK
- DC power supply - 180~400V @ 5A for full power operation
- DC power supply – 0-12V@ 1A
- Oscilloscope - 100MHz, 4 channels
- High voltage probe (>300V)
- Digital Multi-meters (DMM) (>300V)
- Windows compatible PC with spare USB port
- Qorvo I^2C USB cable

Hardware Setup

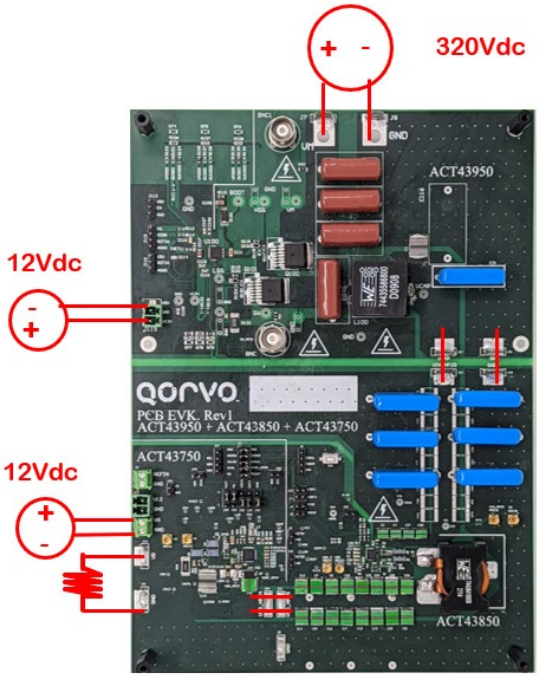


Figure 9. ACT43950/43850/43750 Combo Setup

Quick Start

Hardware Connections

Refer to Figure 9 for hardware connections.

Make all connections with power off

Setup for ACT43950

1. Connect a 320Vdc power supply to connector J7 and J8 for input voltage (VIN) while 320V is off. Please ensure the correct power supply polarity.
2. Connect 12V DC supply between V12V & GND @ J119
3. Connect the jumpers between J27 (VCAP) and J22 (VIN_HP29)
4. Connect the jumpers between J31 (GND) and J18 (GND)

Setup for ACT43850 and ACT43750

5. Make sure the shorting jumper across J24 and J16 is installed.
6. Install all five shorting jumpers across the J2 header.
7. Install the J25 (XINT) shorting jumper to connect the center pin to H
8. Install the J26 (PG) shorting jumper to connect the center pin to H
9. Install the J28 (ENCAL) shorting jumper to connect the center pin to L
10. Connect a PWM generator to the J29 (ENTX) center pin from center to L. The voltage level must be from 0V to 5V. Make sure the PWM generator is off.
11. Install the J30 (ENG) shorting jumper to connect the center pin to L
12. Connect a 12VDC power supply between V12 and GND at J32.
13. Connect the Qorvo USB-TO-I2C Dongle cable to J17. The black wire connects to the GND pin.
14. If testing a dummy resistor load
    a. Connect the resistor between J19 (VD) and J21 (GND).
15. If testing an RF PA
    a. Connect the RF PA Drain between J19 (VD) and J21 (GND).
    b. Connect the gate to J11.
    c. (Optional) connect an RF input source between J16 and J9. Ensure the RF signal to the RF PA is disabled.

All ACT43750/43850/43950 Test GUI Operation

GUI Setup

Refer to the end of this document for detailed instructions to install the ACT43x50 GUI.

Note: ACT43950 doesn't have an I²C function. The ACT43750 GUI controls the dongle GPIO to enable the ACT43950

GUI Operation

Both the ACT43750 and ACT43850 GUIs are integrated in one program. Either ACT43850 or 43750 can be selected.

1. Same steps as ACT43850 standalone operation, see Figure 4 for details.
2. Same steps as ACT43750 standalone operation, see Figure 8 for details.

All 3-Chip Operation

Input: 320V DC power supply at ACT43950

12V DC bias for IC operation & Vg generation (2 terminal blocks)

Output: Vg (Gate dc bias), Vd (Drain switching pulse)

Control: Qorvo dongle I²C @ ACT43750, GPIO @ ACT43950

PWM generator for Vd pulse @ ACT43750

Operation Basic:

Very similar to operation of ACT43750 (w/ACT43850 slave), but the "120V dc supply" comes from ACT43950.

This combo board supports 48V/20A/500us drain pulse with on board 90uF.

Additional 50uF to 100uF needed for 1ms pulse.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for ACT43950

Parameter	Description	Min	Typ	Max	Unit
VIN	Input voltage	180	-	400	V
VCAP	Output capacitor voltage	125	130	140	V
Icharge	Charge current	1	-	4	A
V12V	12V dc bias voltage	10.8	12	13.2	V

Table 4. Recommended Operating Conditions for ACT43850

Parameter	Description	Min	Typ	Max	Unit
VIN	Input voltage	See note1	-	150	V
Vdrain	Drain voltage	20	48	55	V
Idrain	Drain current	0	-	20	A
Frequency	Switching frequency	450	500	900	kHz
V12V	12V DC bias	10.8	12	13.2	V

ACT43750, ACT43850, and ACT43950 Test Probing

Use DMM (>300V) meter to measure input and DMM (<300V) output voltages at test points

Use a high voltage probe (>300V) to measure input voltage, switching node voltage waveforms at test points.

Use voltage probe (<300V) to measure VCAP voltage.

Use current probe to measure the inductor current waveforms if desired. This requires lifting the output voltage side of the inductor.

All 3-Chip Test Procedure

Warning:

- Devices may be damaged if the power up/power down procedure are not strictly followed.
- Don't touch the high voltage potentials: input voltage & output voltage terminals, test points, capacitors, and inductor.

Power up

1. Make sure the ACT43950 is disabled.

   Using the GUI to enable or disable the ACT43950, confirm that ID0 = LOW to disable the ACT43950. Make sure J113 does not have a shorting jumper installed.

   - Note: Read/write function don't work for GPIO function. Measure EN pin voltage to confirm enable or disable

2. Power on the 12V bias supply for both J119 & J32

   - The waveform at SW test point should not be switching and the 12V current should be ~1mA.

3. Power on the 320V supply

   - The waveform at SW should still not be switching and the 320V current should be <1mA.

4. Enable the ACT43950

   - Using the GUI, click on the ID0 = HIGH button.

5. ACT43950 should be enabled.

6. Compare the operating waveforms to those below to confirm proper operation.

7. Enable the ACT43850/43750
   - Using the GUI enable the ACT43750 by clicking "Enable Vgate". This step also enables ACT43850 by having the ACT43750 IC write an I2C command to turn on the ACT43850. Refer to figure 6.
8. Confirm the ACT43750 gate voltage is -4.5V (default).
9. Confirm the ACT43850 SW waveform is switching and that its V50 output voltage is 48V.
10. Enable the drain switch by applying ENTX PWM to J29. Note that J29 has a 50 Ohm termination and that the PWM signal should be between 0V-5V. The pulse width on-time should be greater than 10us. Pulse width higher than 500us will need more capacitance. To limit the power dissipation of devices, the typical duty ratio should be less than 1%.
11. Measure the gate and drain voltage and drain current. Gate voltage should be -4.5V. The drain voltage should be switching between 0V and the programmed V50 output voltage, and the frequency and pulse width should match the input PWM signal. The drain current is determined by drain voltage and load. If testing without drain switching the drain voltage should be DC at the programmed voltage.
12. Take the load resistor power handling capability into consideration when setting the pulse duty cycle. The resistive dummy load supplied by Qorvo is typically capable of 30W average power.
13. Auto-calibration should be done after step 1-10 resistive load test if testing with RF PA. Refer to the auto-calibration section later for details.

    Note 1: Calibration resistor change is necessary for certain RFPA dc bias current. Please refer to App Note 2.

    Note 2: RFPA drain capacitor change is necessary. Please refer to App Note 4 for details.
14. If testing with RF Power, apply the RF power.

Power down

1. If testing an RF PA with an RF input signal, disable the RF input.
2. Disable the drain switch by turning off the ENTX PWM pulses or connecting the ENTX jumper to L.
3. Disable the ACT43850
   a. If using an RFPA, using the GUI, click "Disable Vgate" to disable the ACT43850.
   b. If using a resistive load, don't click "Disable Vgate". Please skip this step.
4. Disable the ACT43950
   a. Using the GUI, set ID0 = LOW. If using the EN pin, short it to ground.
5. For safety, let the VCAP output voltage decay below 30V before touching the probes connected to the PCB or handling the PCB.
6. Power off 320V
   a. VCAP should be lower than 30V before turning off the 320V supply.
7. Power off 12V bias on both J119 & J32

Do auto calibration test for RFPA

Turn on

- Remove the big drain capacitor. Refer to App Note 4.
- Connect RFPA
- Power on 12V bias voltage
- Power on 50V voltage source
- Turn on VG to -4.5V by clicking "Enable Vgate".
- In ACT43750 GUI, click "Autocalibration.
- VG ramp up to the target voltage and DC bias current reach the target.
- Record the gate voltage and the bias current after auto-calibration.

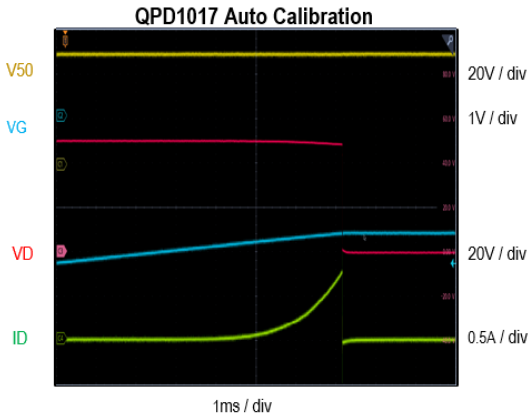
Turn off

- Change VG to -4.5V by selecting "Manual Vgate (mV)"
- Power off 50V voltage source
- Power off 12V bias voltage

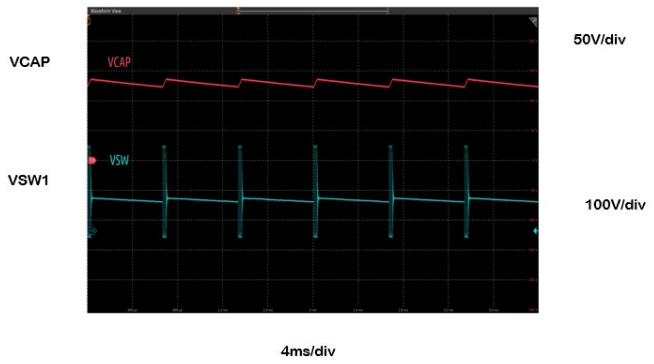
For ACT43X50PCKCB1,

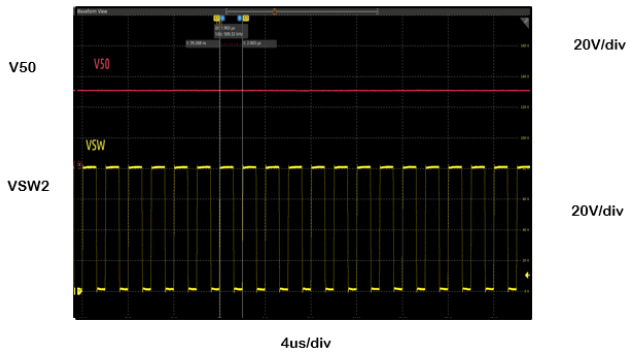
The default bias current is 750mA. Full load is 20A. OCP is 35A.

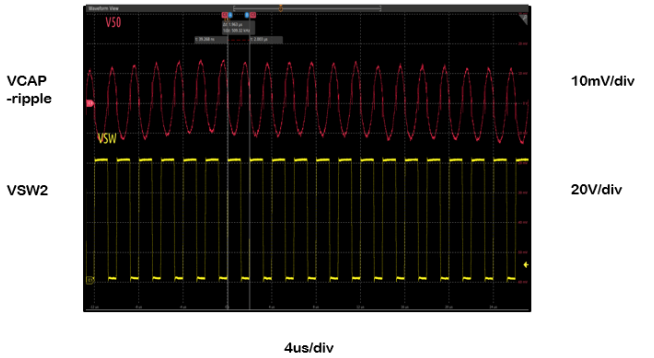
RFPA is QPD1017 or QPD1028

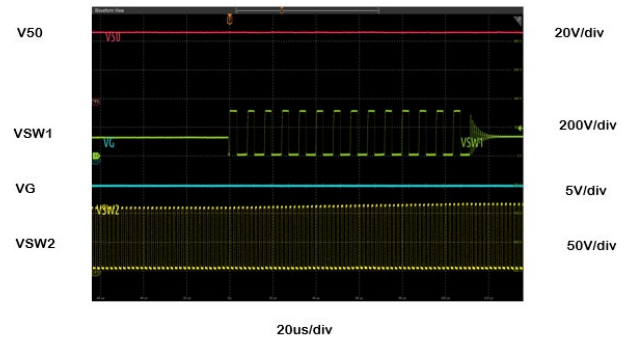


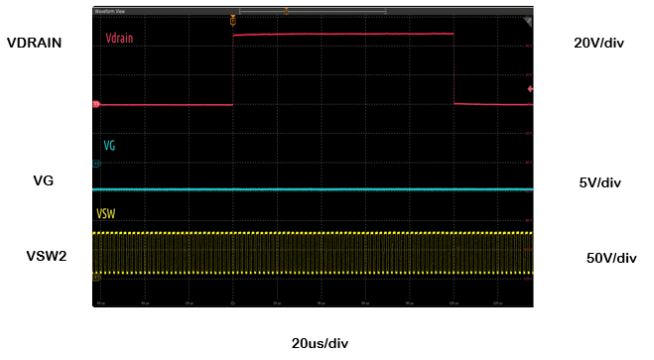
Test Results (Test condition: Input voltage=320V, VCAP=124V, V50=48V) (Load=300ohm light load, Load=2.5ohm for max current operation in the last picture)

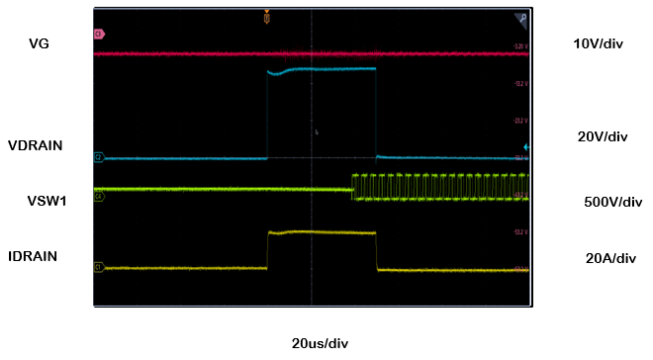












Note: SW1 is the switching node of the ACT43950 and SW2 is the switching node of the ACT43850.

Schematic

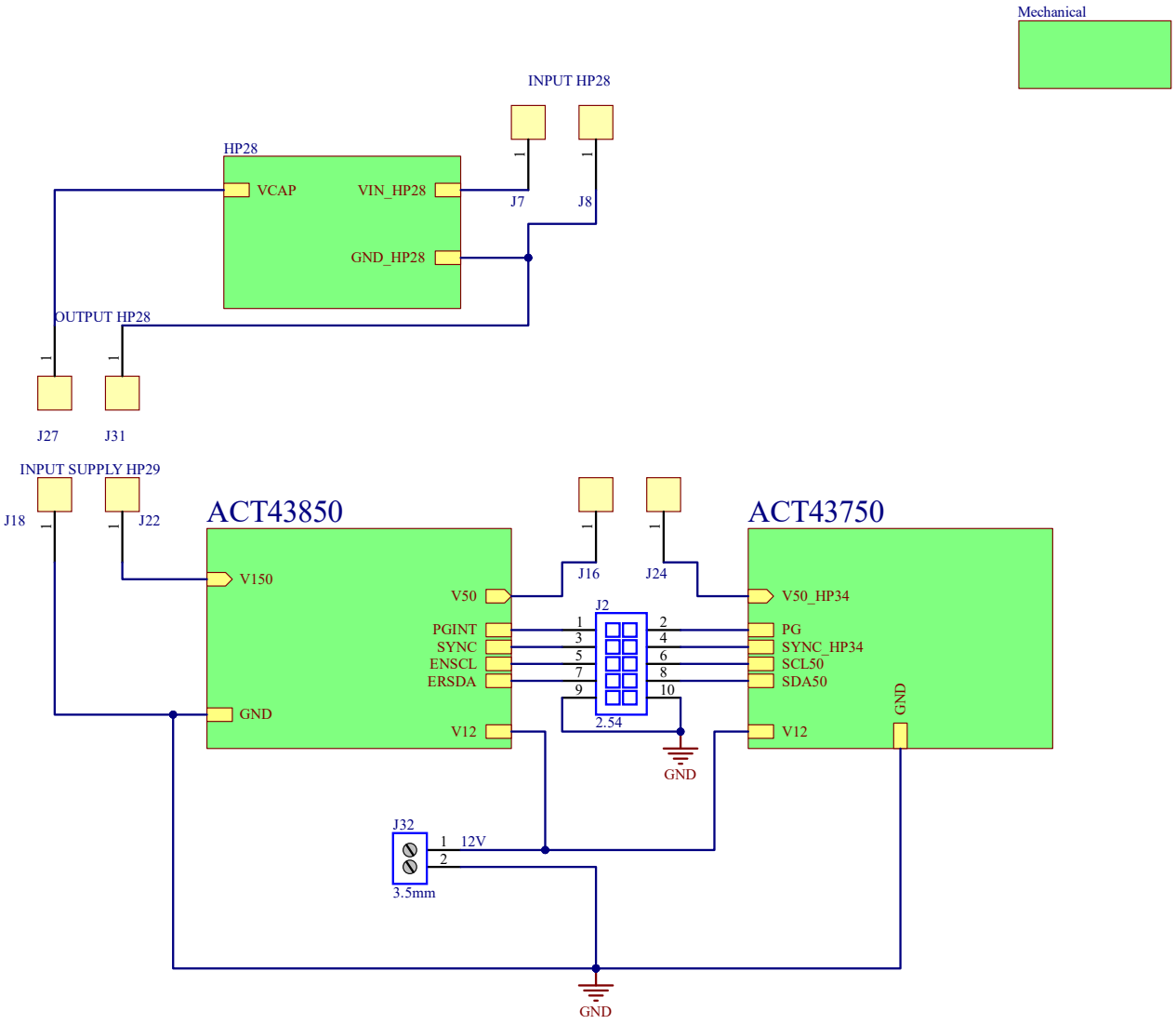


Figure 10. Schematic Top Level

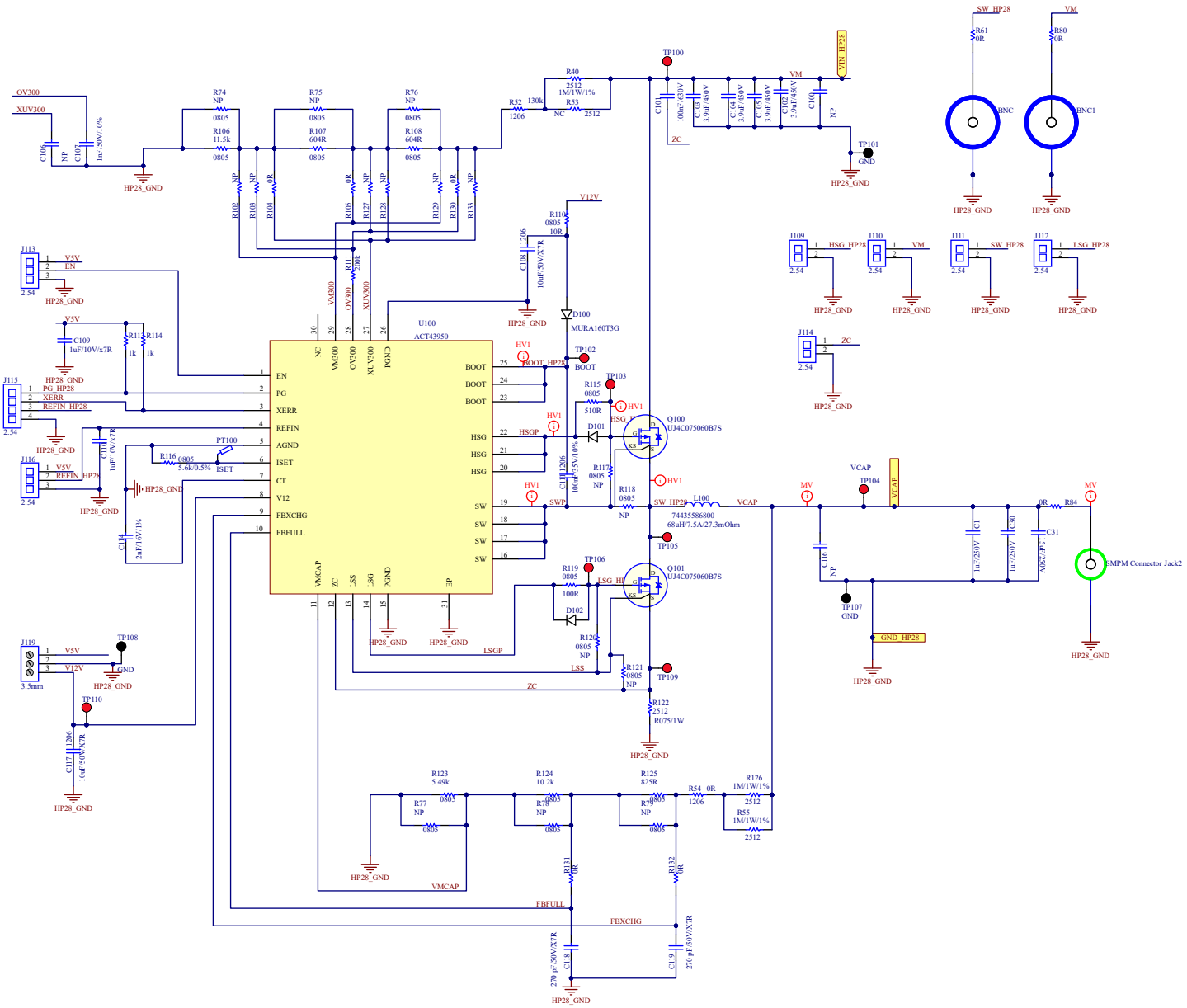


Figure 11. Schematic ACT43950

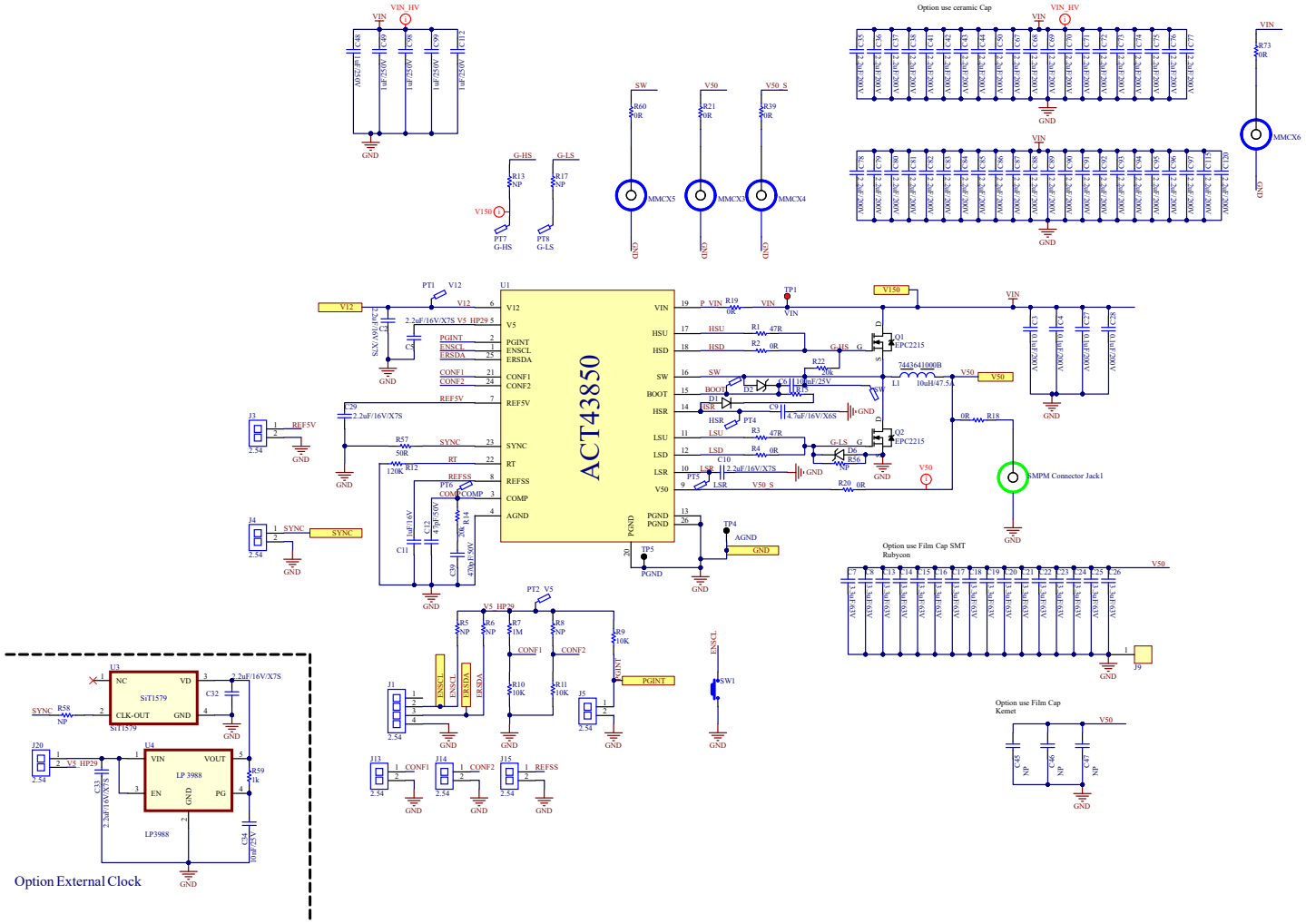


Figure 12. Schematic ACT43850

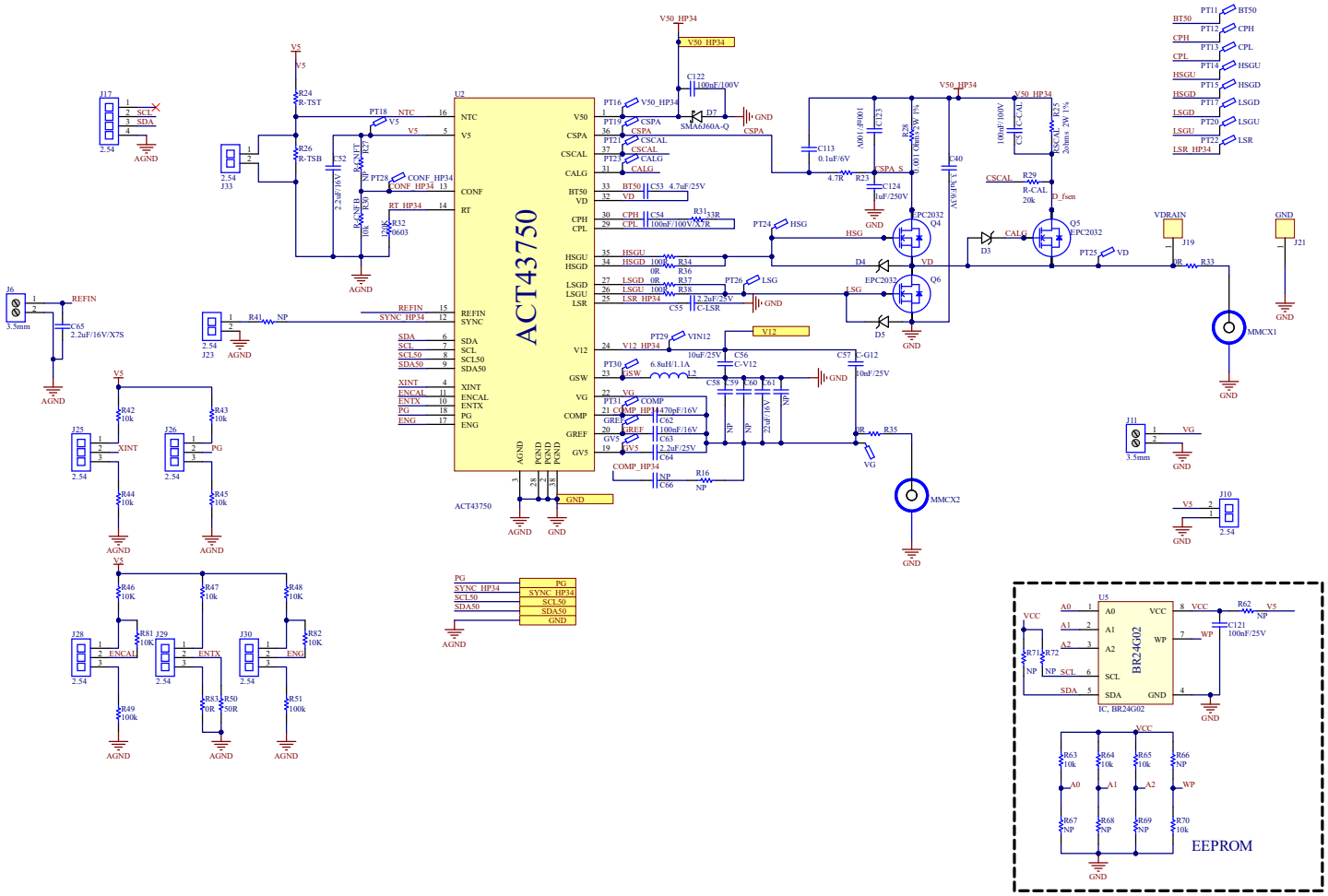


Figure 13. Schematic ACT43750

Layout

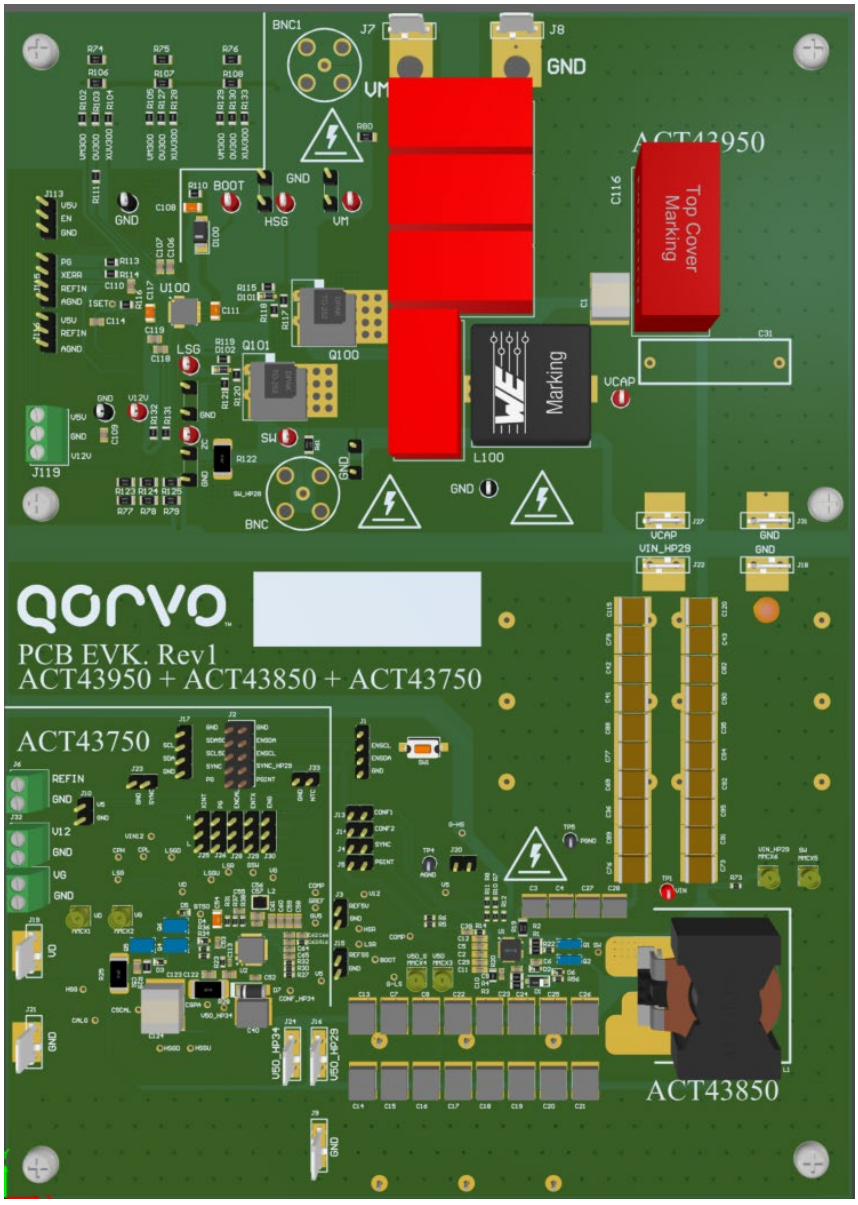


Figure 14. Assembly Top Layer

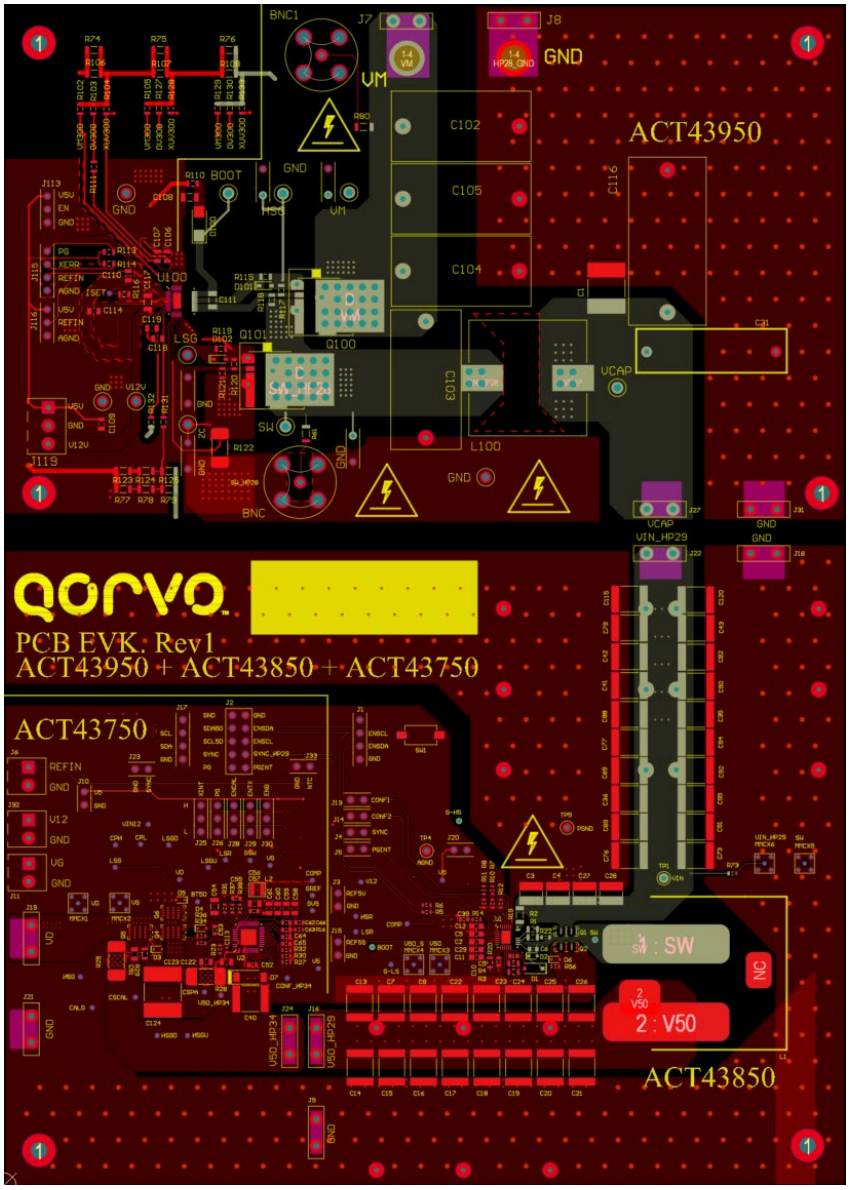


Figure 14. Layout Top Layer

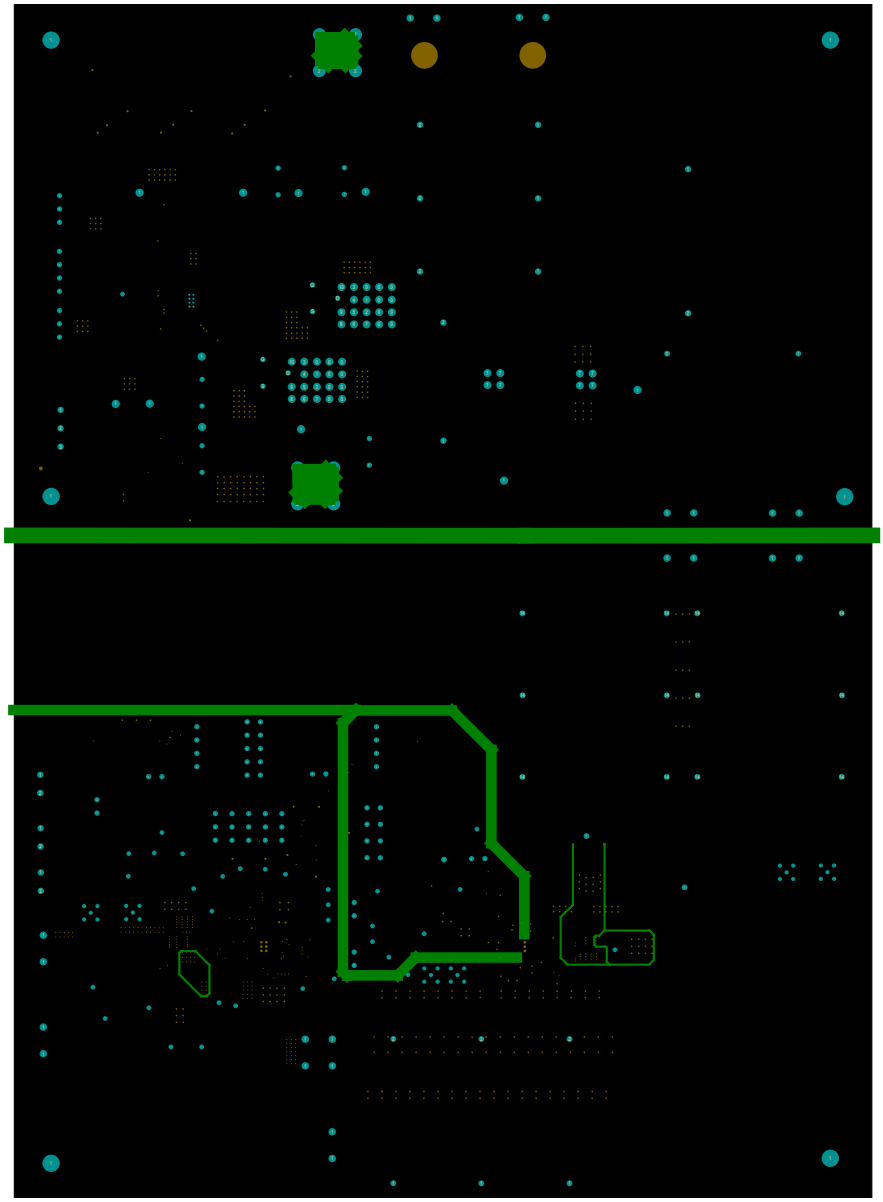


Figure 15. Layer 2 – GND Plane

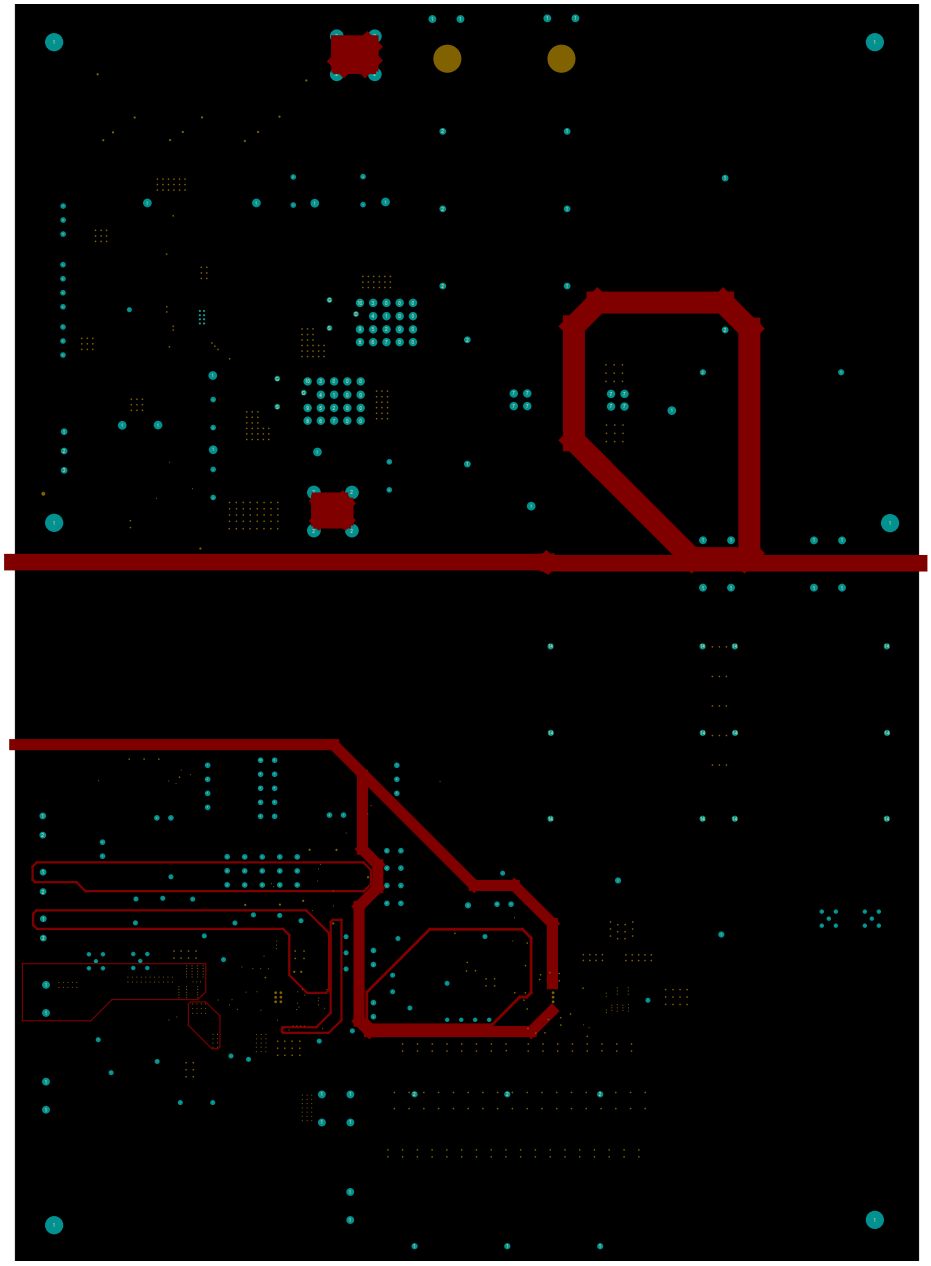


Figure 16. Layer 3 - GND Plane

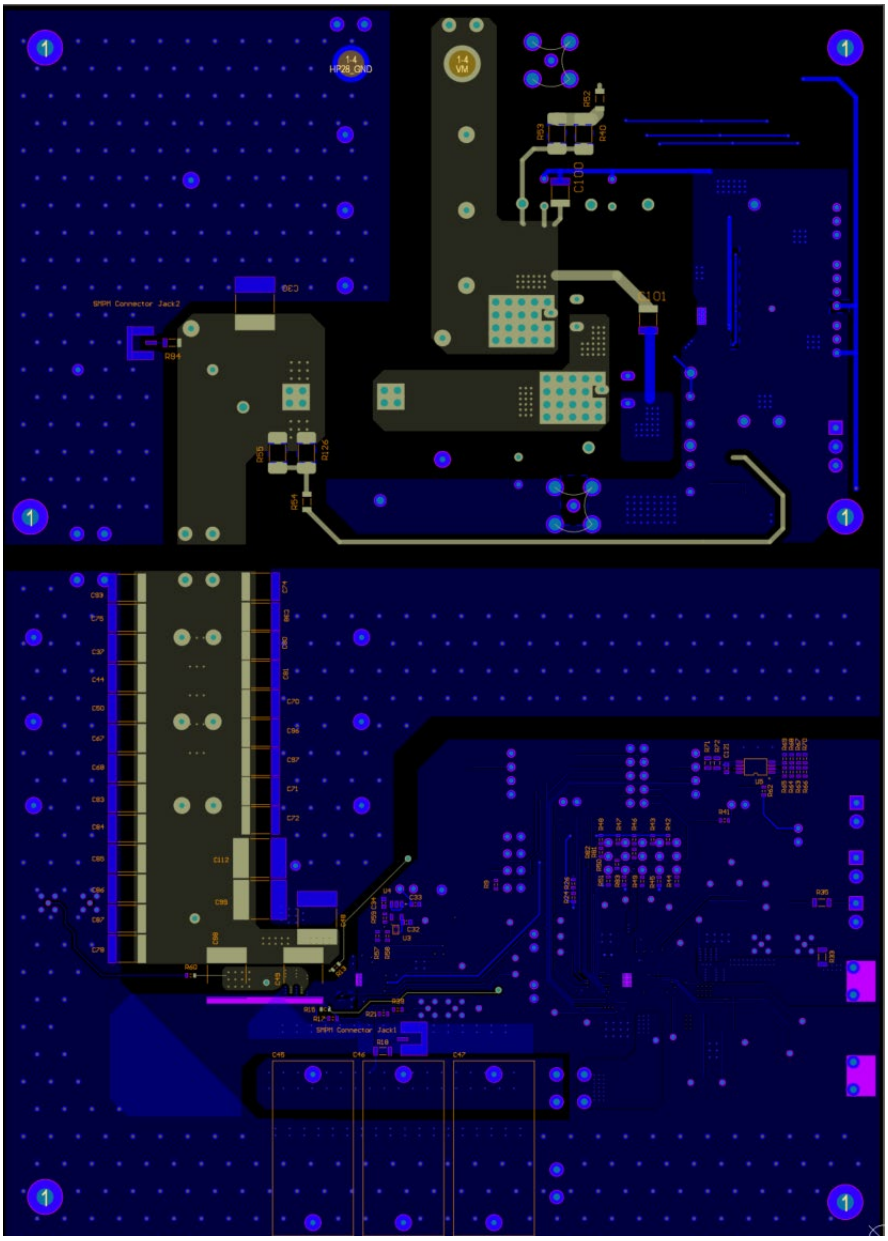


Figure 17. Layout Bottom Layer

Bill of Materials

ACT43750 BOM

Description	Value	Package	Designator	Vendor	Part Number	Qty
MMCX		MMCX	MMCX1, MMCX2	WE		2
Capacitor, Film Cap	3.3uF/63V	2220	C40	Rubycon	63MU335MD35750	1
Capacitor FILM	1uF/250V		C124	Standard	250 MH 105 M F2 8271 (250V, 1µF, 8271 size)	1
CON, QC TAB	TAB		J19, J21, J24	TE Con	1217861-1	3
Header, Unshrouded , 2.54, Male, 2P	2.54, Male, 2P	2.54, Male, 2P	J10, J23, J33, J34	Wurth	61300211121	4
Header, Unshrouded , 2.54, Male, 3P	2.54, Male, 3P	2.54, Male, 3P	J25, J26, J28, J29, J30	Wurth	61300311121	5
Header, Unshrouded , 2.54, Male, 4P	2.54, Male, 4P	2.54, Male, 4P	J17	Wurth	61300411121	1
Connector, Screw Terminal, 3.50, 2P	3.50, 2P	3.50, 2P	J6, J11	Wurth	691214110002S	2
IC, ACT43750	ACT43750	TSLP 30L 5X5 4mm Pick	U2	Qorvo	ACT43750	1
IC,	EEPROM Memory IC 1Kb (128 x 8)	8-TSSOP	U5	Rohm	BR24G02FVT-3AGE2	1
Diode, Zener	Zener 5.1V	SOD-523	D3, D4, D5	MCC	BZT52C5V1T-TP	3
Resistor,	0.001 Ohms 2W 1%	2512	R28	Standard	CRE2512-FZ-R001E-2	1
Resistor,	2ohms 2W 1%	2512	R25	Bourns	CRM2512-FX-2R00ELF	1
Inductor,	6.8uH/1.1A	2520	L2	Murata	DFE252010F-6R8M=P2	1
MOSFET, N-FET, Single,	100V/48A	EPC2032	Q4, Q5, Q6	EPC	EPC2032	3
Capacitor, Ceramic,	100nF/100V	0805	C51, C122, C123	Murata	GCM21BR72A104KA37L	3
Capacitor, Ceramic,	2.2uF/16V/X7S	0603	C65	Murata	GRM188C71C225KE11J	1

Diode, TVS	66.7V Breakdown	SMA (DO-214AC)	D7	Bourns	SMA6J60A-Q	1
Capacitor, Ceramic,	0.1uF/6V	0402	C113	Standard	Standard	1
Capacitor, Ceramic,	100nF/25V	0603	C121	Standard	Standard	1
Capacitor, Ceramic,	2.2uF/16V	0603	C52	Standard	Standard	1
Capacitor, Ceramic,	4.7uF/25V	0603	C53	Standard	Standard	1
Capacitor, Ceramic,	2.2uF/25V	0603	C55, C64	Standard	Standard	2
Capacitor, Ceramic,	100nF/100V	1206	C54	Standard	Standard	1
Capacitor, Ceramic,	10uF/25V	0805	C56	Standard	Standard	1
Capacitor, Ceramic,	10nF/25V	0603	C57	Standard	Standard	1
Capacitor, Ceramic,	NP	0805	C58, C59, C61	Standard	Standard	0
Capacitor, Ceramic,	22uF/16V	0805	C60	Standard	Standard	1
Capacitor, Ceramic,	470pF/16V	0603	C62	Standard	Standard	1
Capacitor, Ceramic,	100nF/16V	0603	C63	Standard	Standard	1
Capacitor, Ceramic,	NP	0603	C66	Standard	Standard	0
Resistor,	NP	0603	R16, R27, R62, R66, R67, R68, R69	Standard	Standard	0
Resistor,	0R	0603	R83	Standard	Standard	1
Resistor,	4.7R	0603	R23	Standard	Standard	1
Resistor,	5K	0603	R24, R26	Standard	Standard	2
Resistor,	20k	0805	R29	Standard	Standard	1
Resistor,	10k	0603	R30, R42, R43, R44, R45, R46, R47, R48, R63, R64, R65, R70, R81, R82	Standard	Standard	14
Resistor,	33R (100//100//100)	1206	R31	Standard	Standard	1

Resistor,	120K	0603	R32	Standard	Standard	1
Resistor,	0R	1206	R33, R35, R84	Standard	Standard	3
Resistor,	100R	0603	R34, R38	Standard	Standard	2
Resistor,	0R	0603	R36, R37, R41	Standard	Standard	3
Resistor,	100k	0603	R49 , R51	Standard	Standard	2
Resistor,	50R	0603	R50	Standard	Standard	1
Resistor,	NP	0805	R71, R72	Standard	Standard	0
Test pin	GND			Standard	Standard	2
Test pin	VIN, VD, VG		PT16, PT25, VG	Standard	Standard	3

ACT43850 BOM

Description	Value	Package	Designator	Vendor	Part Number	Quantity
IC,	SiT1579		U3	SiTime		1
IC,	LP3988	SOT23-5	U4	TI		1
MMCX		MMCX	MMCX3, MMCX5, MMCX6	WE		4
MMCX		SMPM	MMCX4			
Probe test point (PCB hole)			PT1, PT2, PT3, PT4, PT5, PT6, PT7, PT8, PT9			9
SMPM Connector		SMPM	SMPM Connector Jack1	Amphenol RF		1
SWITCH TACTILE SPST-NO 0.05A 12V			SW1			1
Capacitor, Film Cap	3.3uF/63V	2220	C7, C8, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26	Rubycon	63MU335MD35750	16
Capacitor, Film	0.1uF/200V		C3, C4, C27, C28	Rubycon	200MU104KC43245	4
Capacitor FILM	NP		C45, C46, C47	Kemet		0
Capacitor FILM	1uF/250V		C48, C49, C98, C99, C112	Rubycon	250MH105MF28271	4
CON, QC TAB	TAB	TAB	J9, J22, J18, J16	TE Connectivity	1217861-1	4
Inductor,	10uH/47.5A	Tray	L1	Wurth Elektronik	7443641000B	1
Header, Unshrouded , 2.54, Male, 2P	2.54, Male, 2P	2.54, Male, 2P	J3, J4, J5, J13, J14, J15, J20	Wurth	61300211121	7

Header, Unshrouded , 2.54, Male, 4P	2.54, Male, 4P	2.54, Male, 4P	J1	Wurth	61300411121	1
IC, ACT43850	ACT43850	TSLP 30L 5X5 4mm Pick	U1	Qorvo	ACT43850	1
Diode, Zener	Zener 5.1V		D2, D6	MCC	BZT52C5V1T-TP	2
Capacitor, Ceramic,	47pF/50V	0603	C12	KEMET	C0603C470K5RACAUTO	1
Diode, Gerneral	200V/1A	PowerDI-123-2	D1	Diodes	DFLS1200	1
MOSFET, N-FET, Single,	200V/32A	EPC2215	Q1, Q2	EPC	EPC2215	2
Capacitor, Ceramic,	1uF/16V	0603	C11	Murata Electronics	GCG188L8EE105KA07D	1
Capacitor, Ceramic,	470pF/16V	0603	C39	Yageo	CC0603JRX7R7BB471	1
Capacitor, Ceramic,	2.2uF/16V/X7S	0603	C32, C33	Murata Electronics	GRM188C71C225KE11J	2
Capacitor, Ceramic,	2.2uF/16V/X7S	0603	C2, C5, C10, C29	Murata Electronics	GRM188C71C225KE11J	4
Capacitor, Ceramic,	10nF/25V	0603	C34	Murata Electronics	GRM188C71C225KE11J	1
Capacitor, Ceramic,	4.7uF/16V/X6S	0603	C9	Murata Electronics	GRM188C81C475KE11D	1
Capacitor, Ceramic,	15uF/250V	Through-hole	C35, C36, C37, C38, C41, C42	UCC	KTD251B156M99A0B00	6
Capacitor, Ceramic,	100nF/25V	0603	C6	Standard	Standard	1
Resistor,	47R	0805	R1, R3	Standard	Standard	2
Resistor,	120K	0603	R12	Standard	Standard	1
Resistor,	0R	0603	R21, R39, R60, R73	Standard	Standard	4
Resistor,	20k	0603	R14, R22	Standard	Standard	2
Resistor,	10R	0603	R15	Standard	Standard	1
Resistor,	0R	1206	R18	Standard	Standard	1
Resistor,	0R	1206	R19	Standard	Standard	1
Resistor,	0R	0805	R2, R4, R20	Standard	Standard	3
Resistor,	NP	0603	R5, R6, R8,	Standard	Standard	6

			R13, R17, R58			
Resistor,	50R	0603	R57	Standard	Standard	1
Resistor,	1k	0603	R59	Standard	Standard	1
Resistor,	1M	0603	R7	Standard	Standard	1
Resistor,	10K	0603	R9, R10, R11, R56	Standard	Standard	4
Test pin	GND			Standard	Standard	2
Test pin	VIN, SW, VOUT			Standard	Standard	3

ACT43950 BOM

Description	Value	Package	Designator	Vendor	Part Number	Qty
BNC		BNC	BNC, BNC1	Amphenol RF		2
Capacitor,	15uF/250V	Through-hole	C31	UCC	KTD251B156M99A0B00	1
Capacitor	NP	Through-hole	C116	Wurth	890273327007CS	0
Probe test point	Standard	Standard	PT100			1
SMPM Connector		SMPM	SMPM Connector Jack2	Amphenol RF		1
Capacitor FILM	1uF/250V	8271	C1, C30	Rubycon	250MH105MF28271	2
Capacitor FILM	1uF/250V	8271	C200	Rubycon	250MH105MF28271	1
Capacitor, Ceramic,	270 pF/50V/X7R	0805	C118, C119	WALSIN	0805B271J500CT	2
Capacitor, Ceramic,	NP	0805	C106	WALSIN	0805B102K500CT	0
Capacitor, Ceramic,	1nF/50V/10%	0805	C107	WALSIN	0805B102K500CT	1
Resistor,	500k/2W/1%	2512	R55	Stackpole	HVCB2512FTD500K	1
CON	4mm Banana Plug Jack mounter		J7 (Red), J8 (Black)	Standard	JS-910B	2
Header, Unshrouded , 2.54, Male, 3P	2.54, Male, 3P	2.54, Male, 3P	J113, J116	Wurth	61300311121	2
Header, Unshrouded , 2.54, Male, 4P	2.54, Male, 4P	2.54, Male, 4P	J115	Wurth	61300411121	1
Inductor,	68uH/7.5A/27.3mOhm	2212	L100	Wurth	74435586800	1
Connector, Screw Terminal, 3.50, 3P			J119	Wurth	691214100003	1
Capacitor, Ceramic,	NP	1812	C100	Wurth Elektronik	885342211006	0

Capacitor, Ceramic,	100nF/630V	1812	C101	Wurth Elektronik	885342211006	1
IC, ACT43950,TSLP 30L5X5	ACT43950	TSLP 30L 5X5 4mm Pick	U100	Qorvo	ACT43950	1
Capacitor, Ceramic,	2nF/16V/1%	0805	C114	KEMET	C0805C202F4HACAUTO	1
Capacitor, Ceramic,	100nF/35V/10%	1206	C111	KEMET	C1206C104K6RACTU	1
Capacitor, Ceramic,	1uF/10V/x7R	0805	C109, C110	TDK	C2012X7R1A105KT000A	2
Capacitor, Ceramic,	10uF/50V/X7R	1206	C108, C117	TDK	C3216X7R1HK160AC	2
Diode, Gerneral	20V/500mA	0603	D101, D102	Comchip Technology	CDBU0520	2
Resistor,	1M/1W/1%	2512	R40	Vishay / Dale	CRCW25121M00FKEG	1
Resistor,	NP	2512	R53, R126	Vishay / Dale, TE Connect / Holsworthy	CRCW25121M00FKEG, 3521510KFT	
Header, Unshrouded , 5.08, Male, 2P	5.08, Male, 2P		J109, J110, J111, J112, J114	Custom	Custom	5
Resistor,	5.6k/0.5%	0805	R116	Panasonic	ERJ-6RBD5601V	1
Capacitor, CAP FILM	3.9uF/450V	263X126X18	C102, C103, C104, C105	Panasonic	F2W395JA	4
Diode, General	MURA160T3G	SMA	D100	ON Semi	MURA160T3G	1
Resistor,	0R	0805	R103, R104, R105, R130,R131, R132, R133	Standard	Standard	7
Resistor,	11.5k	0805	R106	Standard	Standard	1
Resistor,	10.2k	0805	R124	Standard	Standard	1
Resistor,	604R	0805	R107, R108	Standard	Standard	2

Resistor,	**10R**	**0805**	**R110**	**Standard**	**Standard**	**1**
Resistor,	**200k**	**0805**	**R111**	**Standard**	**Standard**	**1**
Resistor,	**1k**	**0805**	**R113, R114**	**Standard**	**Standard**	**2**
Resistor,	**510R**	**0805**	**R115**	**Standard**	**Standard**	**1**
Resistor,	**100R**	**0805**	**R119**	**Standard**	**Standard**	**1**
Resistor,	**825R**	**0805**	**R125**	**Standard**	**Standard**	**1**
Resistor,	**5.49k**	**0806**	**R123**	**Standard**	**Standard**	**1**
Resistor,	**0R**	**1206**	**R54, R61, R80**	**Standard**	**Standard**	**3**
Resistor,	**NP**	**0805**	**R74, R75, R76, R77, R78, R79, R102, R117, R118, R120, R121, R127, R128, R129**	**Standard**	**Standard**	**0**
Resistor,	**0R**	**1206**	**R84**	**Standard**	**Standard**	**1**
Resistor,	**130k**	**1206**	**R52**	**Standard**	**Standard**	**1**
MOSFET, Single,	**750 V/58mhom**	D2PAK-7L	**Q100, Q101**	**UnitedSiC**	**UJ4C075060B7S**	**2**
Resistor,	**R075/1W**	**2512**	**R122**	**Vishay / Dale**	**WSL2512R0750FEA**	**1**
Test pin	**GND**			**Standard**	**Standard**	**2**
Test pin	**VIN, VOUT, SW**			**Standard**	**Standard**	**3**

GUI Installation

1. Get GUI installers from the Qorvo
2. Plug the Qorvo dongle USB-TO-I²C cable into a free USB port.
3. Follow the instructions in the "How to install driver for dongle" folder.
4. Double click on the ACT43750 GUI Rev0.6.exe to start the ACT43750 GUI
5. Double click on the ACT43850 GUI Rev4.6.exe to start the ACT43850 GUI

Application Note 1: Safe Operation at High Drain Switching Frequency

ACT43X50PCKCB1 is designed for operation at low drain switching frequency, typically less than 500Hz. If the drain switching frequency exceeds 500Hz, the charge pump circuit component R31 must be upgraded. The reason is that the power loss of resistor R31 is proportional to the drain switching frequency, capacitance, and drain voltage square. The following formula can calculate the power loss of R31:

$$P = 0.5 * C54 * V^2 * F$$

Where:

P – power loss of resistor R31, unit W.

C54 – charge pump capacitance, unit is F. It's 100nF in ACT43X50PCKCB1.

R31 – charge pump resistance, unit is ohm. It's 33ohm in ACT43X50PCKCB1.

F – drain switching frequency, unit is Hz

V – drain voltage, unit is Volt. It's 50V in typical application.

At drain switch frequency 500Hz, power loss is 0.0625w. R31 is 0603 size resistor and power rating is 0.125w. It's OK for the original board design. When the drain switch frequency exceeds 500Hz, R31 power loss is higher than the rating value. So, the R31 needs to be changed to a higher-power resistor.

The process to determine the component change is listed below:

Step 1, Calculate power loss of R31 at the desirable drain switch frequency

Step 2, If the power loss is less than 0.125w, no action is needed; if it's higher than 0.125w, then go to next step

Step 3, Find the resistors power rating is higher the requirement with good margin

Step 3, Locate R31 in the board, replace it with higher power resistors

For example, frequency is 5KHz, P=0.625w. R31 must be larger size and higher power. It's recommended to stack 5pc 182ohm 1206 size resistor replace 0603 size resistor. In ACT43X50PCKCB1 board, 3pc 100ohm 1206 size resistor in stack is used for R31.

Application Note 2: How to Configure Bias Current and Current Limit

Every RF PA has a specific dc bias drain current and drain current limit requirement.

1. DC Bias Drain Current

ACT43750 can provide setpoint +/- 31%, 1% step the drain current programming by I2C command. The register13 has 5 bits to change the setpoint. The adjustment detail can refer to Table 37 in the ACT43750 datasheet. The setting will be lost and returned to the default after the power recycle.

If the bias current adjustment is more than +/-31% setpoint, the calibration resistor R25 can be changed to get the right dc bias current. The following formula can calculate the calibration resistance.

$$R25 = 1.5V/Idq$$

Where:

Idq – RF PA dc bias current, unit A.

R25 – Calibration resistance, unit Ω.

2. Drain Current Limit

RF PA has the drain current limit to protect the device, and the current limit can be changed by resistor R1.

$$R28 = 35mV/ID$$

Where:

ID – RF PA drain current, unit A.

R28 – Current limit resistance, unit mΩ.

Please refer to the schematics and layout for resistor connection and location.

Application Note 3: How to Configure Drain Switching Time

The drain switching time is defined by the drain voltage rising and falling from 10% peak to 90% peak or 90% to 10% peak. The drain voltage VD switching transition time can be changed by adjusting the gate resistance. The default rising switching time is 100ns and falling switching time is 10ns. R34 is 100Ω. R36 is 0Ω.

To reduce rising switching time, R34 should be a smaller resistance value. To increase rising switching time, R34 should be larger resistance value. To increase falling switching time, R36 should have larger resistance value.

Please refer to schematics and layout for resistor connection and location.

Application Note 4: Drain Capacitance for RFPA Drain Switching Operation

Most RFPA evaluation kits are designed with a large drain capacitor to improve stability in CW. For RFPA drain switching operation, it should be careful to calculate the inrush current of the drain switch and ensure it is less than the drain current limit (OCP). The following formula can calculate the inrush peak current:

$$Ipk = Cd * \frac{dVd}{dtr}$$

Where:

Ipk – RF PA drain peak current, unit A.

Cd – Drain capacitance, unit F.

Vd – Drain voltage, unit V.

tr – Rising time of the drain voltage, unit s.

For an example, C=4.7uF, V=50v, t=100ns

Ipk=2350A

The default OCP is 35A. So, OCP protection will be triggered. ACT43750 will shut down the drain switching and get bias error.

To do the drain pulsing operation, we need to remove the big drain capacitor. We change the drain capacitor to 1000pF.

Ipk=0.5A

With the inrush peak current 0.5A, the drain switching can work well.

The rise time depends on the gate resistance R34. The default gate resistance R34=100Ω. The rise time is 100ns. The R34=10Ω, the rise time is 10ns.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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