USER'S GUIDE

ACT43750EVK3 User's Guide

Description

This document describes the characteristics and operation of the Qorvo ACT43750EVK3 evaluation kit (EVK). It provides setup and operation instructions, schematic, layout, BOM, GUI, and test data. This EVK ships as a standalone board that can be evaluated independently or with a GaN RF Power Amplifier.

The ACT43750 is an integrated power solution that controls GaN RF PA drain and gate:

- Generates negative gate voltage for the PA gate
- Properly sequenced turn on and turn off
- Automatic gate voltage / drain current calibration
- Drain voltage switching

It is an ideal solution for radio frequency (RF) power amplifiers (PAs) that demand fast transient, high current pulsed loads.

Features

Qorvo recommends that the user evaluate the EVK functionality with an RF PA and with the EVK connected to a PC running the graphical user interface (GUI) software. The GUI allows the user to enable/disable the outputs and to customize the exact voltage and current requirements for the specific RF PA being tested. The user can use the ACT43750 GUI to set the RF PA Idq bias current target, and the EVK autonomously finds and stores the optimal gate voltage for the Idq bias current.

Figure 1 - ACT43750EVK3 Board

EVK Contents

The EVK ships with the following:

- ACT43750EVK3 PCB
- USB-TO-I2C Dongle and cables
- The EVK does not ship with an RF PA

Hardware Setup

Required Equipment

- ACT43750EVK3
- DC power supply - 10~55V @ 10A for full power operation
- DC power supply – 12V
- Oscilloscope - 500MHz, 4 channels
- Function generator
- Current probe
- Digital Multi-meters (DMM)
- Windows compatible PC with spare USB port
- Qorvo USB-to-I²C dongle
- Compatible GaN RF PA

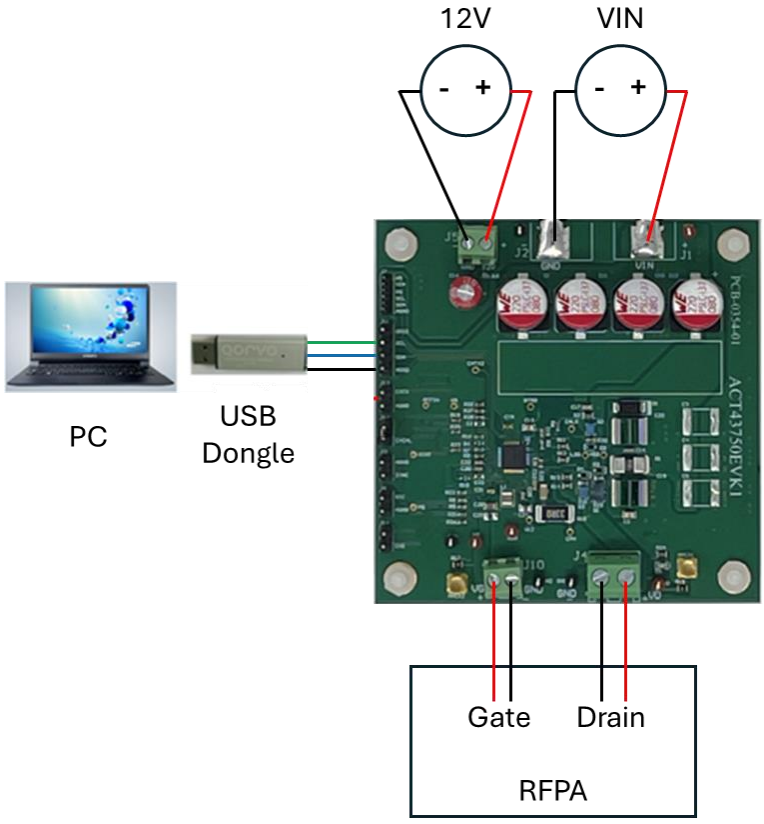


Figure 2 - ACT43750EVK3 SET-UP

Hardware Connections

Refer to Figure 2 & 3 for hardware connections. Make all connections with power off.

1) Open J12 (ENCAL)
2) Open J6 (NTC)
3) Open J14 (ENG)
4) Connect the Qorvo USB-TO-I2C dongle cable to J11. The black wire connects to the AGND pin.
5) Optional: Connect a PWM generator to the J13 (ENTX). ENTX supports 5V and 3.3V logic. Make sure the PWM generator is turned off. If an external PWM generator is not used, leave it open.
6) Connect a DC power supply between J1 (VIN) and J2 (GND). This is the voltage that is applied to the RF PA drain.
7) Connect a 12VDC power supply to J5.
8) If testing a dummy resistor load:
    a. Connect the resistor between VD and GND on J4.
9) If testing an RF PA:
    a. Connect the RF PA Drain between VD and GND on J4.
    b. Connect the RF PA Gate between VG and GND on J10.
10) The drain switch can be turned on/off by the ENTX pin or by the GUI. For high-frequency operation, connect a function generator to ENTX.

Recommended Operating Conditions

The ACT43750EVK3 operates with a 10V to 55V drain voltage and supports up to a 10A load.

Parameter	Description	Min	Typ	Max	Unit
Vdrain	Drain voltage	10	-	55	V
Idrain	Drain current	0	-	10	A
V12V	12V DC bias	10.8	12	13.2	V
ENTX On-Time		12	-	-	µs
ENTX Off-Time		40	-	-	µs

ACT43750 Test Procedure

Warning:

Devices may be damaged if the power up/power down procedure is not strictly followed.

Don't touch the high voltage potential: input voltage & output voltage terminals, test points, capacitors, and inductor.

GUI Installation

- Get GUI files from the Qorvo website
- Plug the Qorvo dongle USB-TO-I2C cable into a free USB port.
- The USB driver will be automatically installed.
- Double click on the ACT43750 Customer GUI Rev0.6.exe to open GUI

Power up

1) Make sure the RF input signal is turned off.
2) Power on the 12V bias supply.
3) Power on the Vdrain supply (set voltage to appropriate value for the RF PA)
4) Open the GUI. Press "Read" button. Press "Enable Vgate" button.
    a. This sets the Vg voltage to -4.5V.
5) If testing with an RF PA, perform auto-calibration. The gate voltage will increase until the target IDQ is met. If testing with dummy load, auto-calibration is not necessary.
    a. Note1: Calibration resistor change is necessary for certain dc bias current. Please refer to App Note 2.
    b. Note 2: RFPA drain capacitor change is necessary. Please refer to App Note 5 for drain capacitance and drain switching operation.
6) Enable the drain switches with either ENTX pin or with the GUI. The pulse width on-time should be greater than 12µs. To limit the power dissipation in the load device (dummy resistor or RF PA), consider using a low duty cycle.

Power down

1) If testing an RF PA with an RF input signal, disable the RF input.
2) Disable the drain switch by turning off the ENTX PWM pulses or using GUI
3) Power off Vdrain DC power supply.
4) Power off 12V bias supply.

ACT43750 GUI Operation

GUI Operation

- Click on the "Read" icon and confirm the GUI returns "Success"
- Basic tab: easily enable gate and drain voltages
- Register tab: edit register settings
- Tool tab: read/write I2C commands

OCP current sense resistor setting

- Default current sense resistor is 3mΩ for typical 12A overcurrent protection. Note: OCP threshold is set by the resistor on the EVK; the GUI cannot change the OCP threshold.

Calibration current sense resistor setting

- Default calibration current sense resistor is 2Ω for 750mA bias current.
- By entering the value of the R2 resistor, the target bias current will display
- Note 1: Bias current can be adjusted +/- 31% digitally, Idq offset (%) button can do this function.
- Note 2: If the bias current adjustment is larger than +/-31%, the calibration resistor must be changed.
- Please refer to APP Note 2 for details.

Gate voltage control

- Default gate voltage is –4.5V
- Default min gate voltage is –4.5V and max gate voltage is –1.5V
- Gate voltage can be changed by drop down menu in setting
- Note: Gate voltage can be changed when ENTX is low or PWM pulse operation. If ENTX is high, the gate voltage is not allowed to change.
- Auto calibration can be done after enabling Vgate

Enable the ACT43750

- Push Enable Vgate button
- Confirm the gate voltage is -4.5V

Autocalibration

- Push Enable Autocalibration button
- The gate voltage will rise until the target IDQ is met

Drain Switch

- Push Enable Vdrain button
- Confirm the drain voltage is present
- Push this button again
- Confirm the drain voltage is zero
- Note: "Enable Vdrain" button is only for continuous operation. For pulse operation, apply PWM pulse to ENTX pin.

QPD1028EVB and ACT43750EVK3 System Test

Note 1: Calibration resistor change may be necessary for certain RFPA dc bias current. Please refer to App Note 2.

Note 2: RFPA drain capacitor change may be necessary. Please refer to App Note 5.

Note 3: For high-frequency operation of RFPA, it is necessary to estimate the power loss of charge pump resistor R10. Please refer to App Note 1.

Hardware connection

- Connect J10, Vg to Vgate of QPD1028 EVB
- Connect J4, Vd to Vdrain of QPD1028 EVB
- Also connect both ground wires (J10 and J4) to the QPD1028 EVB
- Use short and wide wires to minimize inductance and resistance.

Power Up

1) Make sure RF signal is off
2) Power up the ACT43750 12V bias supply
3) Power on 50V voltage source
4) Turn on VG to -4.5V by pushing Enable Vgate button
5) Do automatic calibration by pushing the Autocalibration button. The gate voltage should gradually rise to -2.6V.
6) Measure VG waveform to confirm VG change to -2.6V.
7) Turn on/off the drain switch by applying a PWM pulse to the ENTX pin
8) Turn on RF signal

Power Down

1) Turn off RF signal
2) Turn off the drain switch by pulling the ENTX pin to low logic level.
3) Adjust VG to –4.5V.
4) Measure VG to confirm it's -4.5V.
5) Power off the 50V voltage source
6) Wait 2 seconds to allow drain capacitors to discharge
7) Turn off the 12V bias supply

Test Results

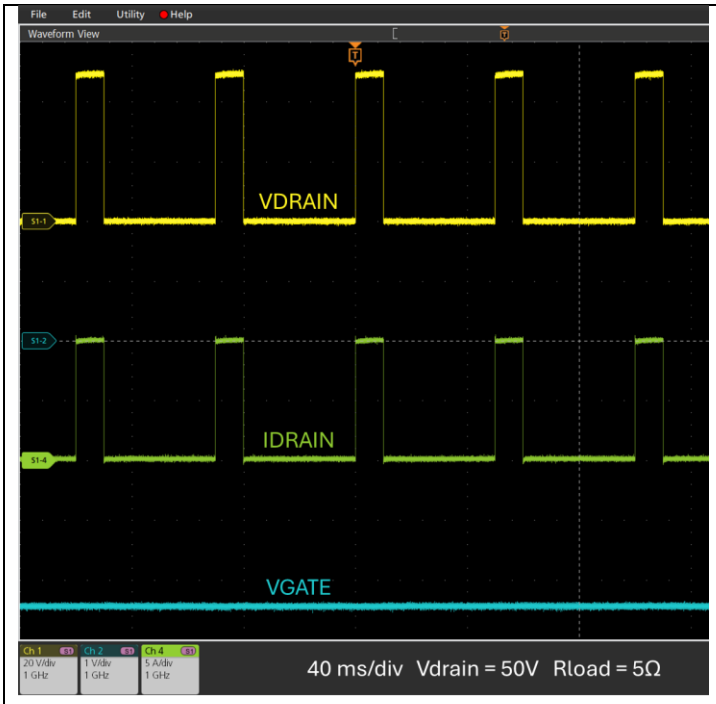


Figure 3 – Drain Switching

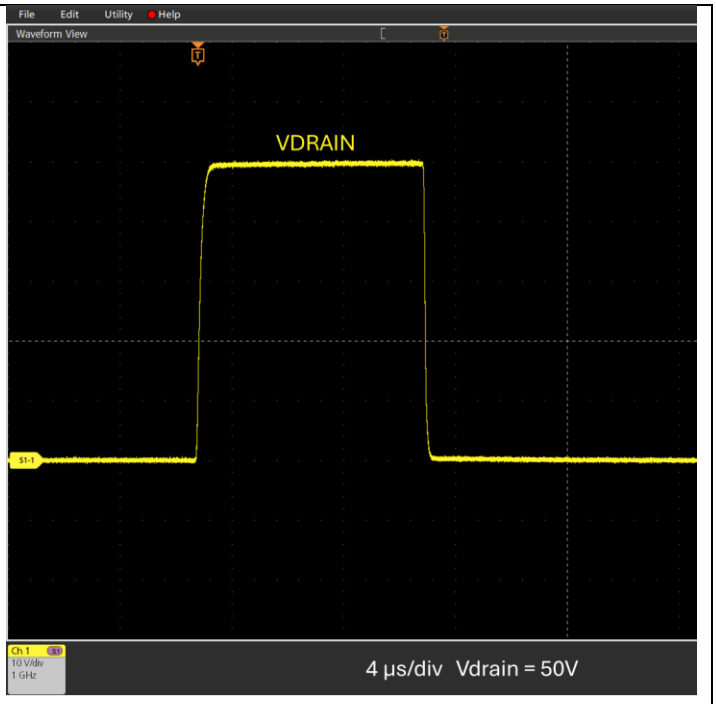


Figure 4 – Drain Rise & Fall Time

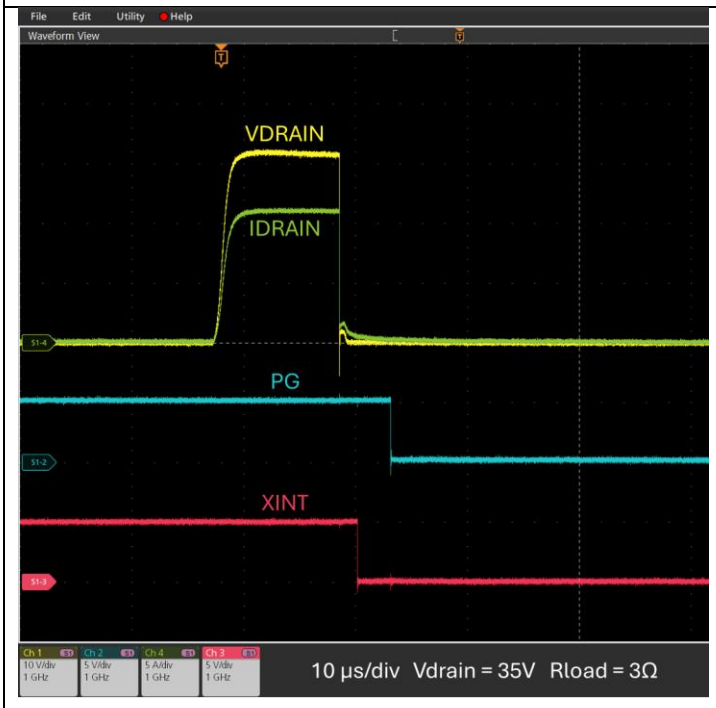


Figure 5 – Over Current Protection

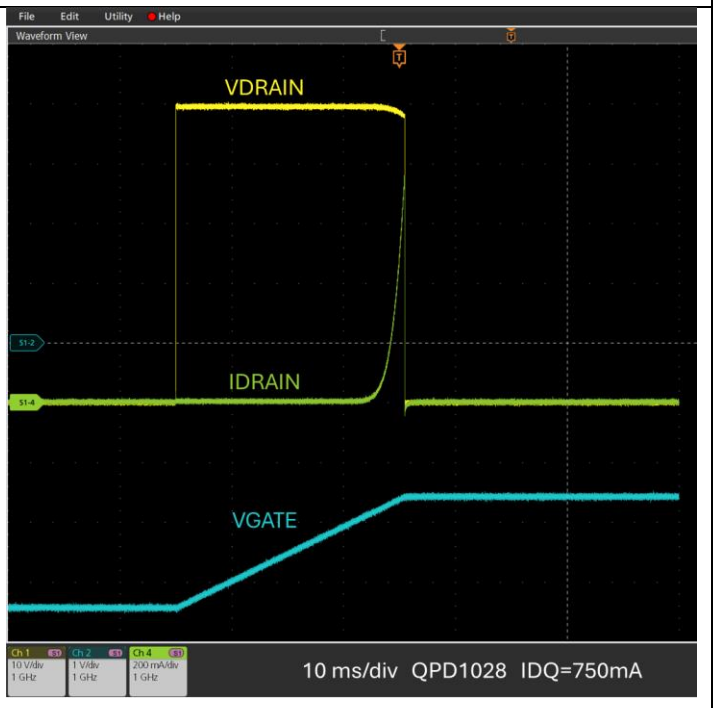


Figure 6 – IDQ Calibration

Schematic

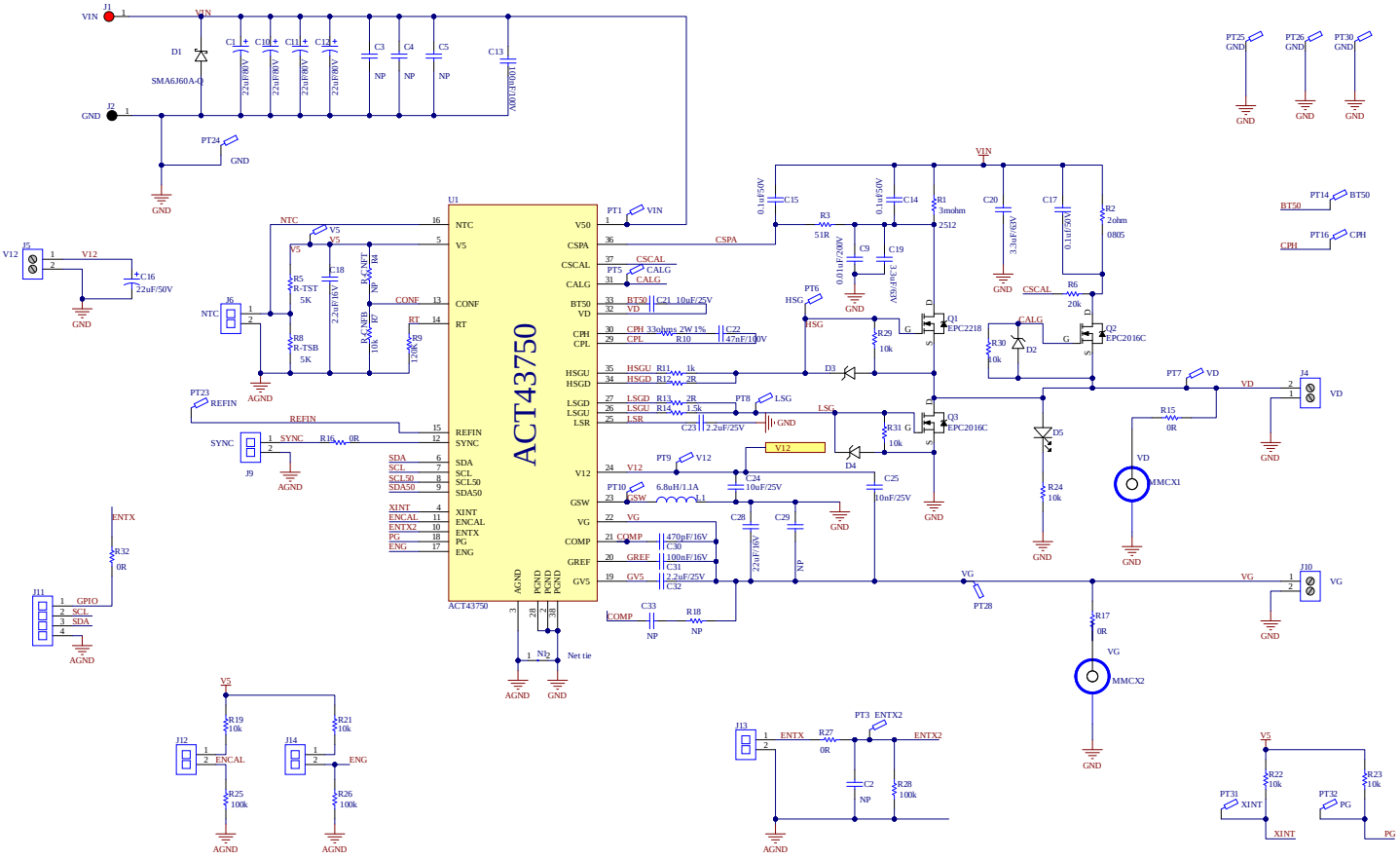


Figure 7 - Schematic

Layout

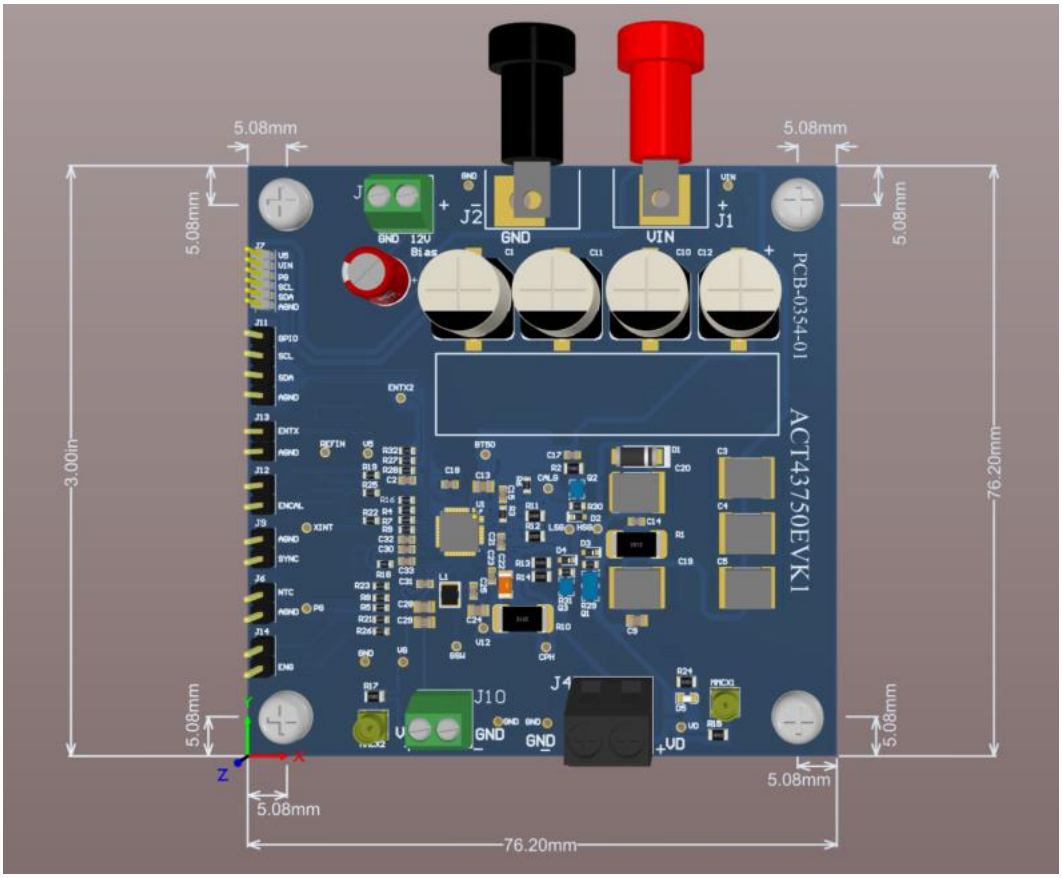


Figure 8 - Assembly Top Layer

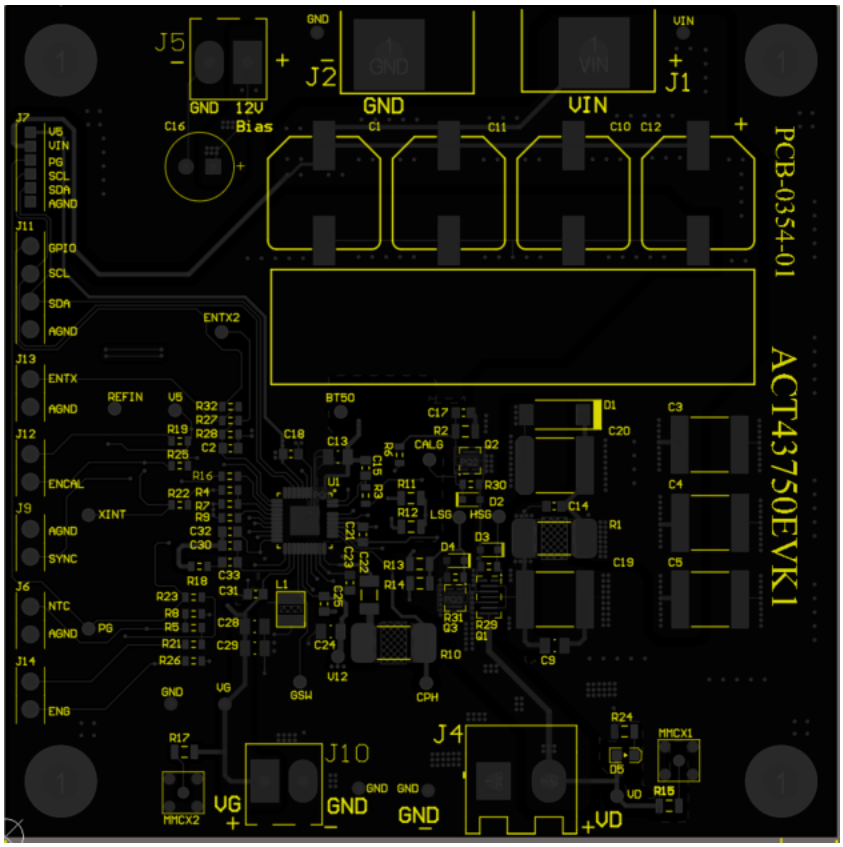


Figure 9 - Top Layer Silk Screen

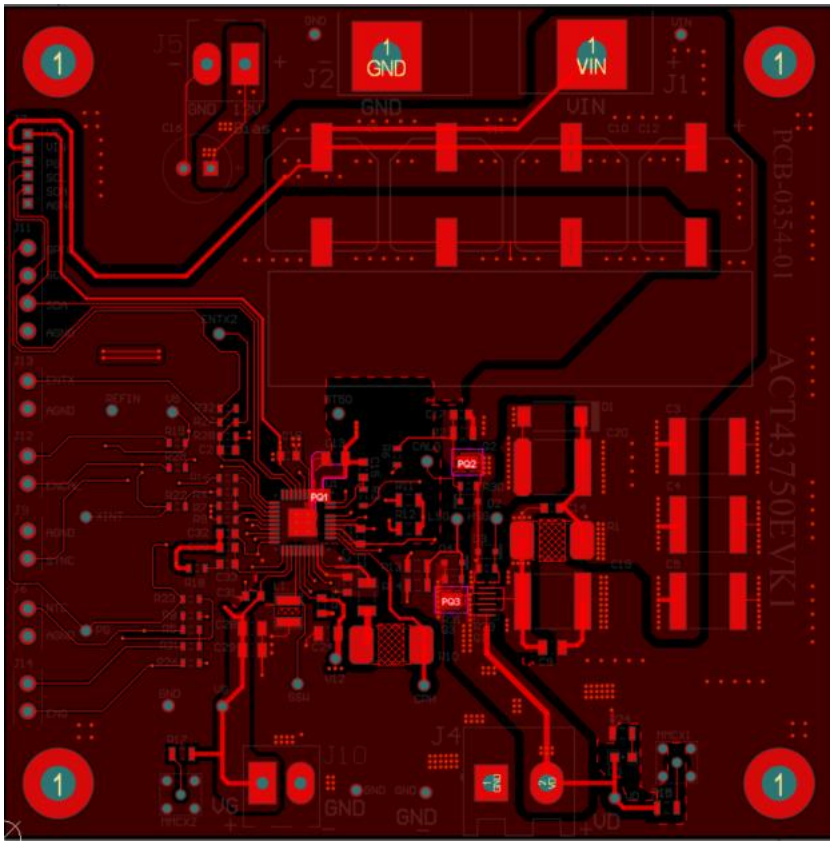


Figure 10 - Layout Top Layer

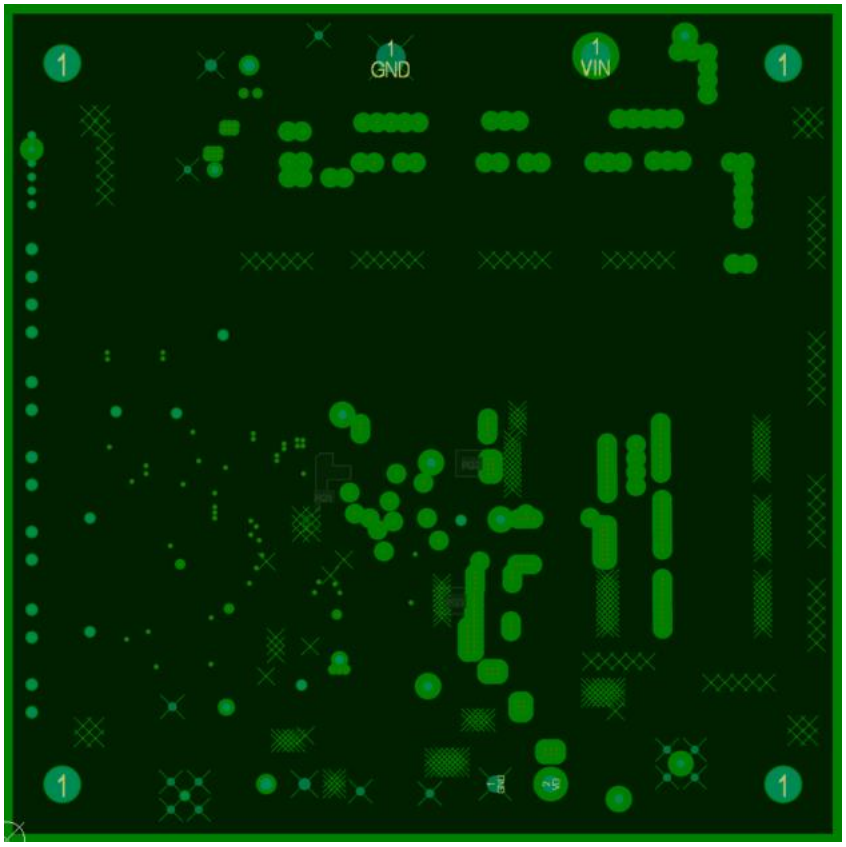


Figure 11 - Layer 2 – GND Plane

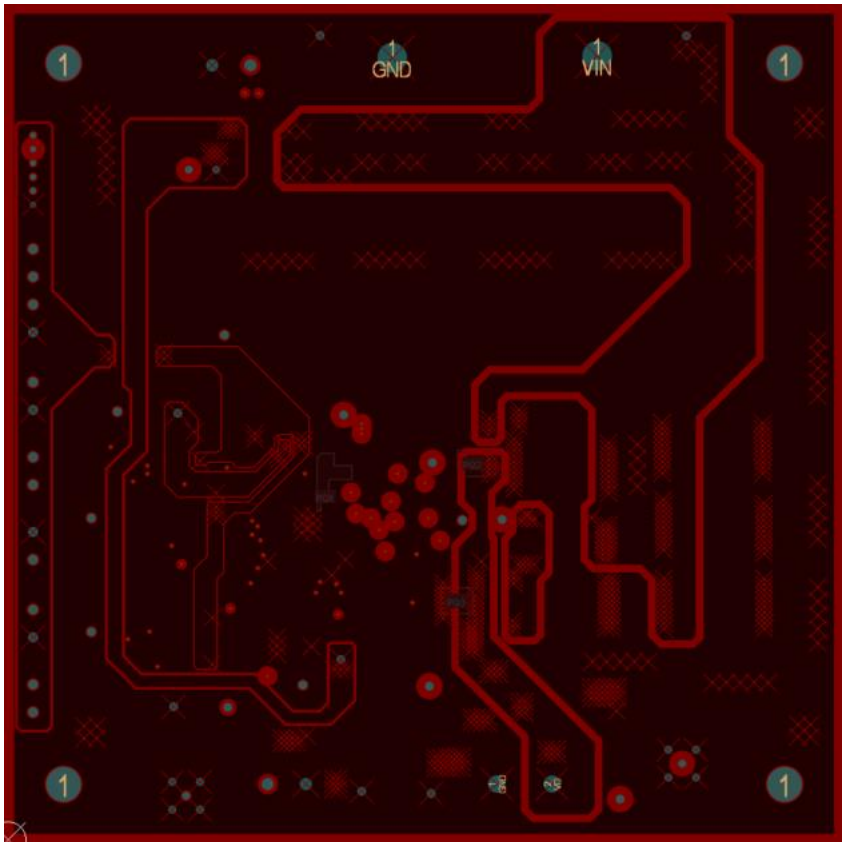


Figure 12 - Layer 3 - GND Plane

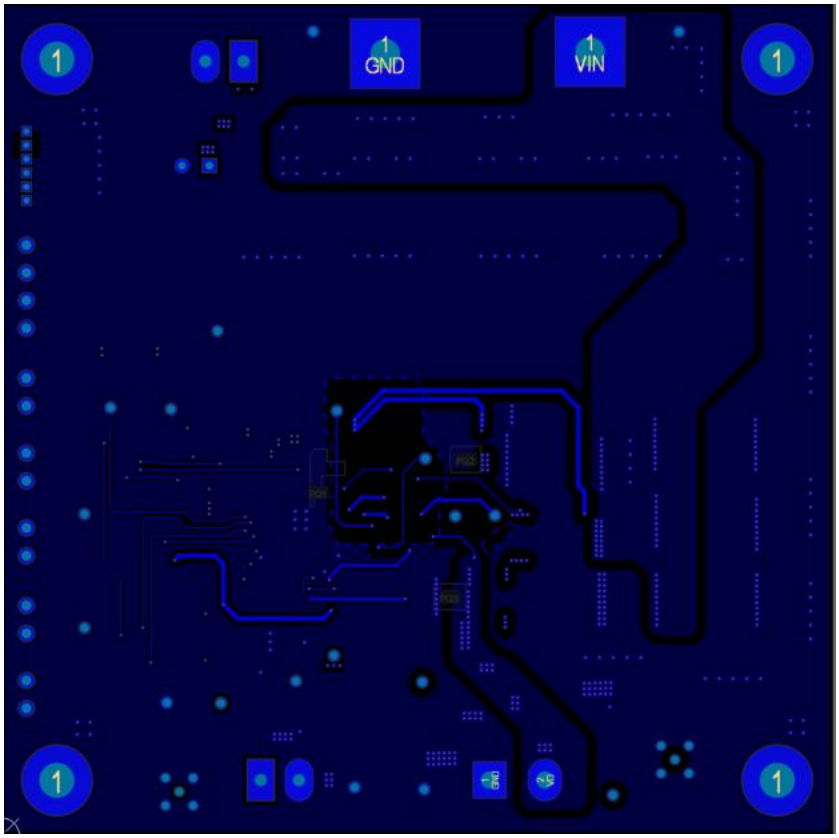


Figure 13 - Layout Bottom Layer

Bill of Materials

Description	Designator	Footprint	Part Number	Value
Capacitor, Aluminum	C1, C10, C11, C12	E-Cap_PCV_10x12.7	Nichicon PCV1K220MCL1GS or WE 875076161003	22uF/80V
Capacitor, Ceramic,	C2	C0603_H	Standard	NP
Capacitor, Aluminum	C16	WCAP-ATG5_6.3x11x2.5	WE 860130673002	22uF/50V
Capacitor, Film Cap	C3, C4, C5	C2220_Film_CAP	Rubycon 63MU335MD35750	NP
Capacitor, Film Cap	C19, C20	C2220_Film_CAP	Rubycon 63MU335MD35750	3.3uF/63V
Capacitor, Ceramic,	C9	C0805_H	Standard	0.01uF/200V
Capacitor, Ceramic,	C13	C0805_H	Murata GCM21BR72A104KA37L	100nF/100V
Capacitor, Ceramic,	C14, C15, C17	C0603_H	Standard	0.1uf/50V
Capacitor, Ceramic,	C18	C0603_H	Standard	2.2uF/16V
Capacitor, Ceramic,	C21	C0805_H	Standard	10uF/25V
Capacitor, Ceramic,	C22	C1206_H	Standard	47nF/100V
Capacitor, Ceramic,	C23	C0603_H	Standard	2.2uF/25V
Capacitor, Ceramic,	C24	C0805_H	Standard	10uF/25V
Capacitor, Ceramic,	C25	C0603_H	Standard	10nF/25V
Capacitor, Ceramic,	C29	C0805_H	Standard	NP
Capacitor, Ceramic,	C28	C0805_H	Standard	22uF/16V
Capacitor, Ceramic,	C30	C0603_H	Standard	470pF/16V
Capacitor, Ceramic,	C31	C0603_H	Standard	100nF/16V
Capacitor, Ceramic,	C32	C0603_H	Standard	2.2uF/25V
Capacitor, Ceramic,	C33	C0603_H	Standard	NP
Diode, TVS	D1	DIODE,DO-213AB	Bourns SMA6J60A-Q	66.7V Breakdown
Diode, Zener	D2, D3, D4	DIODE,SOD-523	MCC BZT52C5V1T-TP	Zener 5.1V
Diode, Led, Green	D5	WL-SMCW_0603	Rohm SMLD12EN1W	Led Green

Description	Designator	Footprint	Part Number	Value
MACHINE SCREW	H1, H2, H3, H4	Apr-40	Standard	Apr-40
CON, BANANA PLUG,RED	J1	CON, BANANA, CINCH	CINCH 108-0902-001	Banana plug red
CON, BANANA PLUG, BLACK	J2	CON, BANANA, CINCH - BLACK	CINCH 108-0903-001	Banana plug black
Connector, Screw Terminal, 5.08, 2P	J4	con,tbk,508-2p,molex-0395443002	WURTH 691236510002	5.08, 2P
Connector, Screw Terminal, 1.27, 6P	J7	con, tbk, 1.27, 6p	Sullins GRPB061VWVN-RC	1.27, 6P
Connector, Screw Terminal, 3.50, 2P	J5, J10	con,tbk,350-2p,kf350	Wurth 691214110002S	3.50, 2P
Header, Unshrouded , 2.54, Male, 2P	J6, J9, J12, J13, J14	con,hdr,254-2p	Wurth 61300211121	2.54, Male, 2P
Header, Unshrouded , 2.54, Male, 4P	J11	con,hdr,254-4p	Wurth 61300411121	2.54, Male, 4P
Inductor,	L1	L25xx_MAPI_R	Murata DFE252010F-6R8M=P2	6.8uH/1.1A
MMCX	MMCX1, MMCX2	MMCX THT	Taoglas PCB.MMCXFSTJ.HT or TE 1_1634009_0	
Test point (Red)	PT1, VIN	TSP, PROBE	Keystone Testpoint 5000	
Test point (Red)	PT7 (VD)	TSP, PROBE	Keystone Testpoint 5000	
Test point (Red)	PT10 (GSW)	TSP, PROBE	Keystone Testpoint 5001	
Test point (Red)	PT28 (VG)	TSP, PROBE	Keystone Testpoint 5000	
Test point (Black)	PT24, PT25, PT26, PT30 (GND)	TSP, PROBE	Keystone Testpoint 5001	
MOSFET, Single,	Q1	GaN, FETs, EPC2218	EPC EPC2218	100V/60A/2.4mOhm
MOSFET, Single,	Q2, Q3	GaN, FETs, EPC2016C	EPC EPC2016C	100V/18A/12mOhm
Resistor,	R1	R2512_L	Bourns CRF2512-FZ-R003ELF	0.003 Ohms 2W 1%
Resistor,	R2	R0805_H	Standard	2ohms 0.125W 1%
Resistor,	R3	R0603_H	Standard	51.1
Resistor,	R4	R0603_H	Standard	NP
Resistor,	R5	R0603_H	Standard	5K
Resistor,	R6	R0603_H	Standard	20k

Description	Designator	Footprint	Part Number	Value
Resistor,	R7	R0603_H	Standard	10k
Resistor,	R8	R0603_H	Standard	5k
Resistor,	R9	R0603_H	Standard	120K
Resistor,	R10	R2512_L	Bourns CRM2512-FX-33R00ELF	33ohms 2W 1%
Resistor,	R11	R0805_H	Standard	1k
Resistor,	R14	R0805_H	Standard	1.5k
Resistor,	R15, R17	R0805_H	Standard	0R
Resistor,	R12, R13	R0805_H	Standard	2R
Resistor,	R16	R0603_H	Standard	0R
Resistor,	R18	R0603_H	Standard	NP
Resistor,	R19, R21, R22, R23	R0603_H	Standard	10k
Resistor,	R24	R0805_H	Standard	10k
Resistor,	R25, R26, R28,	R0603_H	Standard	100k
Resistor,	R27, R32	R0603_H	Standard	0R
Resistor,	R29, R30, R31	R0603_H	Standard	10k
PCB	PCB	PCB-0354-01	Standard	PCB-0354-01
IC, ACT43750	U1	HP34_QFN37-5X5	Qorvo ACT43750-101	ACT43750-101

BOM Changes from EVK2 to EVK3

Ref Des	Old (EVK2)	New (EVK3)
C21	25V / 4.7uF / 0603	25V / 10uF / 0805
C22	100V / 100nF / 1206	100V / 47nF / 1206
R11	10R / 0805	1000R / 0805
R14	100R / 0805	1500R / 0805

Application Note 1: Safe Operation at High Drain Switching Frequency

The power loss of resistor R10 is proportional to the drain switching frequency, C22 capacitance, and drain voltage. The following formula can calculate the power loss in R10:

$$P = 0.5 * C * V^2 * F$$

Where:

P – power loss of charge pump resistor (R10).

C – charge pump capacitance. It's C22 and 47nF in ACT43750 EVK.

R – charge pump resistance. It's R10 and 33ohm in ACT43750 EVK.

F – drain switching frequency

V – drain voltage

For 50V drain and 10-kHz drain switching frequency, the power loss is: 0.588 W

For 24V drain and 1-kHz drain switching frequency, the power loss is: 0.014 W

R10 is a 2512 size resistor, and the power rating is 2W.

Application Note 2: How to Configure Bias Current and Current Limit

DC Bias Drain Current

Drain current (IDQ) is set by resistor R2 according to the formula below. This setpoint can be adjusted by +/- 31% with register 0x13. If the drain current target needs to be adjusted by more than 31%, then the calibration resistor R2 must be changed.

$$R2 = 1.5V/Idq$$

Where:

Idq – RF PA dc bias current, unit A.

R2 – Calibration resistor, unit Ω.

Drain Current Limit

Resistor R1 sets the over-current protection for the RF PA.

$$R1 = 35mV/ID$$

Where:

ID – RF PA drain current limit, unit A.

R1 – Current limit resistor, unit mΩ.

Use a Kelvin connection for the R1 current sense resistor such that V50 and CSPA are measuring across R1.

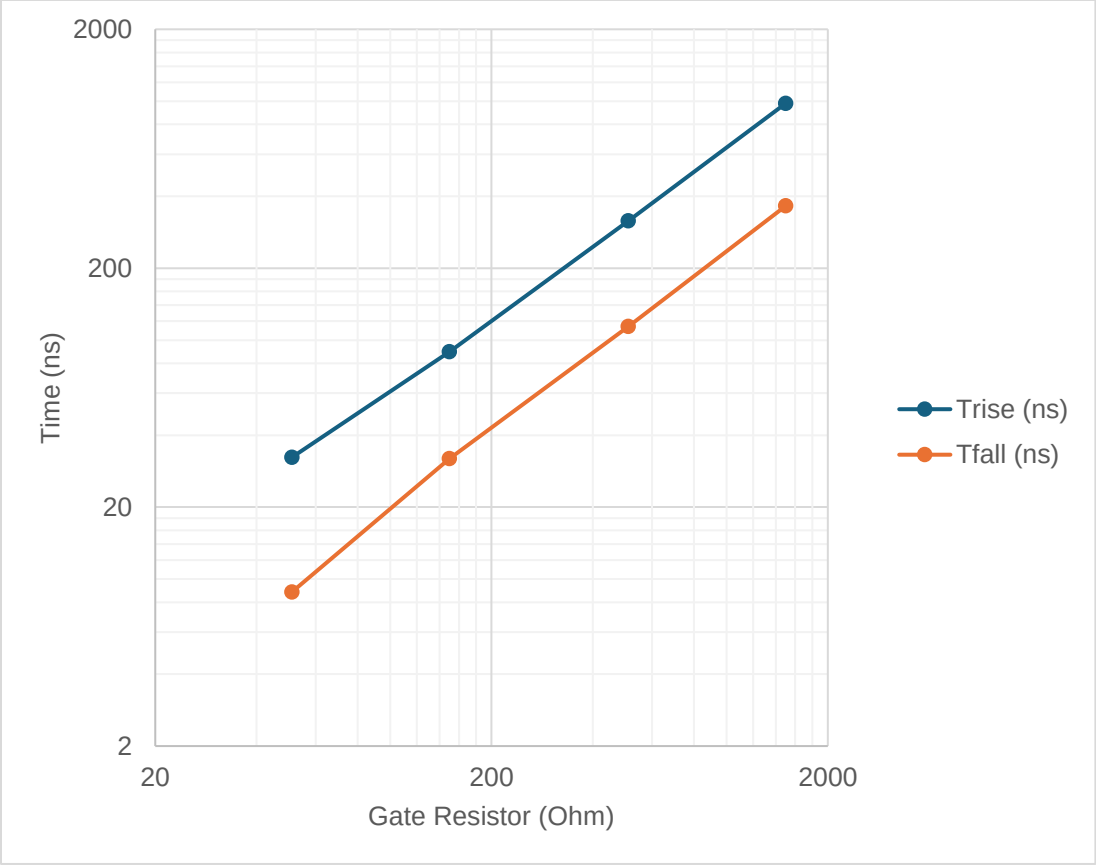
Application Note 3: How to Configure Drain Switching Time

The drain voltage, VD, switching time can be adjusted by gate resistors R11 and R14.

EVK Ref Des	Component
R11	HSGU resistor. Controls rise-time.
R14	LSGU resistor. Controls fall-time.
Q1	High-side FET. Qg will impact rise-time.
Q3	Low-side FET. Qg will impact fall-time.

- The high-side FET is EPC2218 with Qg = 10.5 nC
- The low-side FET is EPC2016C with Qg = 3.4 nC
- Rise-time and fall-time are proportional to both Qg (intrinsic to the MOSFET) and R11 / R14

The chart below illustrates the approximate relationship between R11 / R14 and the Trise / Tfall time.



Application Note 4: How to Select Dongle and GUI

Qorvo has two dongles available.

1. Old dongle is "active semi," which works with the ACT43750 Customer GUI Rev0.2.
   - Dongle connector GND is aligned with the AGND pin of J11 as shown in Figure 3.
   - GUI PWM function is available.

Old dongle connection at J11

2. Dongle is "Qorvo Rev2.0", which works with ACT43750 Customer GUI Rev0.5
   a. Version 1

   - Dongle connector on PCB needs flip 180 deg.
   - Dongle connector (black wire) is aligned with the GPIO pin of J11.
   - Silk screen GND on the top of the right corner as shown in Figure 4
   - GUI PWM function is not available.

Dongle 2.0 version 1

Dongle 2.0 version 2

   b. Version 2

   - Dongle connector on PCB doesn't need flip 180 deg.
   - Dongle connector (black wire) is aligned with the AGND pin of J11.
   - Silk screen GND at bottom of the right corner as shown in Figure 5.
   - GUI PWM function is not available.

Application Note 5: Drain Capacitance for RFPA Drain Switching Operation

Many RFPA evaluation boards are designed with a large drain capacitor to improve stability in CW. For RFPA drain switching operation, the user should calculate the inrush current of the drain switch. The following formula can calculate the inrush peak current:

$$Ipk = Cd * \frac{dVd}{dtr}$$

Where:

Ipk – RF PA drain peak current, unit A.

Cd – Drain capacitance, unit F.

Vd – Drain voltage, unit V.

tr – Rising time of the drain voltage, unit s.

For example: C=1000nF, V=50V, tr=100ns → Ipk = 500 A

To reduce inrush current, we suggest reducing the size of the drain capacitor and increasing the rise and fall times.

For example: C=150nF, V=50V, tr=600ns → Ipk = 12.5 A

The OCP threshold of ACT43750EVK3 is ~11A. EVK components R3 and C15 form a low-pass filter for the OCP measurement. This filter can allow short current spikes to pass without tripping the OCP.

Application Note 6: ACT43750 Operation without I2C

ACT43750 can operate without I2C. The enable gate, calibration, and enable/disable drain functions can be controlled by both standard GPIO inputs. The simplified startup sequence can be summarized as follows:

Power Up:

1. ENTX, ENCAL, and ENG digital input signals must be actively terminated low.
2. Apply 12V bias voltage.
3. Apply drain power supply.
4. 5V to ENG pin to turn on the gate. In EVK, put the jumper to J14. Vgate is now -4.5V.
5. 5V to ENCAL pin to perform calibration. (Note, Make sure the RF PA is connected to the ACT43750EVK.) In EVK, put the jumper on J12. The gate voltage ramps up to achieve the desired IDQ bias current. The gate voltage will keep the desired value. Remove 5V to ENCAL.
6. Apply 5V PWM signal to ENTX pin (J13) to turn on and off the drain voltage.

Power Down:

1. Turn off RF input signal.
2. Pull ENTX pin to logic low.
3. Turn off the drain power supply
4. Turn off the 12V bias voltage.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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