

APPLICATION NOTE

The QPA9121 is a wideband, high gain, and high peak power driver amplifier. With Qorvo's GaAs HBT process, this amplifier provides 27dBm P3dB with 28dB gain at 2.6GHz. With a quiescent current of 95mA the part is well suited as a driver in a Tx path DPD loop, for m-MIMO applications.

QPA9121

Stability Tune

Introduction

This document provides application information for the Qorvo® QPA9121

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

DAT.QPA9121: QPA9121 Data Sheet.

POD.QPA9121: QPA9121 Package Outline and Recommended Land Pattern Guidelines drawings.

APPLICATION NOTE: QPA9121

Description, Operation, and Control

The QPA9121 is a wideband, high gain, and high peak power driver amplifier. With Qorvo's GaAs HBT process, this amplifier provides 27dBm P3dB with 28dB gain at 2.6GHz. With a quiescent current of 95mA the part is well suited as a driver in a Tx path DPD loop, for m-MIMO applications.

The QPA9121 is internally match to 50Ω over the entire operating frequency band of 2.3-5.0 GHz and incorporates a shut-down function through the V_{PD} pin. The amplifier has been proven to provide excellent DPD correction with 5G signals as wide as 160MHz.

The QPA9121 is housed in a 16-pin 3X3mm SMT package and is footprint and pin-compatible to QPA9120.

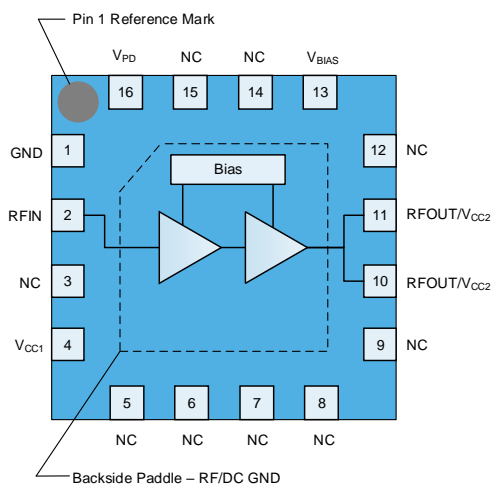


Figure 3.0. QPA9121 Block Diagram.

References: DAT.QPA9121

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Application Circuit Recommendations

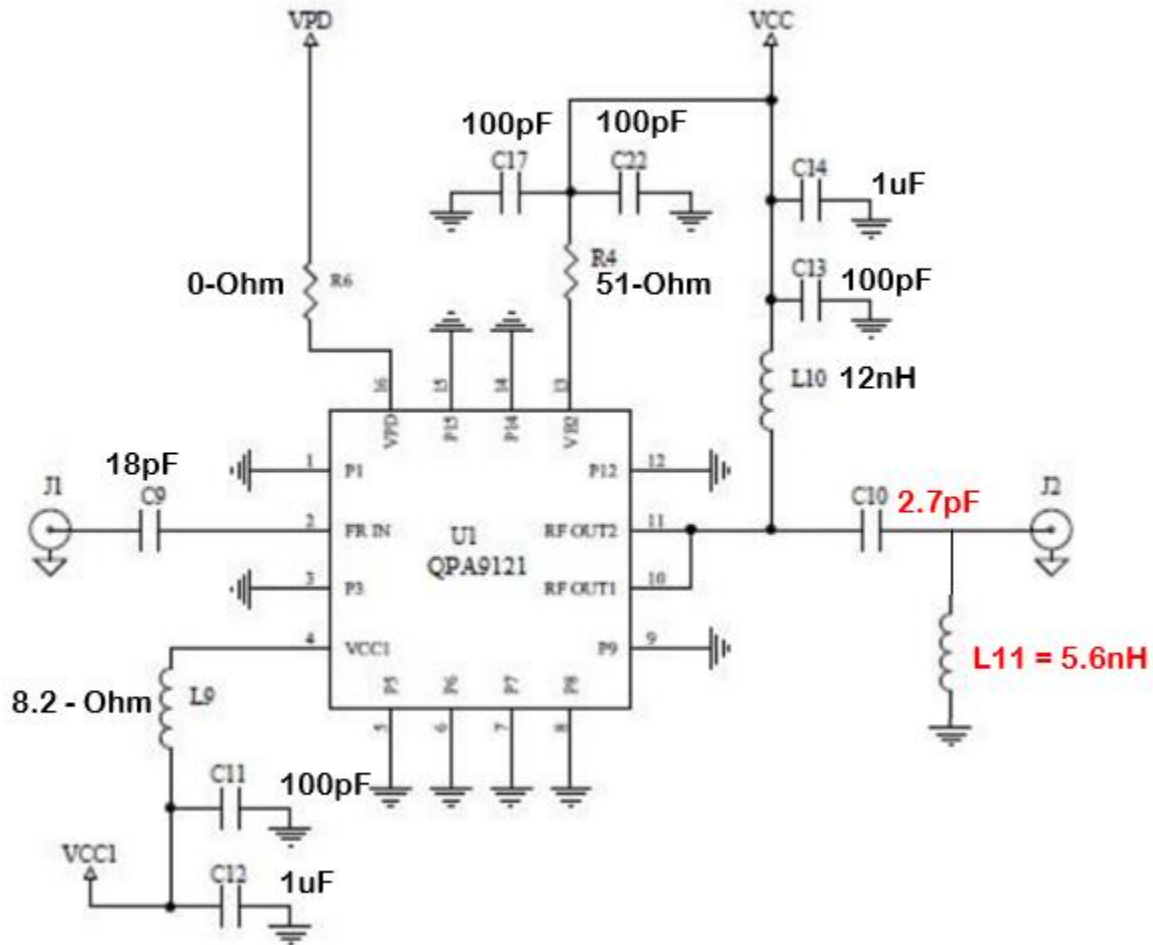


Figure 4.0. APT Application Circuit

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RF Matching

RF Input: The input matching network serves the dual purpose of providing good source impedance to the PA module and a good load for the transceiver. Transceivers are usually designed for operation into 50 Ω loads, and the PA module is designed for nominal 50 Ω source impedance at the input. The input matching network can also serve to suppress harmonic outputs from the transceiver before they reach the PA. As a starting point, the 50 Ω matching networks recommended by the transceiver or filter manufacturers should be used.

RF Outputs: To achieve optimal performance, it is almost always necessary to add a matching network between the PA RF output and the next element in the RF path, such as a duplexer or front-end-module (FEM). The RF output path should include provisions for a pi network for maximum tuning flexibility in optimizing RF performance (efficiency, ACLR, Harmonics, etc.) to meet your specific transmit chain performance requirements.

To see the effects of a relatively modest VSWR load on the PA load impedance, consider a Duplexer with an input VSWR of 1.5:1 connected to one of the PA RF output ports via a length of 50 Ω microstrip.

The load impedance presented to the PA can vary over a wide range, as defined by the ratio $Z_{MAX}/Z_{MIN} = VSWR^2 = 2.25$ for a 1.5:1 VSWR, with Z_{MAX} and Z_{MIN} given by:

$$Z_{MAX} = Z_0 \cdot VSWR = 50 \cdot 1.5 = 75 \Omega; Z_{MIN} = Z_0 / VSWR = 50 / 1.5 = 33.33 \Omega;$$

$$Z_{MAX}/Z_{MIN} = 75/33.33 = VSWR^2 = 2.25$$

The non-50 Ω load impedance seen by the PA output will alter the performance characteristics, such as linearity, efficiency, and gain. The exact impedance within the 33.33 Ω – 75 Ω range seen by the PA RF output pin will be determined by the phase shift between the duplexer and PA, which is a function of microstrip line length and operating frequency. A correctly designed matching network between the PA output and duplexer input can reduce the load VSWR to a smaller value such as 1.2:1, thereby limiting the impedance excursion Z_{MAX}/Z_{MIN} to $(1.2)^2 = 1.44$, a 64% reduction from the 2.25 VSWR in this example.

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Package Marking and Dimensions

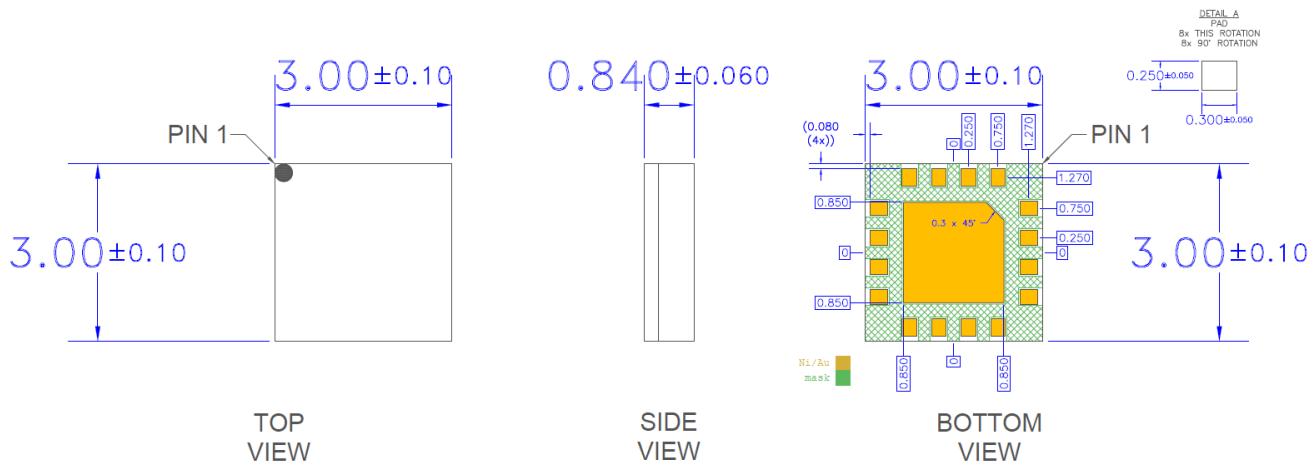


Figure 5.1 Package Marking and Dimensions

All dimensions are in millimeters. Angles are in degrees.
The terminal #1 identifier and terminal numbering conform to SPE-000677
Contact plating: ENEPIG

PCB Footprint Recommendations

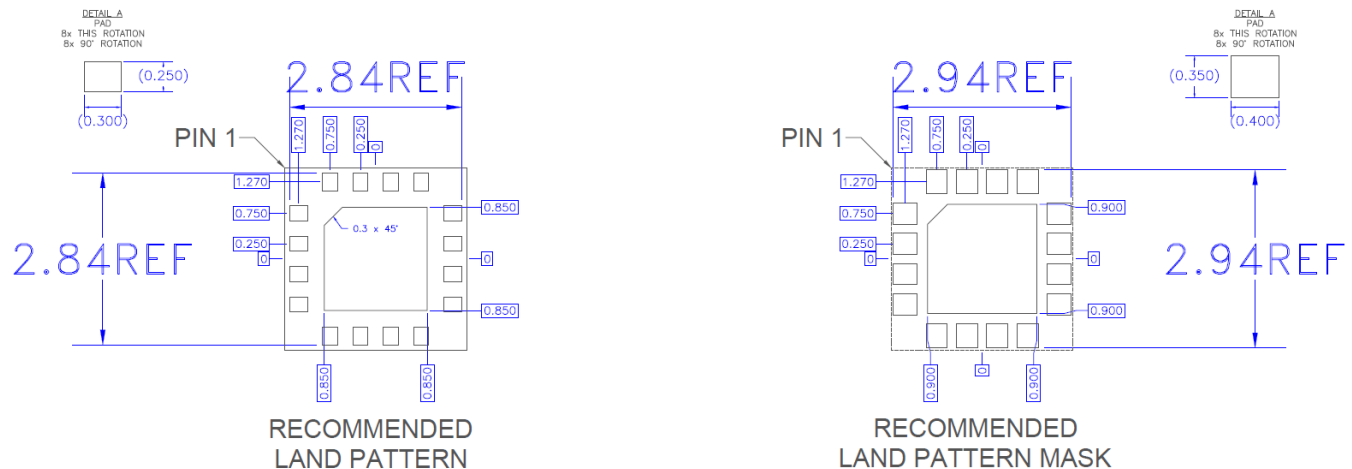


Figure 5.2 PCB Footprint Recommended Solder Mask Pattern.

Reference: POD.QM7500: QPA9121 Package Outline Drawing

All dimensions are in millimeters. Angles are in degrees.
Use 1 oz. copper minimum for top and bottom layer metal.
Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/0.0135") diameter but for drilling via holes and a final plated thru diameter of 0.25mm (0.01")
Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

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Pin Out

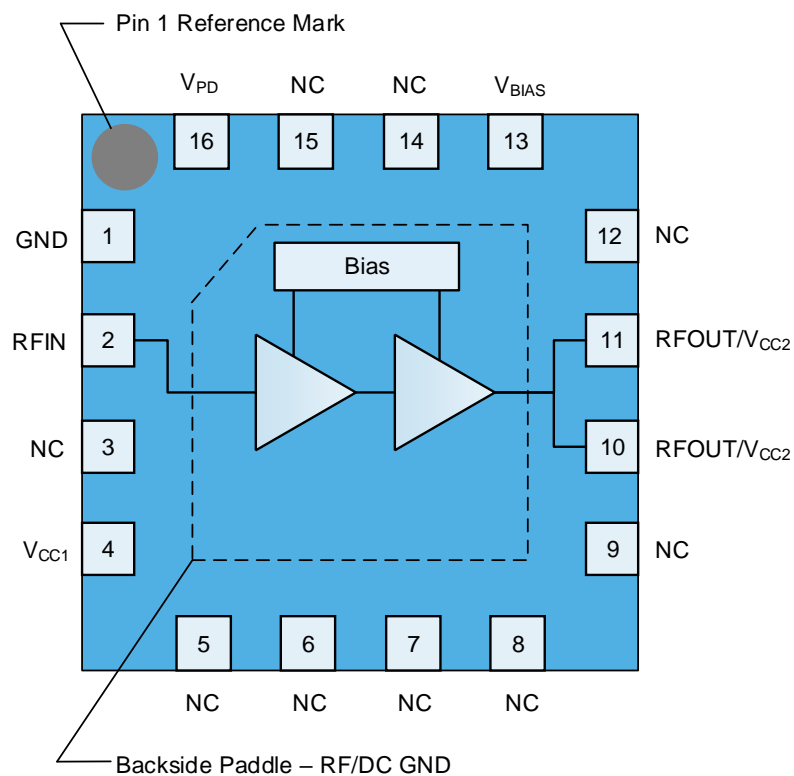


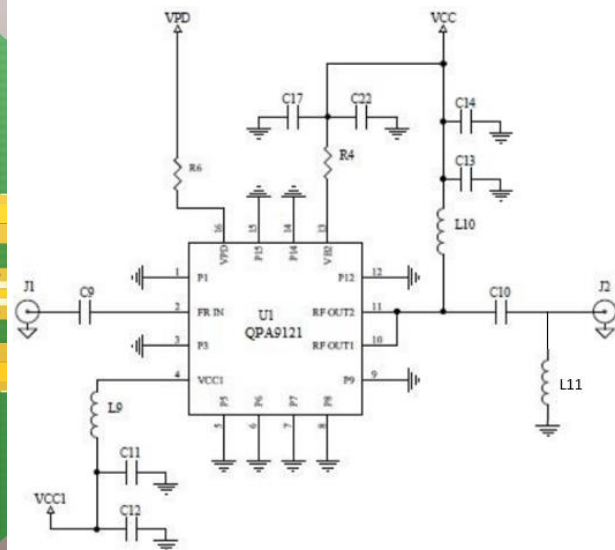
Figure 7.0. Pin Out for QPA9121.

Reference: DAT.QPA9121: QPA9121 Data Sheet

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PIN NO.	LABEL	
1	GND	Ground connection
2	RFIN	RF input. External DC block required.
3, 5, 6, 7, 8, 9, 12, 14, 15	NC	No electrical connection internally. It may be left floating or connected to ground. Land pads should be provided for PCB mounting integrity.
4	V _{CC1}	First stage DC supply.
10, 11	RFOUT / V _{CC2}	RF output and second stage DC supply. External choke and DC block capacitor required.
13	V _{BIAS}	Bias circuit supply voltage.
16	V _{PD}	PA on/off logic control.
Backside Paddle	GND	RF/DC ground connection. The back side of the package should be connected to the ground plan through as short of a connection as possible. PCB vias under the device as many as possible are recommended.
1	GND	Ground connection
2	RFIN	RF input. External DC block required.
3, 5, 6, 7, 8, 9, 12, 14, 15	NC	No electrical connection internally. It may be left floating or connected to ground. Land pads should be provided for PCB mounting integrity.
4	V _{CC1}	First stage DC supply.
10, 11	RFOUT / V _{CC2}	RF output and second stage DC supply. External choke and DC block capacitor required.
13	V _{BIAS}	Bias circuit supply voltage.
16	V _{PD}	PA on/off logic control.

Evaluation Board (EVB) Layout Assembly - QPA9121EVB01



1. Components shown on PCB layout but not on the schematic are not used.

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Evaluation Board Bill of Material

REFERENCE DES.	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
n/a	-	Printed Circuit Board	Qorvo	
U1	-	High Gain Driver Amplifier	Qorvo	QPA9121
C9	18 pF	CAP, 5%, 50V, C0G, 0402	Murata	GRM1555C1H180JA01D
C10	2.7pF	CAP		
C12, C14	1 μ F	CAP, 10V, X5R, CER, 0402	Various	
C11, C13, C17, C22	100 pF	CAP, 5%, 50V, C0G, 0402	Murata	GRM1555C1H101JA01D
R4	51 Ω	RES, 5%, 1/16W, 0402	Various	
R6	0 Ω	RES, 1/10W, 0402	Various	
L9	8.2 Ω	RES, 5%, 1/16W, 0402	Various	
L10	12 nH	IND, 5%, 0402	Coilcraft	0402CS-12NXJLW
L11	5.6nH	IND		
J1, J2	-	Conn, SMA F STRT .062"	Cinch Connectivity	142-0701-851
R5, R7	DNP	n/a	n/a	n/a
n/a	-	Printed Circuit Board	Qorvo	
U1	-	High Gain Driver Amplifier	Qorvo	QPA9121
C9, C10	18 pF	CAP, 5%, 50V, C0G, 0402	Murata	GRM1555C1H180JA01D
C12, C14	1 μ F	CAP, 10V, X5R, CER, 0402	Various	

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Support Data

The Qorvo Factory Applications Engineering team has extensively characterized the QPA9121, including the generation of output load pull data. Output load pull data shows the part performance for a wide range of output load impedances, and is an extremely useful design aid. This data along with other performance data to facilitate design in a particular application is available by request.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

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