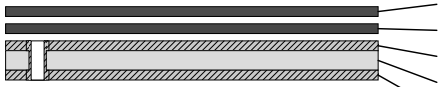
SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD

SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

LAYER STACK LEGEND



Material	Layer	Thickness	Dielectric Material	Type	Comment
	SILKSCREEN_TOP			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
Copper	**METAL1_TOP**	**0.0014in**		**Signal**	**FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**
Core		*0.0080in*	*RO4003*	*Dielectric*	
Copper	**METAL2_BOT**	**0.0014in**		**Signal**	**FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**

Finished board thickness: 0.0112in

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
   METAL 1 (TOP) AND METAL 2 (BOTTOM):
   ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
   ELECTROLESS NICKEL per IPC-4552, 118 - 236µin. (3 - 6µm)
   IMMERSION GOLD per IPC-4552, 3 - 10 µin (0.08 - 0.25µm)
4. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) +/- 10%
5. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM).
   COPPER TO EDGE AT RF CONNECTORS IS CRITICAL FOR PERFORMANCE.
6. TOLERANCE: PC BOARD OUTLINE: ±0.003in.THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
7. BURRS SHALL NOT EXCEED 0.002in.
8. VIA PLATING/FILLING:
   VIAS UNDER DUT ARE TO BE COPPER FILLED OVER PLATED AND PLANERIZED.
   ALL OTHER PLATED THRU HOLES ARE TO BE PLATED TO 0.0007 ± 0.0004in. MIN. THICKNESS.
9. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
10. NO ELECTRICAL TEST NEEDED.
11. NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
14. DELIVER BOARDS BAGGED AS: SINGLES

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 302583		
TOLERANCES .XX = ±.01 .XXX = ±.005 .XXXX = ±.0010 ANGLES = ± 0.5°	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE
	DESIGNER	B.HUFFIN	10/12/2022
	ENGR.	Z.DU	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION	CAGE CODE	1CVM1	
DO NOT SCALE DRAWING			

EAR

WARNING - THIS DOCUMENT CONTAINS TECHNICAL DATA WHOSE EXPORT IS UNDER CONTROL OF THE UNITED STATES DEPARTMENT OF COMMERCE UNDER THE EXPORT ADMINISTRATION REGULATIONS (15 CFR 730-774). DIVERSION CONTRARY TO U.S. LAW IS PROHIBITED. INFORMATION AND GUIDANCE ON EXPORT CONTROL REQUIREMENTS CAN BE FOUND AT www.BIS.doc.GOV

TITLE:
QPA0524 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA0524-4000	N/A	A

SHEET 1 OF 6 | CAD: ALTIUM DESIGNER | SCALE: 2:1

Current Date & Time: 10/12/2022 3:24

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