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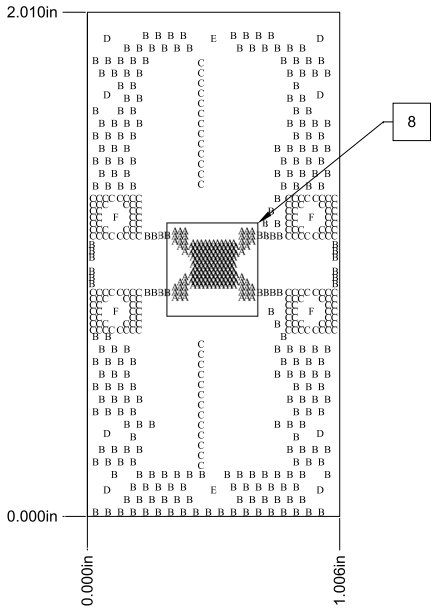
LAYER STACK LEGEND

Material	Layer	Thickness	Dielectric Material	Type	Comment
	Top Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
Surface Material	Top Solder	0.0004in	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
Copper	**Top Layer**	**0.0014in**		**Signal**	**FINISH THICKNESS = 0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**
Core		*0.0080in*	*RO4003C*	*Dielectric*	
Copper	**Bottom Layer**	**0.0014in**		**Signal**	**FINISH THICKNESS = 0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**

Total thickness: 0.0112in

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
   METAL 1 (TOP) AND METAL 2 (BOTTOM):
   ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
   ELECTROLESS NICKEL per IPC-4552, 118 - 236µin. (3 - 6µm)
   IMMERSION GOLD per IPC-4552, 3 - 10 µin (0.08 - 0.25µm)
4. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) ±10%
5. COPPER IS PULLED BACK 0.003in. GROUND PLANE ONLY FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM). NO PULL BACK ON TAPER. THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
6. TOLERANCE: PC BOARD OUTLINE: ±0.005in.
7. BURRS SHALL NOT EXCEED 0.002in.
8. VIA PLATING/FILLING:
   A. ALL 0.006in VIAS UNDER THE DUT ARE TO BE COPPER-FILLED, OVER-PLATED AND PLANARIZED. FINISHED COPPER THICKNESS TO BE 0.0014 ± 0.0004in.
   B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007 ± 0.0004in. MIN. THICKNESS.
9. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
10. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
11. ALL HOLES TO BE LOCATED WITHIN ±0.001 OF CAD DATABASE.
12. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
13. DELIVER BOARDS BAGGED AS: SINGLES
14. NO ELECTRICAL TEST NEEDED.



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair
A	193	0.0060	Plated	Top Layer - Bottom Layer
B	259	0.0100	Plated	Top Layer - Bottom Layer
C	186	0.0120	Plated	Top Layer - Bottom Layer
F	4	0.0900	Plated	Top Layer - Bottom Layer
D	8	0.1000	Plated	Top Layer - Bottom Layer
E	2	0.1200	Plated	Top Layer - Bottom Layer
	652 Total			

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES

INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009

THIRD ANGLE PROJECTION

DO NOT SCALE DRAWING

SAP MATERIAL NUMBER: 302727

APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE

		DATE
DESIGNER	T. THOMAS	11-28-22
ENGR.	P. LITMANEN	

PDE CONTROLLED

TITLE: QPA1111 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA1111-4000	N/A	A

SHEET 1 OF 5 | CAD: ALTIUM DESIGNER | SCALE: 2:1

Current Date & Time: 12/1/2022 10:40

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ASSEMBLY NOTES:

15. WORKMANSHIP & SOLDER PER IPC-A-610C, CLASS 2.
16. QORVO DEVICES (DUT) MAY REQUIRE BAKING PER IPC/JEDEC J-STD-020 FOR A MINIMUM OF 24 HOURS AT 125 +5/-0 DEGREES C. ASSEMBLY MUST TAKE PLACE WITHIN 12 HOURS OF BAKE COMPLETION.
17. MANUFACTURERS' PART NUMBERS ARE SUBJECT TO CHANGE BY THE MANUFACTURERS FOLLOWING THE ISSUE OF THIS DOCUMENT, AND ARE THEREBY INCLUDED FOR REFERENCE ONLY. CONTACT QORVO CORORATE ENGINEERING MATERIALS WITH QUESTIONS REGARDING SPECIFIC MANUFACTURERS' PART NUMBERS.
18. TAKE CARE NOT TO ADD TOO MUCH SOLDER WHEN ASSEMBLING J1 AND J2 (IF PRESENT).

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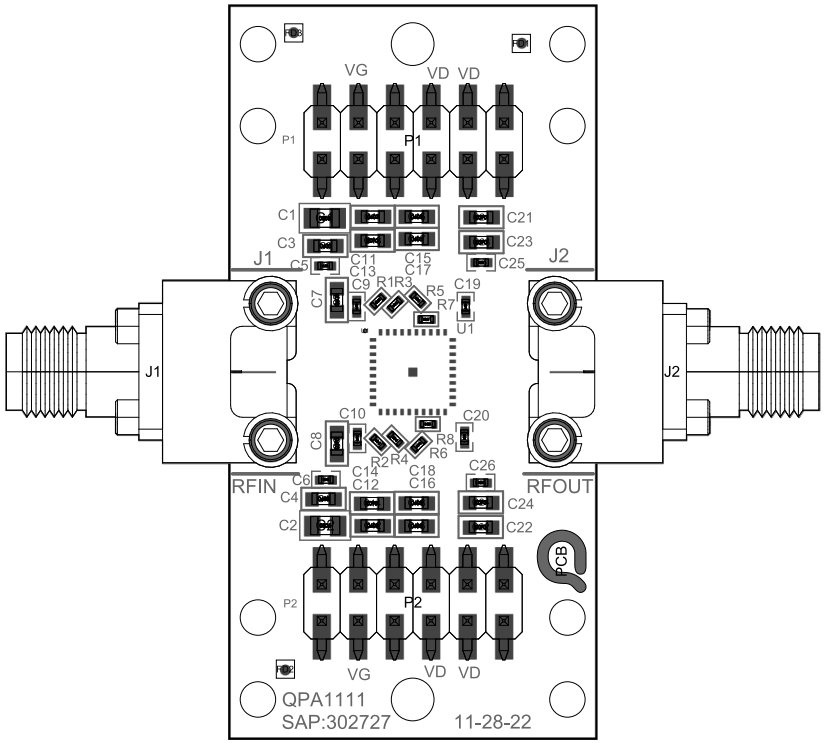

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 302727		
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE
	DESIGNER	T. THOMAS	11-28-22
	ENGR.	P. LITMANEN	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION			
DO NOT SCALE DRAWING			

qorvo™

TITLE: QPA1111 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA1111-4000	N/A	A

SHEET 2 OF 5	CAD: ALTIUM DESIGNER	SCALE: 2:1

Current Date & Time: 12/1/2022 10:40

FOR-001324 REV D