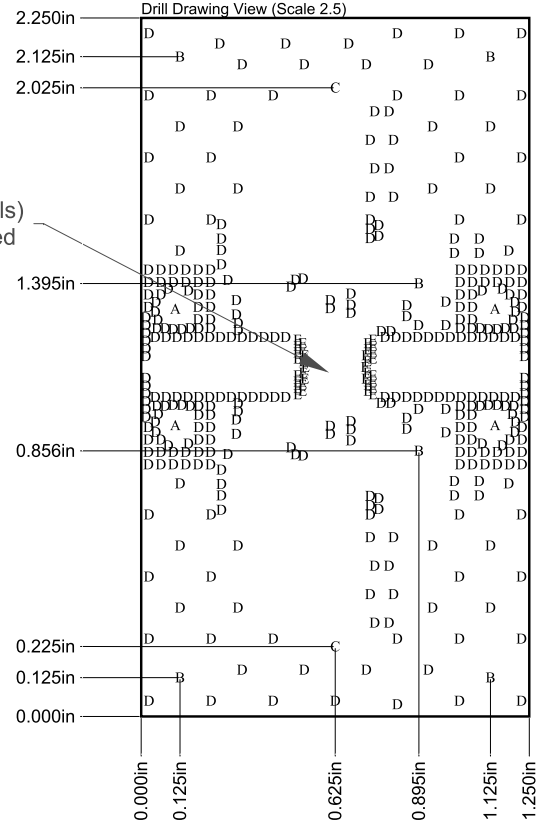
SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD

SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
   A. METAL 1(TOP) AND METAL 4(BOTTOM):
   ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
4. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) ±10%
5. CONTROLLED IMPEDANCE:
   TARGET IMPEDANCE: 50 OHMS
   MICROSTRIP LAYER: 1
   IMPEDANCE TEST PER IPC-TM-650. IMPEDANCE TEST DATA TO BE DELIVERED WITH EACH LOT.
6. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 4 (BOTTOM)METAL TO EDGE IS NECESSARY. THE PRODUCT PERFORMANCE IS SIGNIFICANTLY COMPROMISED WITH LARGE PULL BACKS. WE WILL ACCEPT BURRS.
7. TOLERANCE: PC BOARD OUTLINE:
   A. PC BOARD OUTLINE: ±0.003in.TOLERANCE AND IS CRITICAL TO RF PERFORMANCE
8. SINGULATION: EXTERNAL OF OUTLINE ARE TO BE COMPLETED VIA OPTICAL (LENZ) ROUTING OR LASER TO ACHEIVE PCB OUTLINE TOLERANCE. LASER ROUTING IS AUTHORIZED ONLY IF IT YIELDS A NON-CONTAMINATED SURFACE ADJACENT TO THE LASER-SAWN EDGE.
9. METAL TO EDGE IS NECESSARY. THE PRODUCT PERFORMANCE IS SIGNIFICANTLY COMPROMISED WITH LARGE PULL BACKS. WE WILL ACCEPT BURRS.
10. BURRS SHALL NOT EXCEED 0.002in.
11. VIA PLATING/FILLING:
    A. ALL VIAS ARE TO BE EPOXY-FILLED, OVER-PLATED AND PLANARIZED
    B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007 ± 0.0004in. MIN. THICKNESS.
12. METAL 1(TOP) AND METAL4(BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
13. FINISHED Cu THICKNESS TO BE .0018 ± .0005.
14. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
15. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
16. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
17. NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
18. BOARDS TO BE SINGLULATED PER MECHANICAL 3 (OUTLINE) AND DELIVERED AS SINGLES
19. NO ELECTRICAL TEST IS NEEDED
20. FLATNESS AT COIN AREA TO BE FLUSH TO METAL 1 -0.000 TO +0.0014 PROTRUSION.
21. FLATNESS AT COIN AREA TO BE FLUSH TO METAL 4 WITHIN +0.0014/-0.001.
22. COPPER COIN APERTURE TO BE EDGE PLATED. METAL 1 AND METAL 4 TO BE PLATED COMPLETELY ALONG COPPER APERTURE EDGE
23. COPPER COIN MATERIAL: OXYGEN FREE HIGH CONDUCTIVITY COPPER UWS CDA 101, 102, OR 103, ASTM B187, ASTM B152.
24. PLATING BETWEEN COPPER COIN AND METAL 1 & METAL 4 TO BE CONTINUOUS, (UNINTERRUPTED). IF A SCALLOPED COIN IS USED, GAPS BETWEEN COIN AND PCB MUST BE FILLED.
25. TOP OF COPPER COIN TO BE PLATED TO METAL 1. BOTTOM OF COIN TO BE PLATED TO METAL 4.

Drill Drawing View (Scale 2.5)



Notes 20 - 25:
Copper Coin (168mils X 72mils)
To Be Placed Where Inidicated
And Plated Over

REFERENCE NOTE: Uses QPA0017-4000[1] CAL SAP No. 301001

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 303237	
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE	DATE
	DESIGNER: OMARRUFO	12/9/2022
	ENGR.: D.WOHLERT	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED	
THIRD ANGLE PROJECTION		
DO NOT SCALE DRAWING		

TITLE: QPA0015 EVALUATION PCB DESIGN PACKAGE

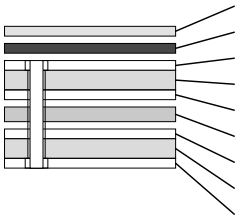
SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA0015-4000	N/A	A

SHEET 1 OF 5 | CAD: ALTIUM DESIGNER | SCALE: 2:1

Current Date & Time: 12/13/2022 3:28

FOR-001324 REV D

LAYER STACK LEGEND_(COPPER THICKNESS IS ~ FINISHED THICKNESS)



Material	Layer	Thickness	Dielectric Material	Type	Note
	Top Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
Surface Material	Top Solder	0.0010in	Solder Resist	Solder Mask	LPI OR LDI, GREEN, MAX FINISH THICKNESS TO BE 0.001in.
Copper	**METAL1_TOP**	**0.0020in**		**Signal**	**0.5oz. (Plus Plating)**
Core		*0.0100in*	*TACONICS RF-35HTC*	*Dielectric*	
Copper	**METAL2_MID1**	**0.0006in**		**Signal**	
Prepreg		*0.0085in*	*370HR*	*Dielectric*	
Copper	**METAL3_MID2**	**0.0006in**		**Signal**	
Core		*0.0100in*	*370HR*	*Dielectric*	
Copper	**METAL4_BOT**	**0.0020in**		**Signal**	**0.5oz. (Plus Plating)**

Total thickness: 0.0347in

NOTE: LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE)

Drill Table (HOLE SIZES ARE DRILLED SIZE)

Symbol	Count	Hole Size	Plated	Drill Layer Pair
E	34	7.00mil(0.18mm)	Plated	METAL1_TOP - METAL4_BOT
D	360	10.00mil(0.25mm)	Plated	METAL1_TOP - METAL4_BOT
A	4	95.00mil(2.41mm)	Plated	METAL1_TOP - METAL4_BOT
B	6	100.00mil(2.54mm)	Plated	METAL1_TOP - METAL4_BOT
C	2	120.00mil(3.05mm)	Plated	METAL1_TOP - METAL4_BOT
	406 Total			

SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA0015-4000	N/A	A
SHEET 2 OF 5	CAD: ALTIUM DESIGNER		SCALE:	2:1

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