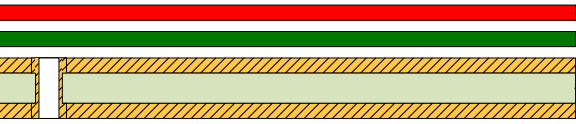


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SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM


LAYER STACK LEGEND

	Material	Layer	Thickness	Dielectric Material	Type	Comment
		SILKSCREEN_TOP			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
	Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
	Copper	METAL1_TOP	0.0014in		Signal	FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH
	Core		0.0100in	ROGERS 4350	Dielectric	
	Copper	METAL2_BOT	0.0014in		Signal	FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH
Finished board thickness: 0.0132in						

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
FABRICATE IN ACCORDANCE WITH IPC-6018, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
METAL 1 (TOP) AND METAL 2 (BOTTOM):
ENEPIG (ELECTROLESS NICKEL ELECTROLESS PALLADIUM IMMERSION GOLD):
ELECTROLESS NICKEL per IPC-4556, 118 - 236µin. (3 - 6µm)
ELECTROLESS PALLADIUM per IPC-4556, 2 - 12µin. (0.0508 - 0.3048µm)
IMMERSION GOLD per IPC-4556, 1.2 µin min(0.03048µm)
4. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) +/- 10%
5. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM).
COPPER TO EDGE AT RF CONNECTORS IS CRITICAL FOR PERFORMANCE.
6. TOLERANCE: PC BOARD OUTLINE: ±0.003in.THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
7. BURRS SHALL NOT EXCEED 0.002in.
8. VIA PLATING/FILLING:
VIAS ARE TO BE EPOXY FILLED OVER PLATED AND PLANERIZED.
ALL OTHER PLATED THRU HOLES ARE TO BE PLATED TO 0.0008 ± 0.0004in. MIN. THICKNESS.
9. CONTROLLED IMPEDANCE: CPW LAYER 1 TRACES ARE 0.015+/- 0.001, REF LAYER 2. TARGET IMPEDANCE IS 50 OHMS
+/-5%. TARGET FREQUENCY 6GHz. CORE DIELECTRIC CAN BE ADJUSTED TO OBTAIN FINISHED THICKESS. GERBER
DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENT TO BE
DONE BY PCB FABRICATOR.
10. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
11. NO ELECTRICAL TEST NEEDED.
12. NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
13. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
14. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
15. DELIVER BOARDS BAGGED AS: SINGLES

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

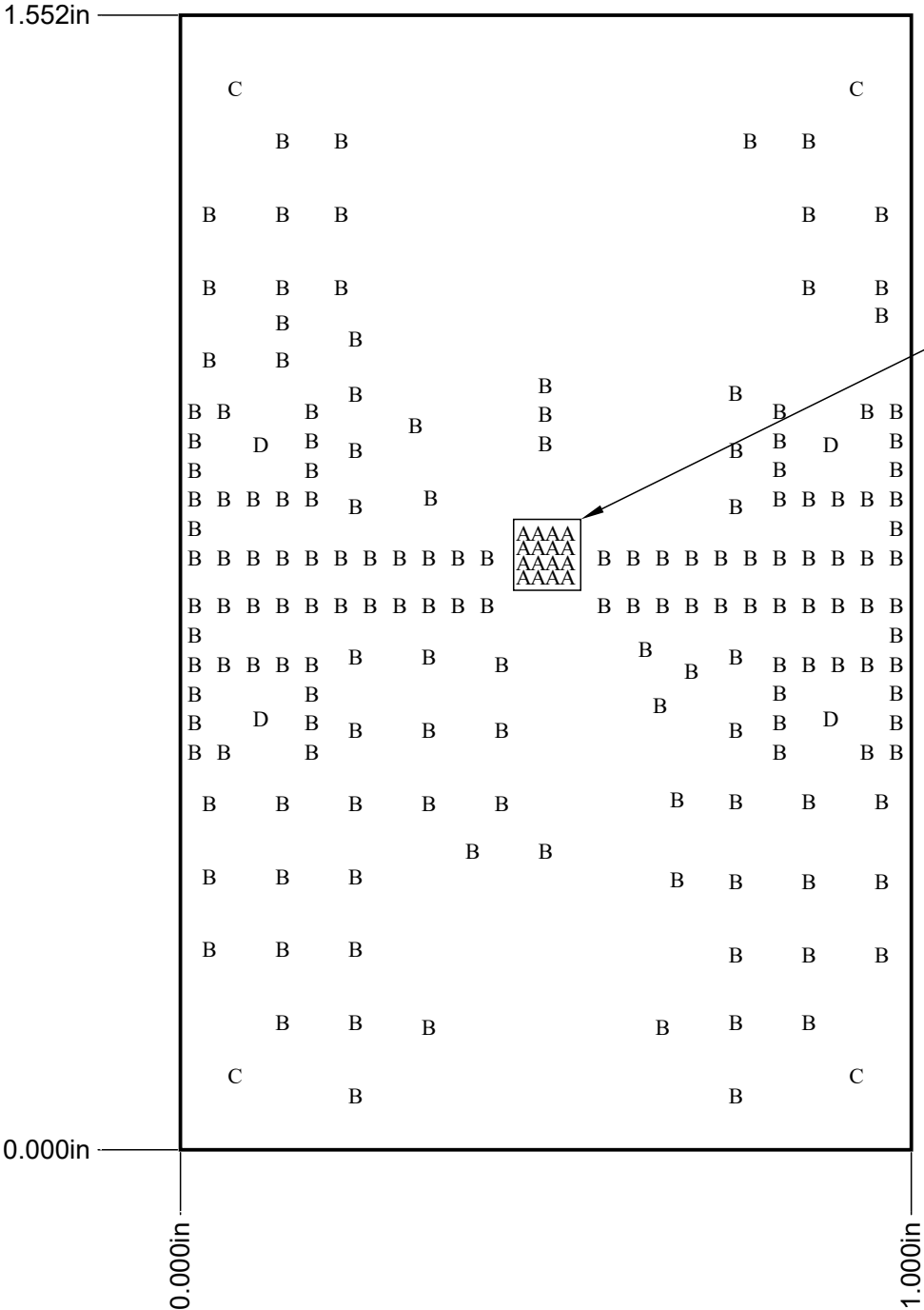
EAR	WARNING - THIS DOCUMENT CONTAINS TECHNICAL DATA WHOSE EXPORT IS UNDER CONTROL OF THE UNITED STATES DEPARTMENT OF COMMERCE UNDER THE EXPORT ADMINISTRATION REGULATIONS (15 CFR 730-774). DIVERSION CONTRARY TO U.S. LAW IS PROHIBITED. INFORMATION AND GUIDANCE ON EXPORT CONTROL REQUIREMENTS CAN BE FOUND AT www.BIS.doc.GOV			PDE CONTROLLED		SIZE B	DOCUMENT NUMBER: QPA0023D-4000	PROTOTYPE INSTANCE: N/A	REV. A
		THIRD ANGLE PROJECTION		CAGE CODE 1CVM1	SHEET 1 OF 7	CAD: ALTIUM DESIGNER	SCALE: 2:1		
		DO NOT SCALE DRAWING							

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Drill Table

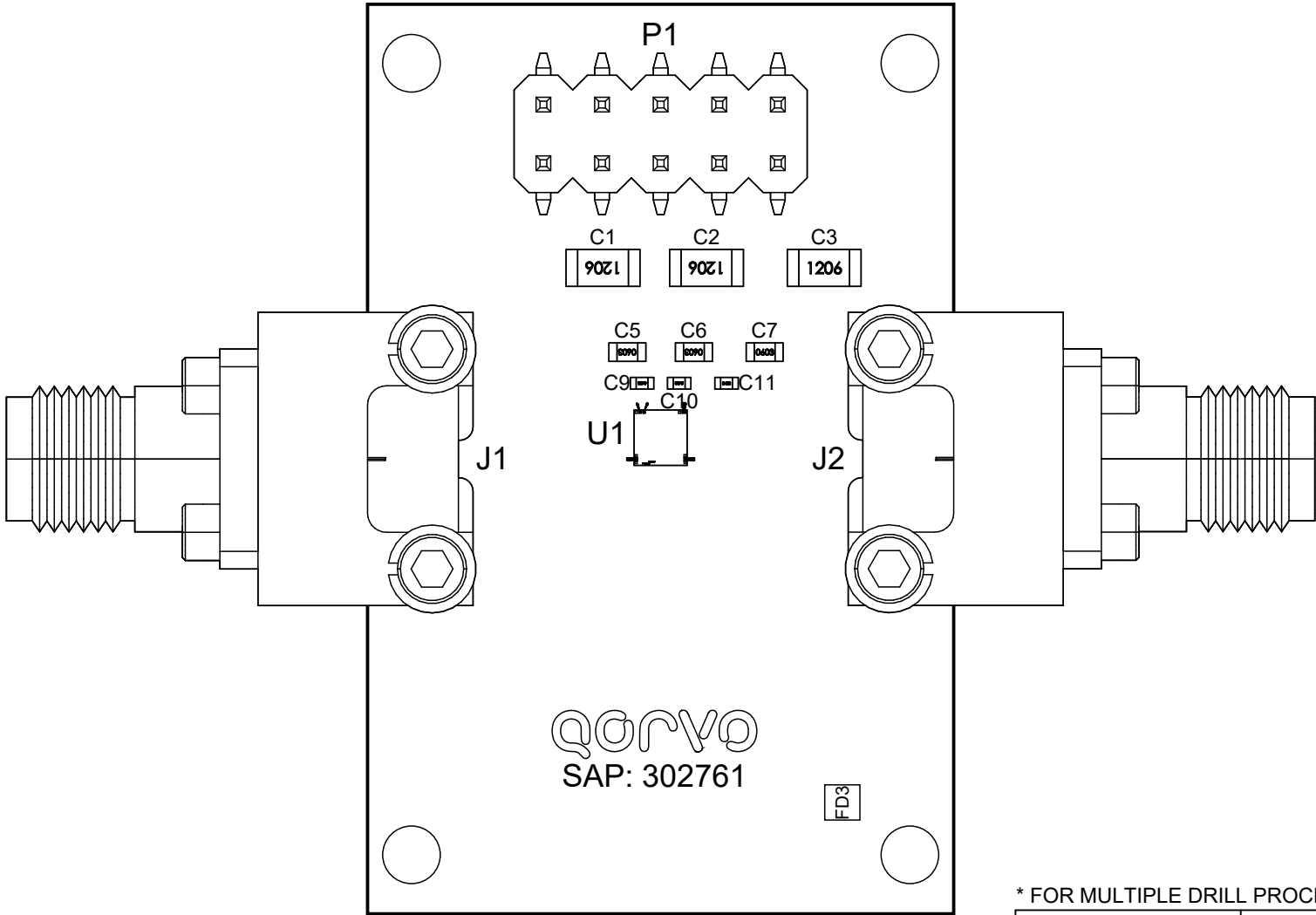
Symbol	Count	Hole Size	Plated	Drill Layer Pair
A	16	0.008	Plated	METAL1_TOP - METAL2_BOT
B	169	0.015	Plated	METAL1_TOP - METAL2_BOT
D	4	0.095	Plated	METAL1_TOP - METAL2_BOT
C	4	0.100	Plated	METAL1_TOP - METAL2_BOT
	193 Total			

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		B	1CVM1		QPA0023D-4000	N/A	A
		SHEET 2 OF 7		CAD: ALTIUM DESIGNER		SCALE:	2:1

ASSEMBLY NOTES:


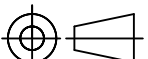
- 16. WORKMANSHIP & SOLDER PER IPC-A-610C, CLASS 2.
- 17. MANUFACTURERS' PART NUMBERS ARE SUBJECT TO CHANGE BY THE MANUFACTURERS FOLLOWING THE ISSUE OF THIS DOCUMENT, AND ARE THEREBY INCLUDED FOR REFERENCE ONLY. CONTACT QORVO CORORATE ENGINEERING MATERIALS WITH QUESTIONS REGARDING SPECIFIC MANUFACTURERS' PART NUMBERS.
- 18. QORVO DEVICES (DUT) MAY REQUIRE BAKING PER IPC/JEDEC J-STD-020 FOR A MINIMUM OF 24 HOURS AT 125 +5/-0 DEGREES C. ASSEMBLY MUST TAKE PLACE WITHIN 12 HOURS OF BAKE COMPLETION.
- 19. LOW TEMP SOLDER SHALL BE USED FOR ALL SMDs AND PRE-TINNING WHEN REQUIRED.
- 20. LEAD FREE (HIGH TEMP) SOLDER SHALL BE USED FOR SMA AND EDGE MOUNT CONNECTORS.

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* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

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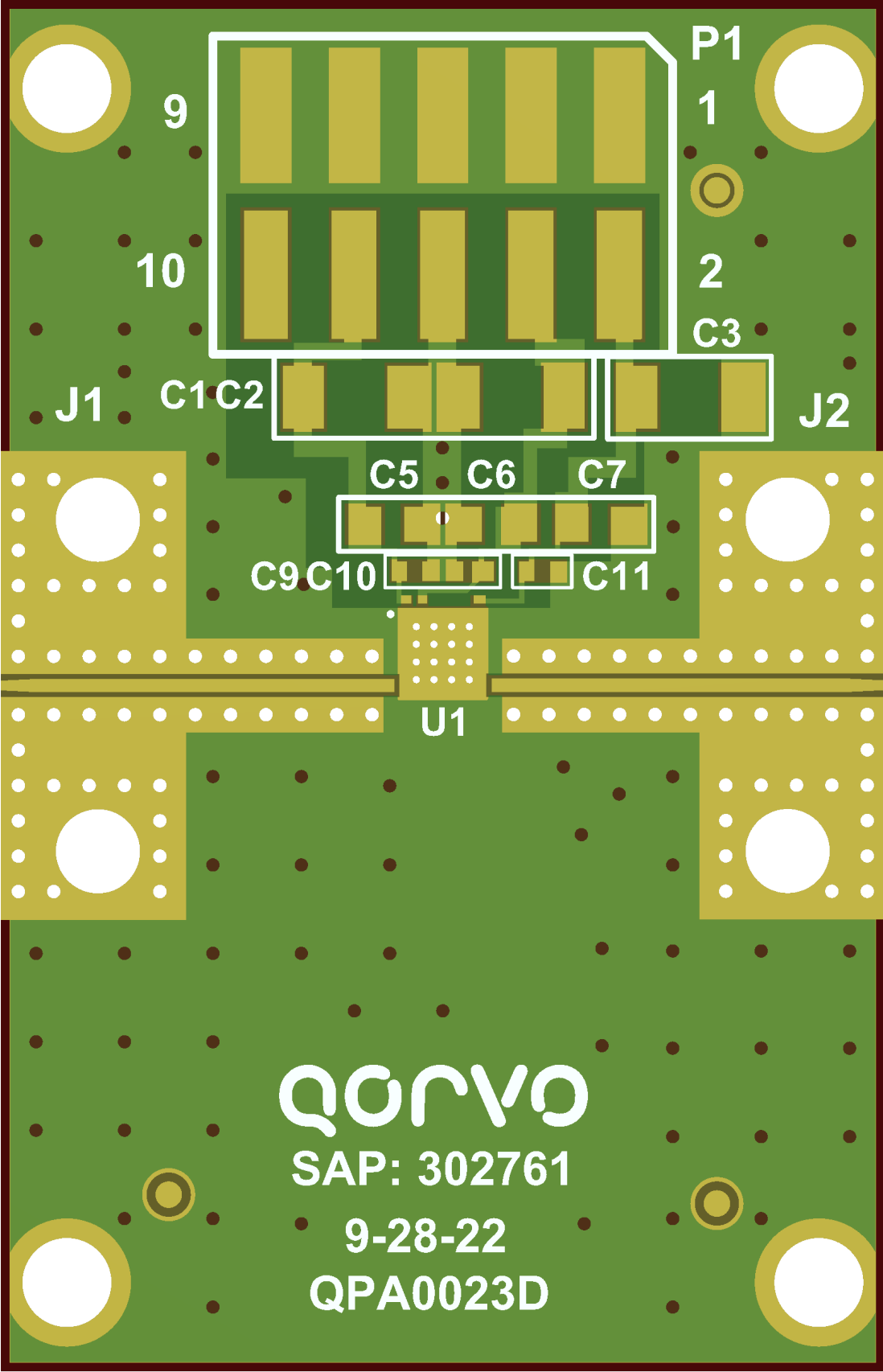
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES		SAP MATERIAL NUMBER: 302761					
TOLERANCES .XX = ±.01 .XXX = ±.005 .XXXX = ±.0010 ANGLES = ± 0.5°		APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE				DATE 10/27/2022	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009		DESIGNER	B.HUFFIN	TITLE: QPA0023D EVALUATION PCB DESIGN PACKAGE			
		ENGR.	M.KELLY				
 THIRD ANGLE PROJECTION DO NOT SCALE DRAWING		PDE CONTROLLED		SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
		CAGE CODE	1CVM1	B	QPA0023D-4000	N/A	A
				SHEET 3 OF 7		CAD: ALTIUM DESIGNER	
						SCALE: 2:1	

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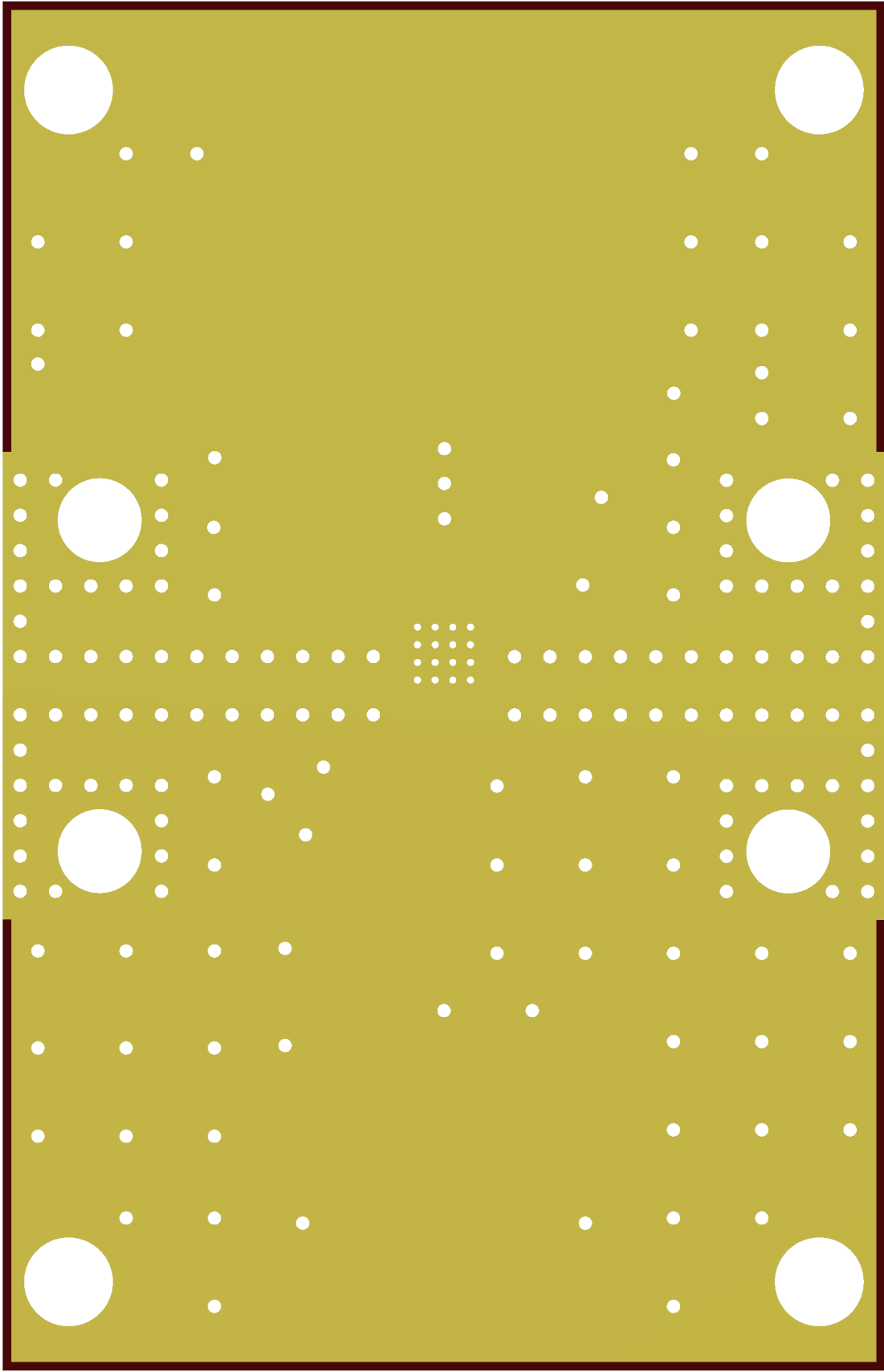
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					SHEET 4 OF 7			CAD: ALTIUM DESIGNER	
								SCALE: 2:1	

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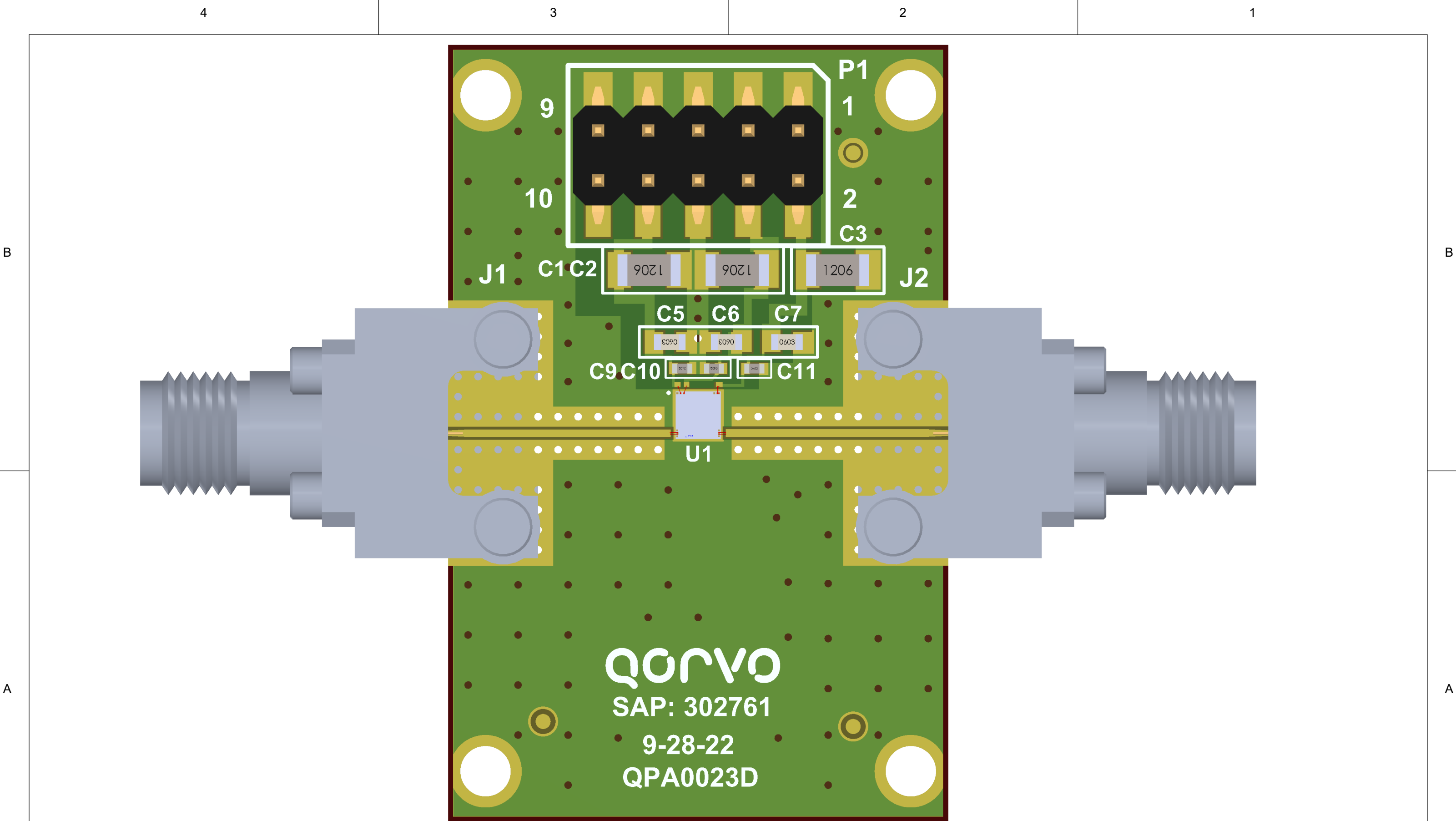
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	SHEET 5 OF 7			CAD: ALTIUM DESIGNER			SCALE: 2:1	

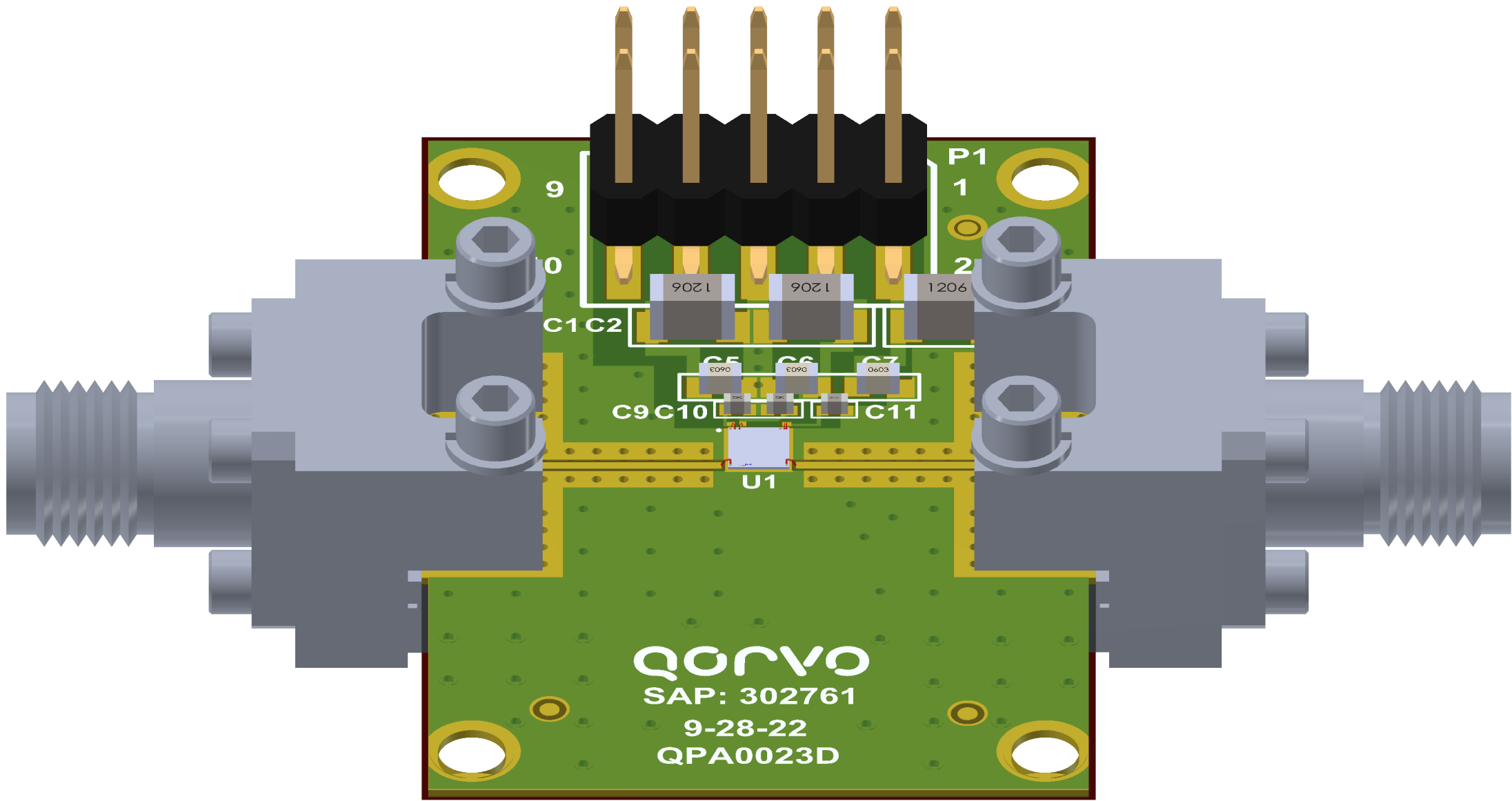


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		B	1CVM1	QPA0023D-4000	N/A	A
		SHEET 6 OF 7	CAD: ALTIUM DESIGNER			SCALE: 2:1

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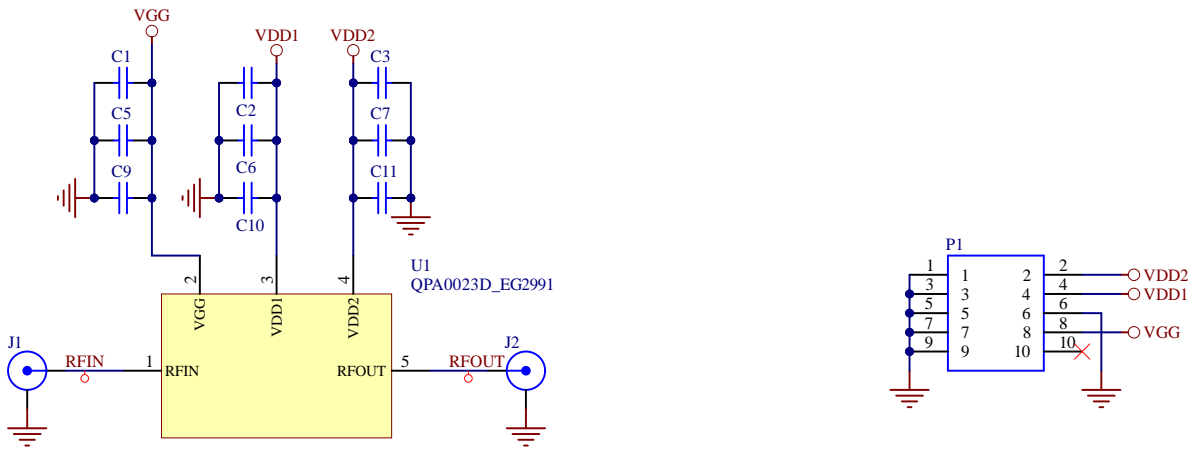
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		B	1CVM1	QPA0023D-4000	N/A	A
		SHEET 7 OF 7	CAD: ALTIUM DESIGNER			SCALE: 2:1

Current Date & Time: 10/27/2022 2:47

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
A	PRODUCTION RELEASE	10/27/2022	M.KELLY



SAP MATERIAL NUMBER: 302761			
APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE	DATE		
DESIGNER ENGR.	B.HUFFIN M.KELLY	TITLE: QPA0023D EVALUATION PCB DESIGN PACKAGE	
PDE CONTROLLED		SIZE B	DOCUMENT NUMBER: QPA0023D-4000
		SCALE: NTS	PROTOTYPE INSTANCE: N/A
		REV. A	
		SHEET 1 OF 1	