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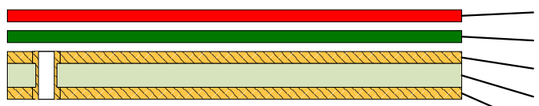
LAYER STACK LEGEND



Material	Layer	Thickness	Dielectric Material	Type	Comment
	SILKSCREEN_TOP			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
Copper	**METAL1_TOP**	**0.0014in**		**Signal**	**FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**
Core		*0.0100in*	*ROGERS 4350*	*Dielectric*	
Copper	**METAL2_BOT**	**0.0014in**		**Signal**	**FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**

Finished board thickness: 0.0132in

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
   A. METAL 1(TOP) AND METAL 2(BOTTOM):
   ELECTROLYTIC FLASH GOLD
   NICKEL PLATE per QQ-N-290, CLASS 1, GRADE G, 200µin. (5µm)
   GOLD PLATE per ASTM B 488, TYPE III, CODE A, 3-10µin. (0.08-0.25µm)

   B. METAL 1(TOP) SELECTIVE ELECTROLYTIC FLASH GOLD PLATING:
   GOLD PLATE per ASTM B 488, TYPE III, CODE A, CLASS 1, 50µin. (1.27µm)
   PLATING MUST BE FREE FROM CONTAMINATION, STAINS AND DEBRIS.
4. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) +/- 10%
5. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM). COPPER TO EDGE AT RF CONNECTORS IS CRITICAL FOR PERFORMANCE.
6. TOLERANCE: PC BOARD OUTLINE: ±0.003in.THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
7. BURRS SHALL NOT EXCEED 0.002in.
8. VIA PLATING/FILLING:
   VIAS UNDER DUT ARE TO BE EPOXY FILLED OVER PLATED AND PLANERIZED.
   ALL OTHER PLATED THRU HOLES ARE TO BE PLATED TO 0.0008 ± 0.0004in. MIN. THICKNESS.
9. CONTROLLED IMPEDANCE: CPW LAYER 1 TRACES ARE 0.015+/- 0.001, REF LAYER 2. TARGET IMPEDANCE IS 50 OHMS +/-5%. TARGET FREQUENCY 6GHz. CORE DIELECTRIC CAN BE ADJUSTED TO OBTAIN FINISHED THICKESS. GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENT TO BE DONE BY PCB FABRICATOR.
10. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
11. NO ELECTRICAL TEST NEEDED.
12. NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
13. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
14. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
15. DELIVER BOARDS BAGGED AS: SINGLES

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 300703		
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE
	DESIGNER	B.HUFFIN	01/31/2022
	ENGR.	N.NOVARIS	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION			
DO NOT SCALE DRAWING			

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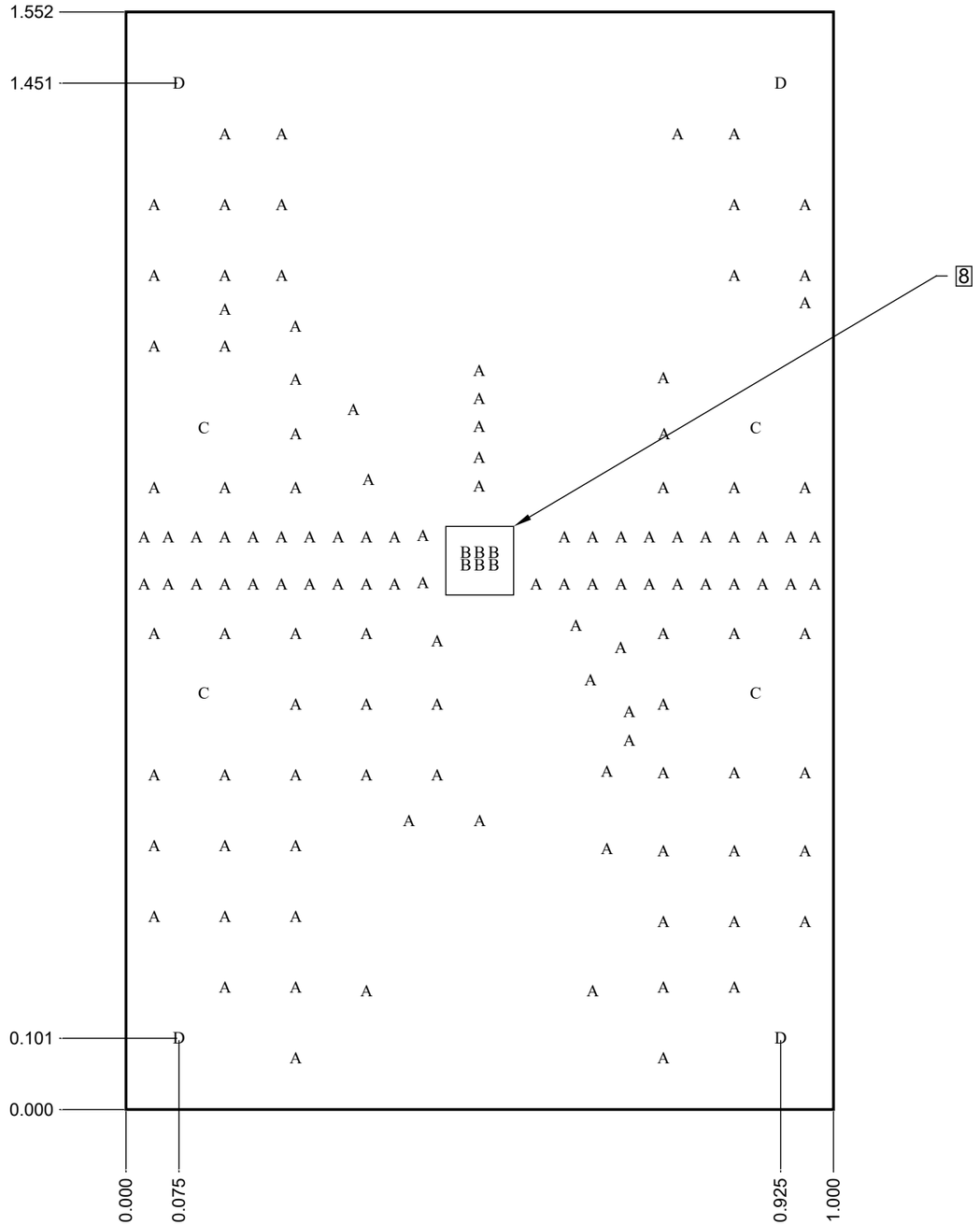
TITLE: QPA0022 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA0022-4000	N/A	A

SHEET 1 OF 6 | CAD: ALTIUM DESIGNER | SCALE: 2:1

Current Date & Time: 2/10/2022 5:01 PM

FOR-001324 REV D



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair
B	6	0.008	Plated	METAL1_TOP - METAL2_BOT
A	128	0.015	Plated	METAL1_TOP - METAL2_BOT
C	4	0.090	Plated	METAL1_TOP - METAL2_BOT
D	4	0.100	Plated	METAL1_TOP - METAL2_BOT
	142 Total			

SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA0022-4000	N/A	A
SHEET 2 OF 6	CAD: ALTIUM DESIGNER		SCALE:	2:1

Current Date & Time: 2/10/2022 5:01 PM

FOR-001324 REV D

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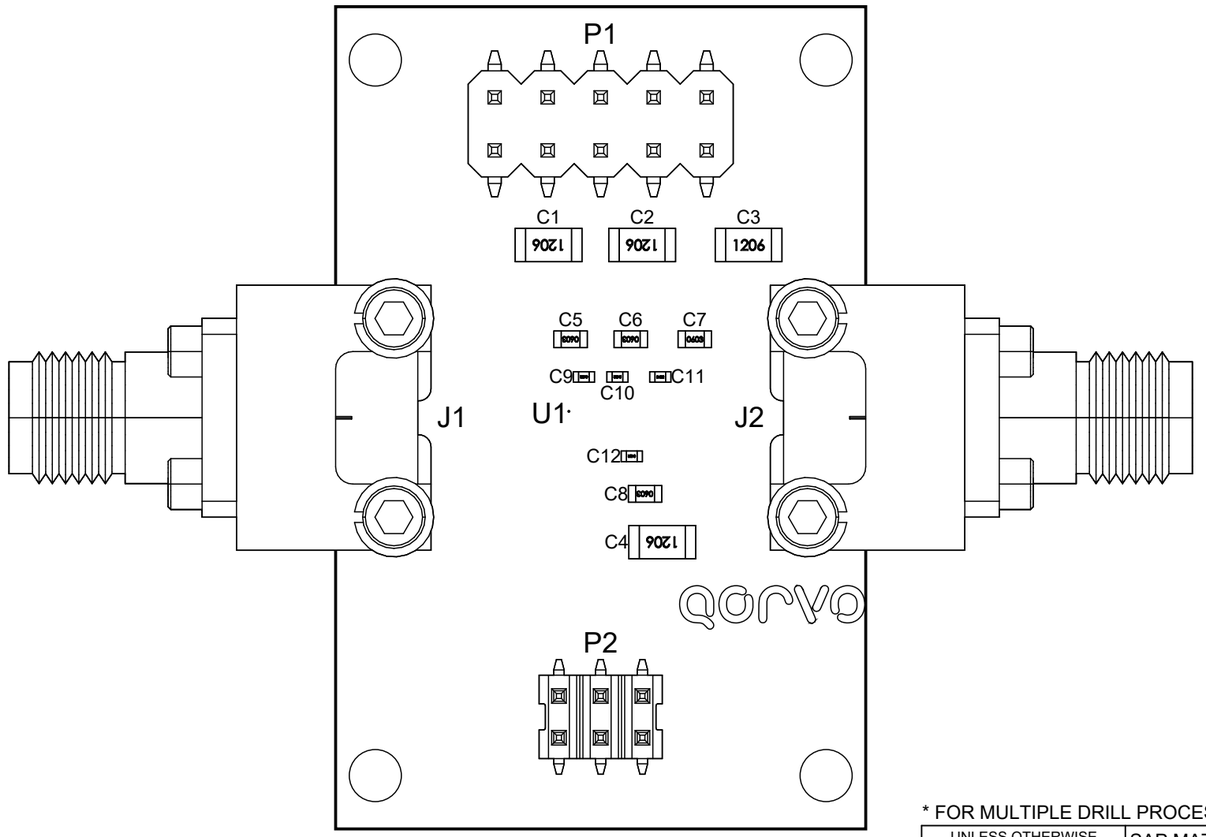
ASSEMBLY NOTES:

16. WORKMANSHIP & SOLDER PER IPC-A-610C, CLASS 2.
17. MANUFACTURERS' PART NUMBERS ARE SUBJECT TO CHANGE BY THE MANUFACTURERS FOLLOWING THE ISSUE OF THIS DOCUMENT, AND ARE THEREBY INCLUDED FOR REFERENCE ONLY. CONTACT QORVO CORORATE ENGINEERING MATERIALS WITH QUESTIONS REGARDING SPECIFIC MANUFACTURERS' PART NUMBERS.
18. QORVO DEVICES (DUT) MAY REQUIRE BAKING PER IPC/JEDEC J-STD-020 FOR A MINIMUM OF 24 HOURS AT 125 +5/-0 DEGREES C. ASSEMBLY MUST TAKE PLACE WITHIN 12 HOURS OF BAKE COMPLETION.
19. LOW TEMP SOLDER SHALL BE USED FOR ALL SMDs AND PRE-TINNING WHEN REQUIRED.
20. LEAD FREE (HIGH TEMP) SOLDER SHALL BE USED FOR SMA AND EDGE MOUNT CONNECTORS.



* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 300703		
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE
	DESIGNER	B.HUFFIN	01/31/2022
	ENGR.	N.NOVARIS	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION			
DO NOT SCALE DRAWING			

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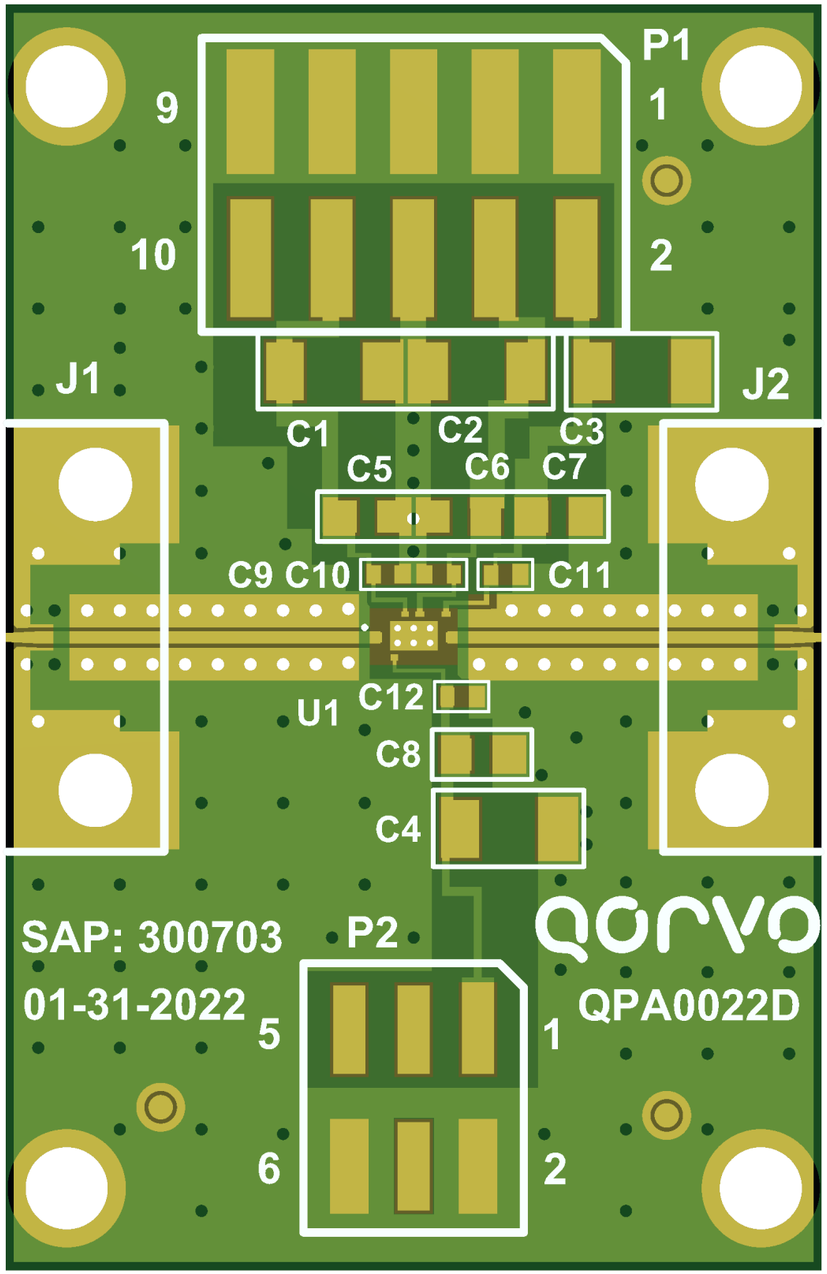
TITLE: QPA0022 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA0022-4000	N/A	A

SHEET 3 OF 6	CAD: ALTIUM DESIGNER	SCALE: 2:1

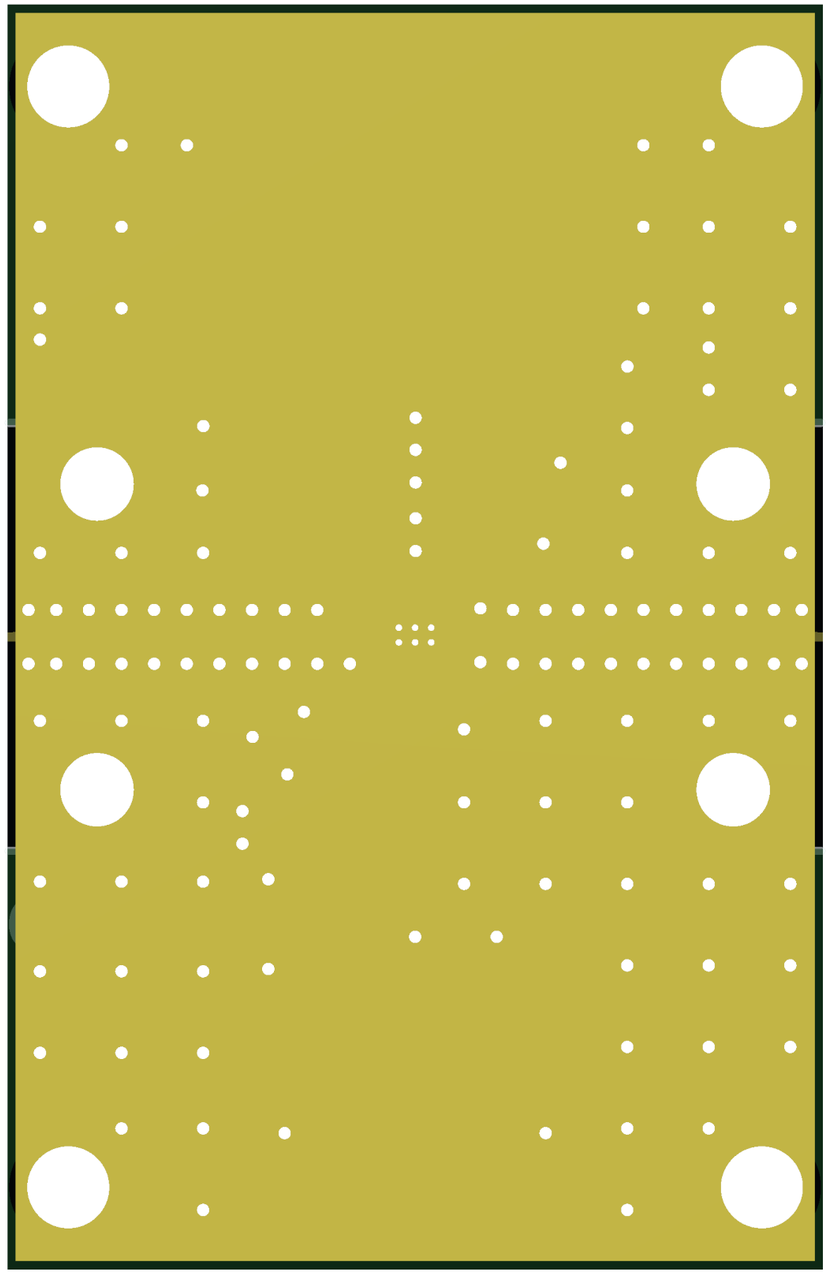
Current Date & Time: 2/10/2022 5:01 PM



SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA0022-4000	N/A	A
SHEET 4 OF 6	CAD: ALTIUM DESIGNER		SCALE:	2:1

Current Date & Time: 2/10/2022 5:01 PM

FOR-001324 REV D



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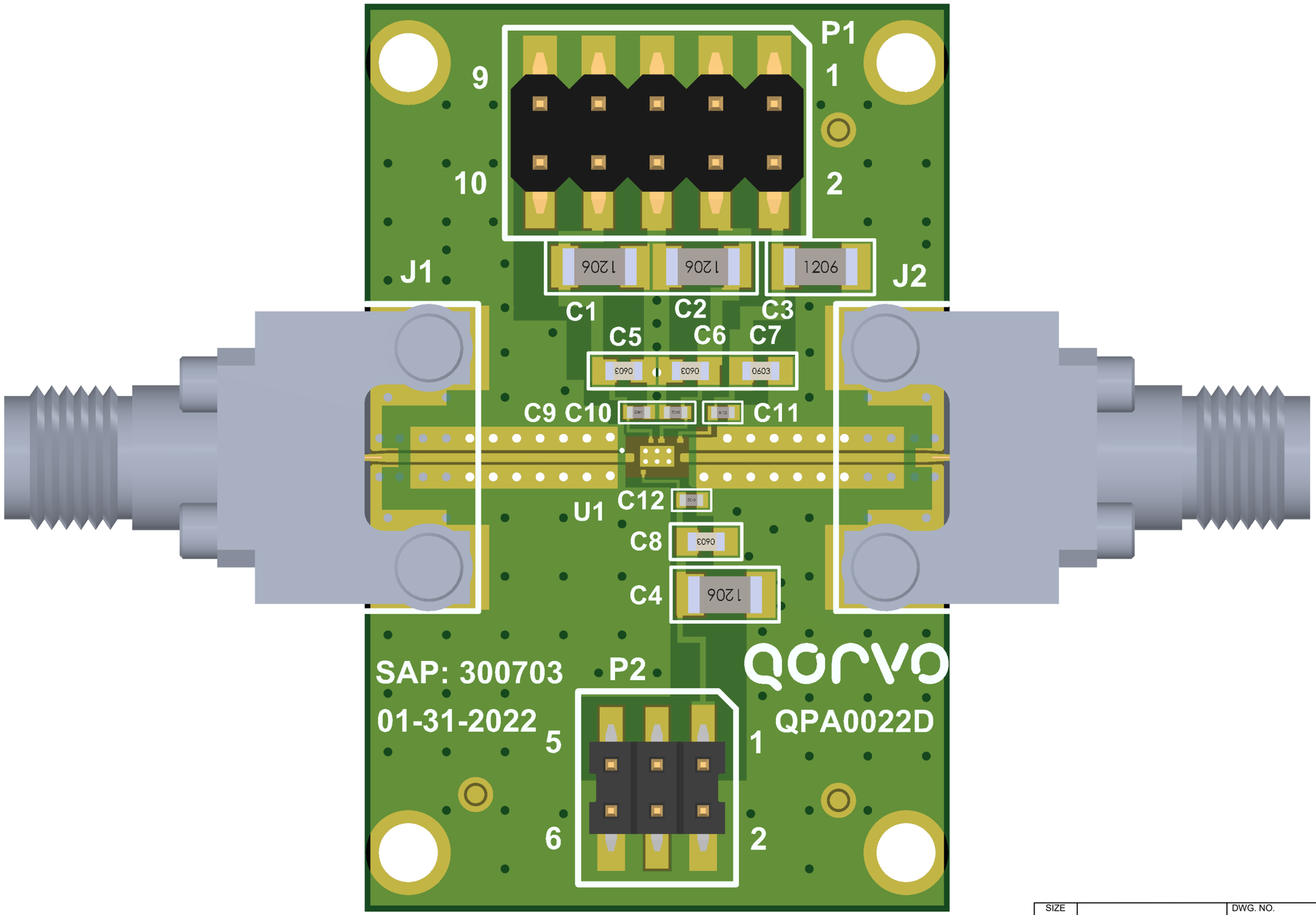
B		QPA0022-4000	N/A	A
SHEET 5 OF 6	CAD: ALTIUM DESIGNER		SCALE:	2:1

Current Date & Time: 2/10/2022 5:01 PM

FOR-001324 REV D

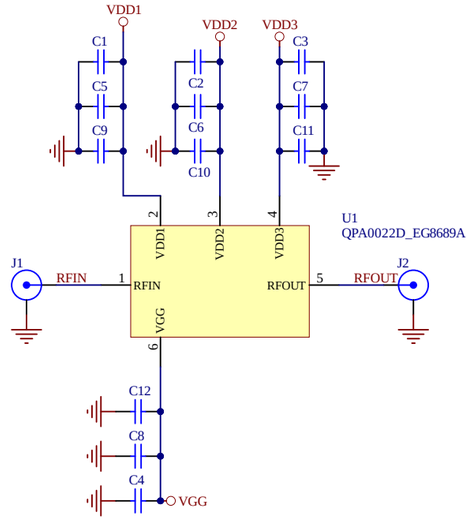


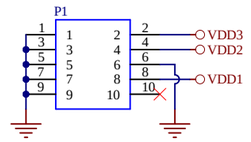
SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA0022-4000	N/A	A
SHEET 6 OF 6	CAD: ALTIUM DESIGNER		SCALE:	2:1

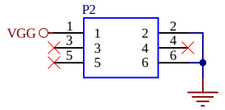
Current Date & Time: 2/10/2022 5:01 PM

FOR-001324 REV D

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
A	INITIAL RELEASE	01-31-2022	N.NOVARIS







QORVO_LOGO

FD1 FD2 FD3

SAP MATERIAL NUMBER: 300703			
APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE	
DESIGNER	J.CHAN	01-31-2022	
ENGR.	N.NOVARIS		
PDE CONTROLLED			

TITLE: QPA0022D EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA0022D-4000	N/A	A

SCALE: NTS SHEET 1 OF 1