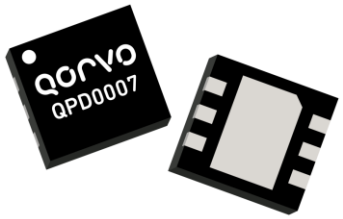
QPD0007

20 W, 48 V, DC – 5 GHz, GaN RF Transistor

Product Overview

The QPD0007 is a single-path discrete GaN on SiC HEMT in a DFN package which operates from DC to 5 GHz. It is a single-stage, unmatched transistor capable of delivering P3dB of 20W at +48 V operation.

Lead free and RoHS compliant.



6 Pin 4.5 x 4.0 mm DFN Package

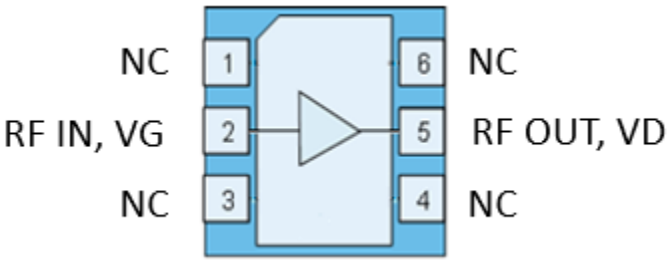
Key Features

- Operating Frequency Range: DC – 5 GHz
- Operating Drain Voltage: +48 V
- Maximum Output Power (P3dB): 20 W (1)
- Maximum Drain Efficiency: 73% (1)
- Efficiency-Tuned Back off Gain: 19 dB (1)
- 4.5 x 4.0 mm DFN Package

Notes:

1. Single-path load pull data at 3.5 GHz.

Functional Block Diagram



Applications

- WCDMA / LTE
- Macrocell Base Station
- Microcell Base Station
- Small Cell
- Active Antenna
- 5G Massive MIMO
- General Purpose Applications

Ordering Information

Part Number	Description
QPD0007TR13	13” Reel – 2500 Pieces
QPD0007EVB02	3.4 – 3.6 GHz EVB

Absolute Maximum Ratings

Parameter	Rating
Breakdown Voltage (BV_{DG})	+165 V
Gate Voltage Range (V_G)	−7 to +2 V
Drain Voltage (V_D)	+55 V
Peak RF Input Power	+34 dBm
VSWR Mismatch, P1dB Pulse (10% Duty Cycle, 100 µs Width), T = +25°C	10:1
Storage Temperature	−65 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Gate Voltage (V_G)		−2.7		V
Drain Voltage (V_D)		+48		V
Quiescent Drain Current (I_{DQ})		32.5		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3400		3600	MHz
Quiescent Drain Current			32.5		mA
Gain (1)	P_{OUT} = 29 dBm	17.4	18.4		dB
Peak Power (2)		39.0	39.7		dBm
Drain Efficiency (1)	P_{OUT} = 29 dBm	17.0	20.0		%
Gate Leakage	V_G = -7V, V_D = +48V	-1.5			mA

Notes:

1. Test conditions unless otherwise noted: VD = +48 V, IDQ = 32.5 mA, T = +25°C, using an LTE 20 MHz 8 dB PAR at 3600 MHz on a 3400 – 3600 MHz test fixture tuned for maximum efficiency.
2. Test conditions unless otherwise noted: VD = +48 V, IDQ = 32.5 mA, T = +25°C, using an LTE 20 MHz 10 dB PAR at 3600 MHz on a 3400 – 3600 MHz test fixture tuned for maximum efficiency.

Thermal Information

Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	T_{CASE} = +85°C, T_{CH} = 119°C CW: P_{DISS} = 4.6 W, P_{OUT} = 1 W	7.5	°C/W

Notes:

1. Thermal resistance is measured to package backside.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	5.6 – j1.4	25.1 + j13.6	43.3	62.9	19.0
2600	5.6 – j3.7	25.0 + j13.6	43.2	62.1	18.4
2700	5.8 – j5.2	18.7 + j11.3	43.3	59.5	17.8
3400	5.8 – j11.8	17.1 + j9.7	43.2	62.6	15.9
3500	5.8 – j11.3	19.0 + j7.3	43.3	61.4	15.8
3600	5.9 – j12.1	19.0 + j8.2	43.2	63.1	15.5
3700	6.1 – j13.4	21.8 + j4.1	43.3	59.7	14.9
3800	5.9 – j13.4	21.6 + j4.8	43.3	61.8	15.5

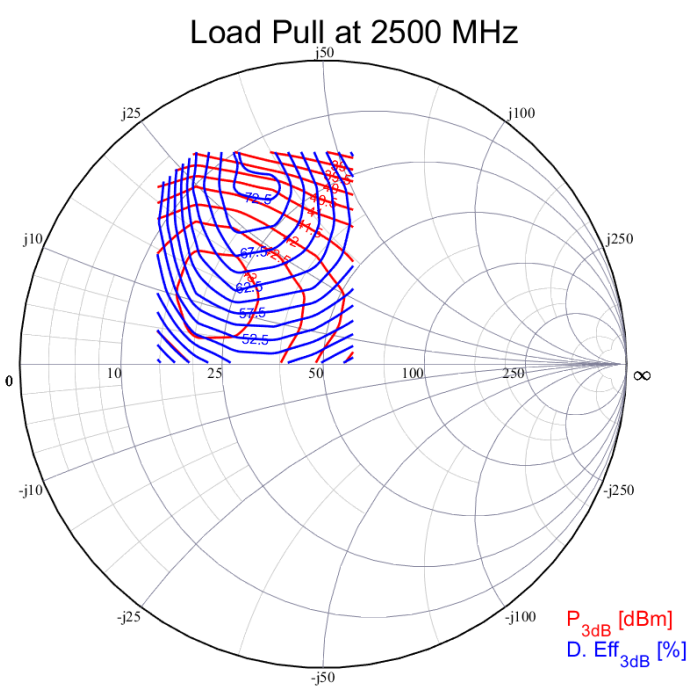
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse CW (10% duty cycle, 100 µs width).

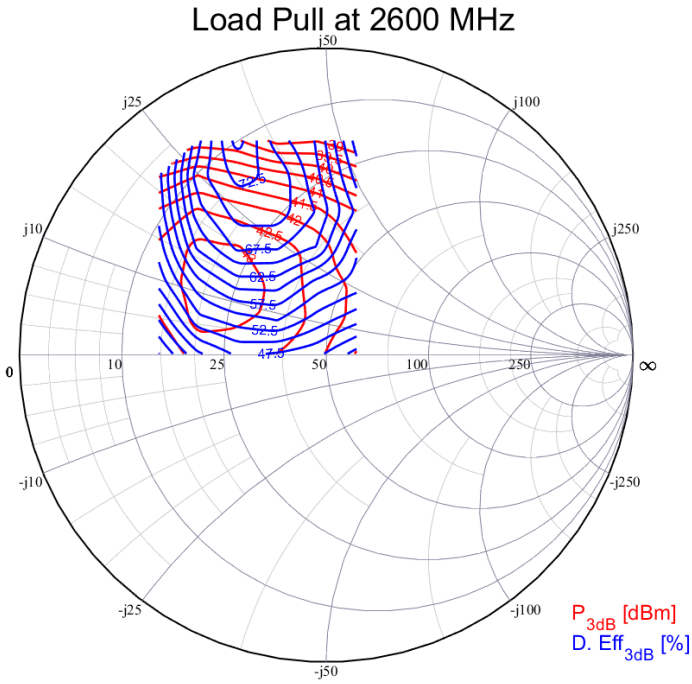
Efficiency-Matched Load Pull Performance

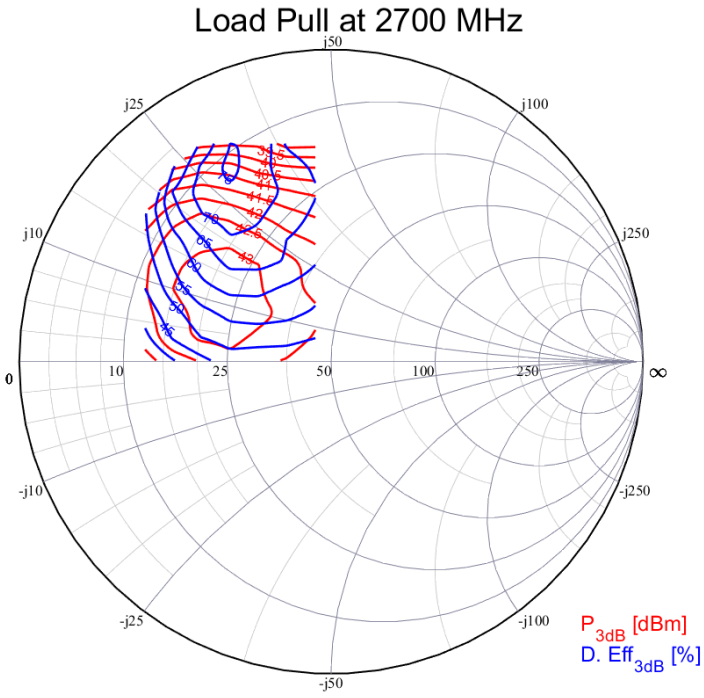
Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	5.6 – j1.4	18.8 + j34.6	40.9	74.5	20.0
2600	5.6 – j3.7	9.9 + j32.5	39.5	76.9	20.4
2700	5.8 – j5.2	11.8 + j29.0	40.7	77.5	19.8
3400	5.8 – j11.8	10.7 + j21.7	41.2	76.0	17.2
3500	5.8 – j11.3	12.6 + j21.2	41.4	74.4	17.1
3600	5.9 – j12.1	12.7 + j21.5	41.1	73.5	16.6
3700	6.1 – j13.4	11.1 + j16.9	41.4	72.7	16.4
3800	5.9 – j13.4	10.8 + j17.4	40.9	71.8	16.7

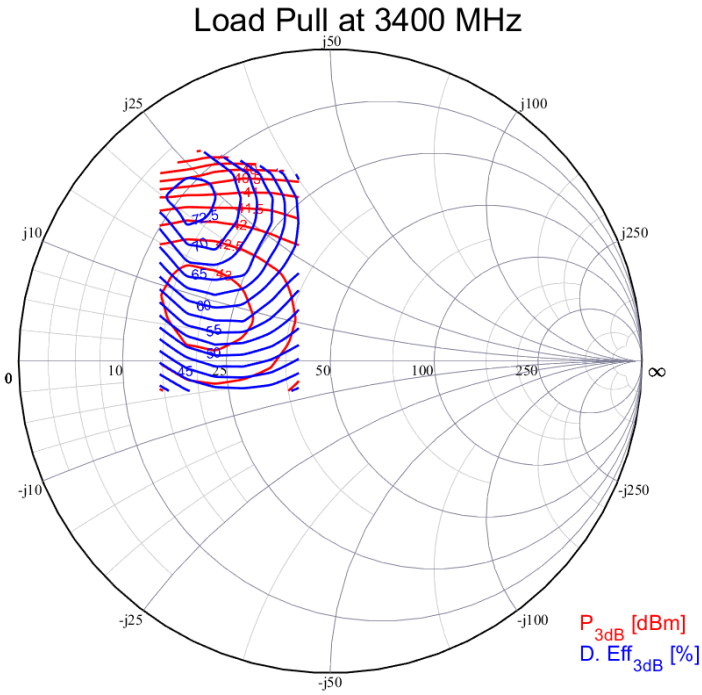
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse CW (10% duty cycle, 100 µs width).

Load Pull Contours









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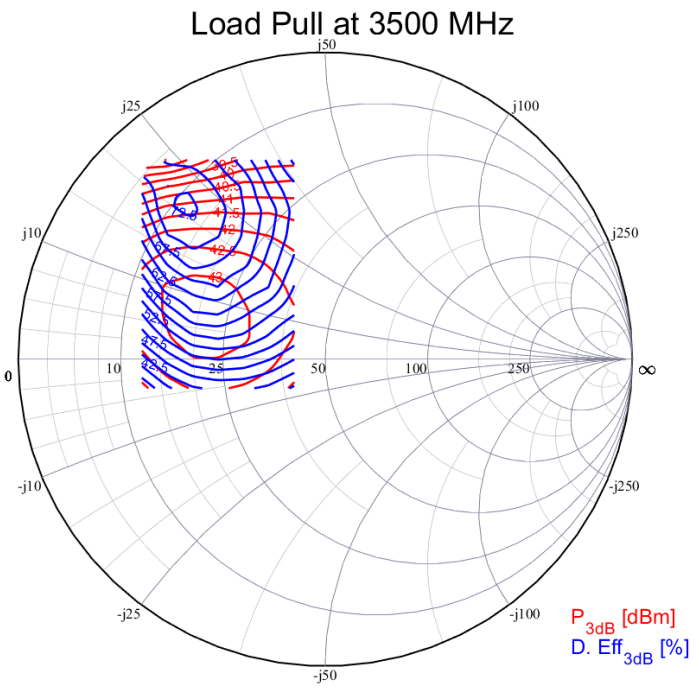
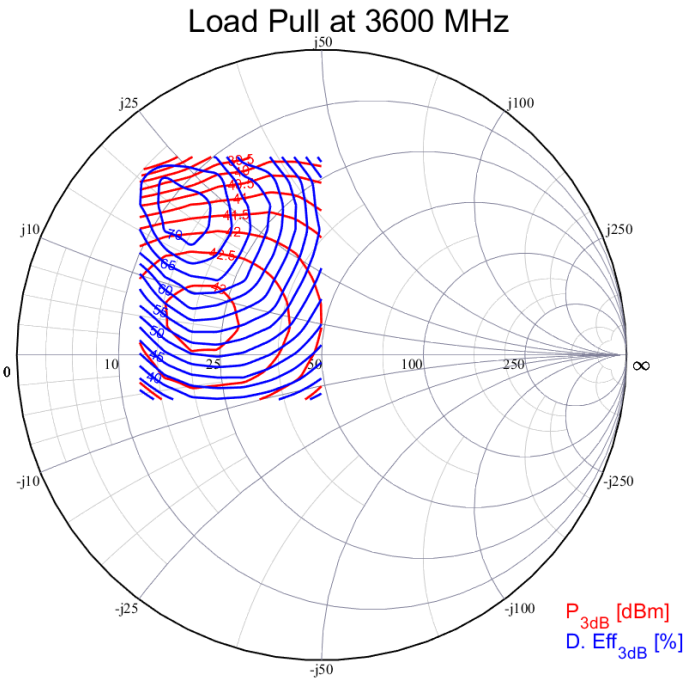
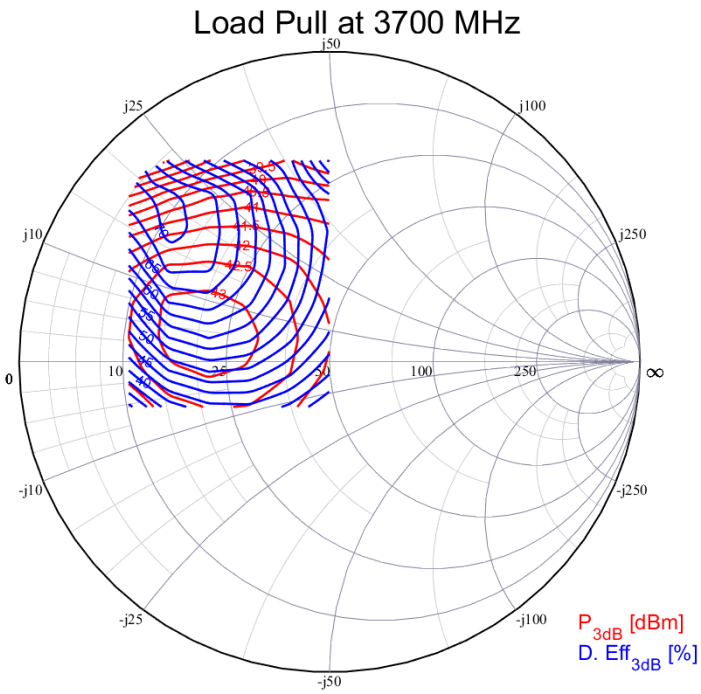
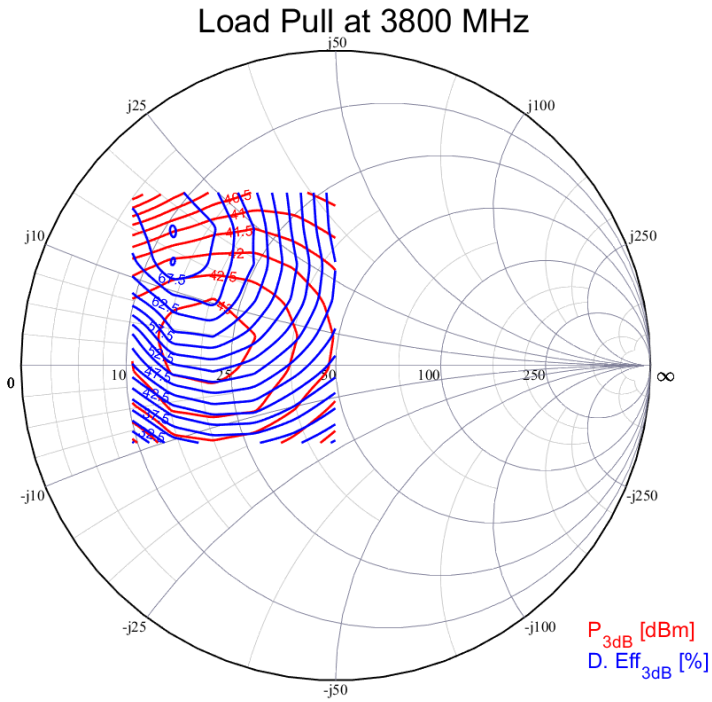


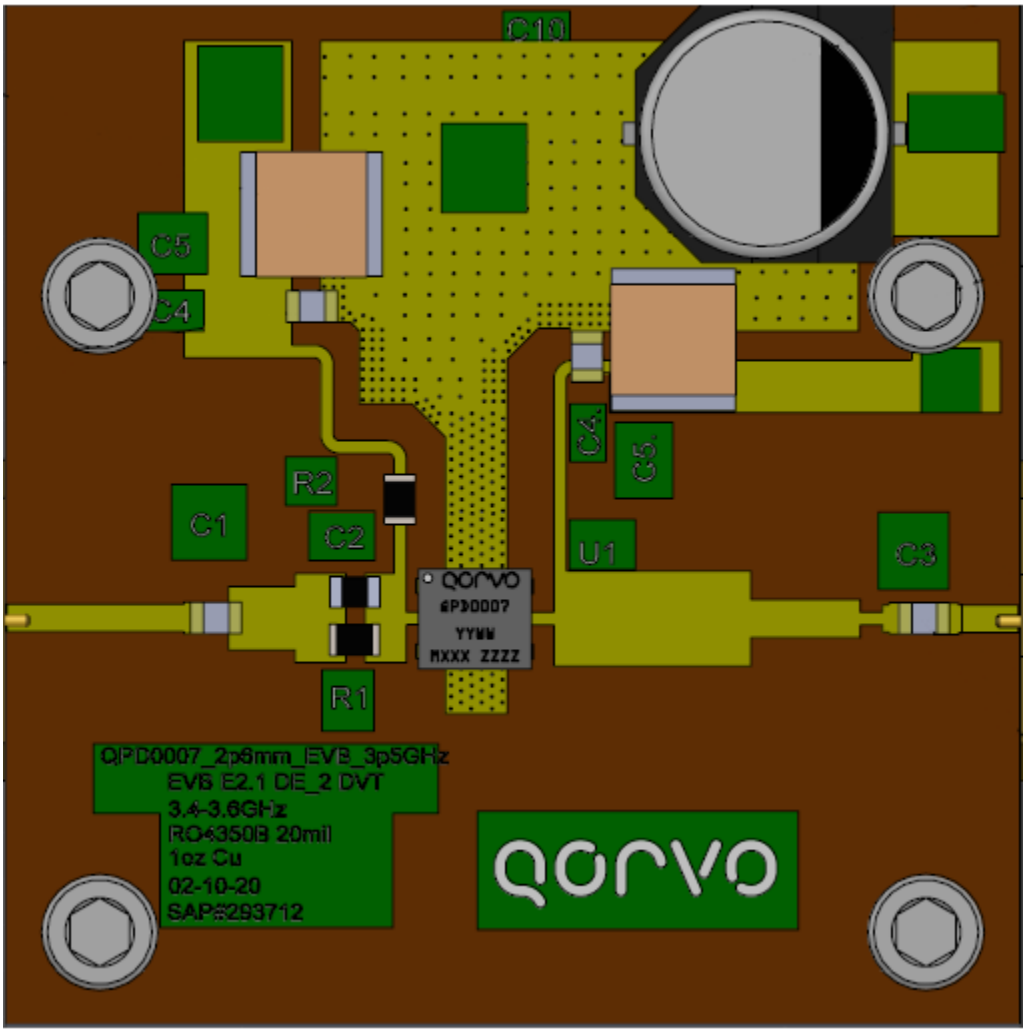






Test Conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse CW (10% duty cycle, 100 µs width).

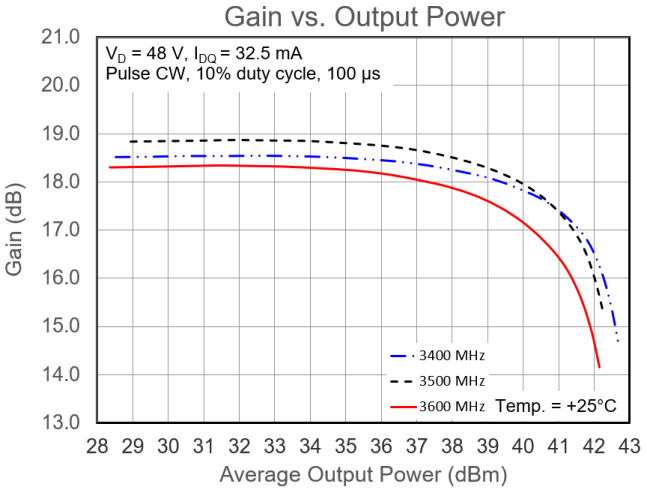
QPD0007EVB02 Layout – 3400 – 3600 MHz Reference Design

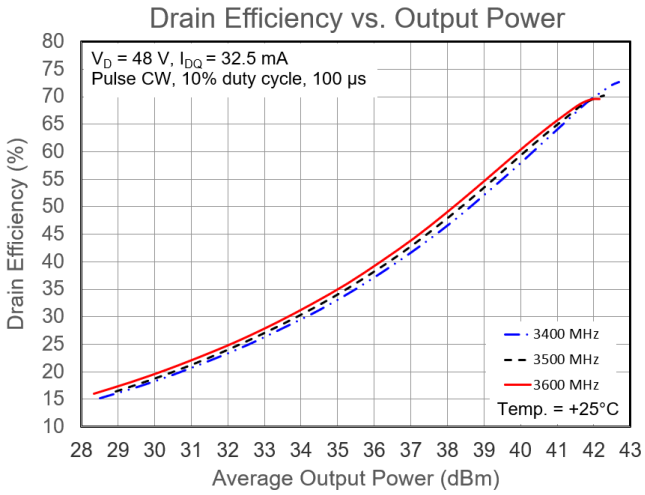


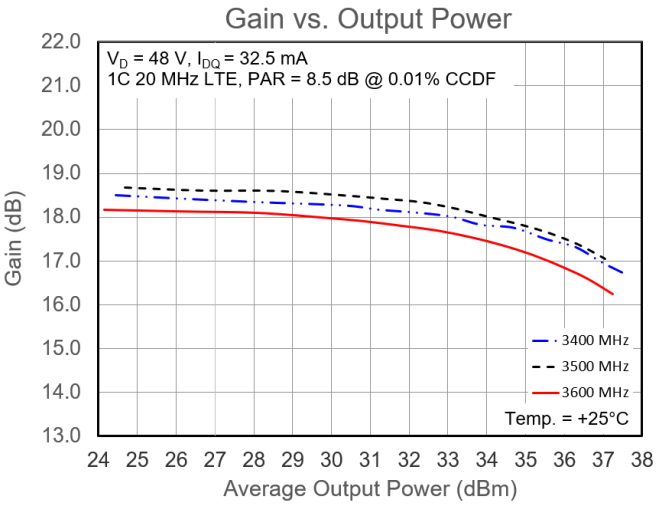
QPD0007EVB02 Bill of Materials – 3400 – 3600 MHz Reference Design

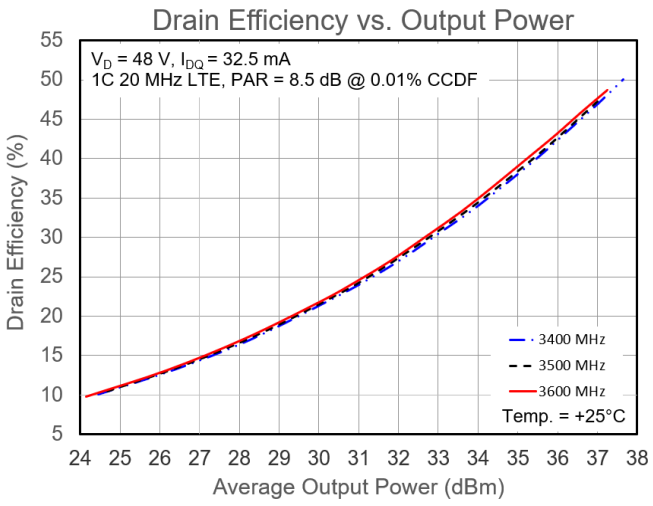
Reference Des.	Value	Description	Manuf.	Part Number
C1, C3	0.9pF	CAP, 0.9pF, +/-0.1pF, 250V, C0G, 0805	ATC	600F0R9BT250XT
C2	1.8pF	CAP, 1.8pF, ±0.05pF, 250V, C0G, 0805	ATC	600F1R8AT250XT
C4, C4	10pF	CAP, 10pF, 1%, 250V, C0G, 0805	ATC	600F100FT250XT
C5, C5	10uF	CAP, 10uF, 20%, 100V, X7S, 2220	TDK	C5750X7S2A106M230KB
C10	220uF	CAP, 220uF, 20%, 50V, 500mA, ALU-ELECTRO	United Chemi-Con	EMVY500ADA221MJA0G
R1	330Ohm	RES, 330OHM, 0.1%, 1/4W, 0805	Panasonic	ERJ-PB6B3300V
R2	15Ohm	RES, 15OHM, 2%, 50W, 0805	International Manufacturing	ND3-0805WA15R0G
U1	-	3.4-3.8GHz 15W 50V GaN Single Channel	Qorvo	QPD0007
J1, J2 (not pictured)	-	CONNECTOR, SMA (PSF-S00-000)	Powell	PSF-S00-000

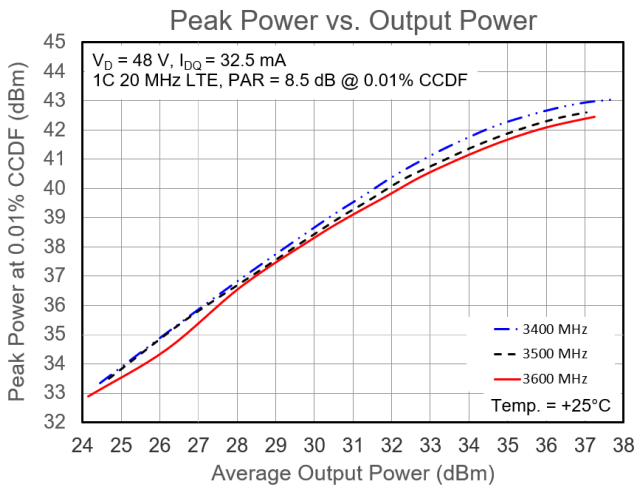
QPD0007EVB02 Performance Plots – 3400 – 3600 MHz Reference Design

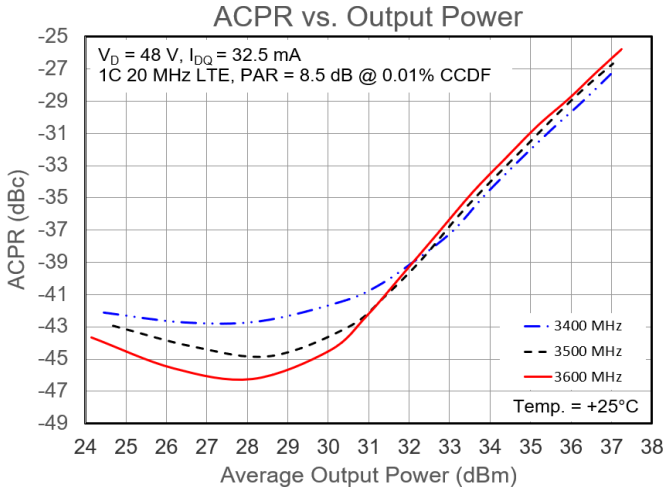






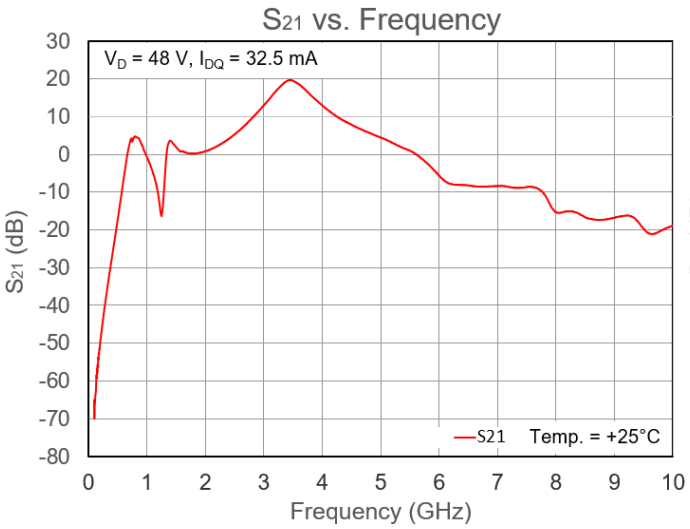


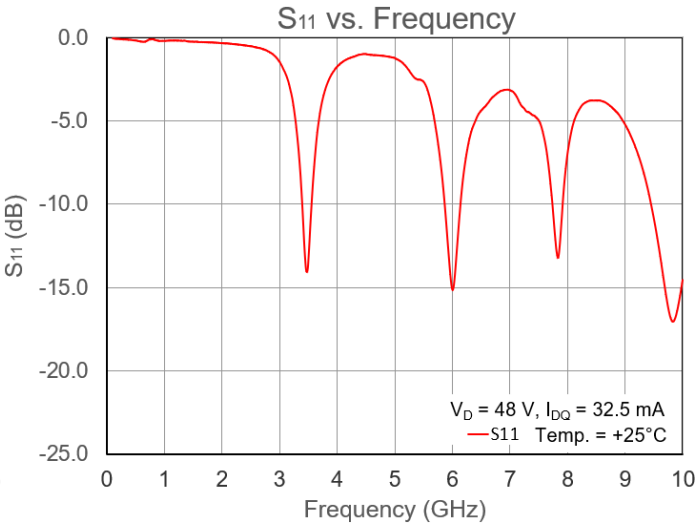


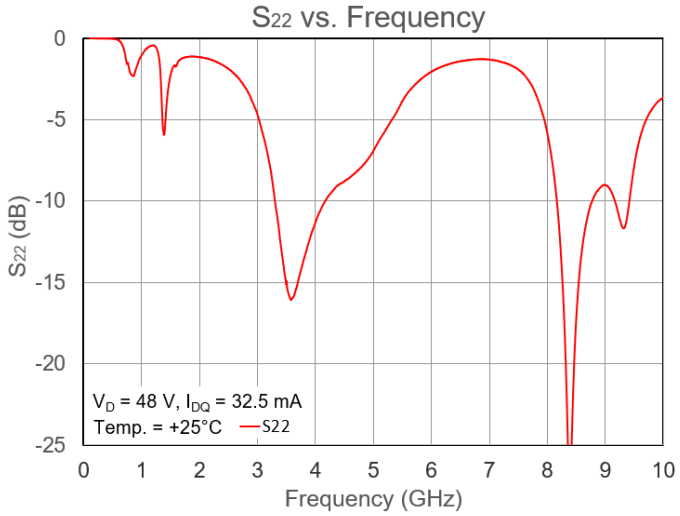


Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C on a reference design fixture tuned for 3400 – 3600 MHz.

QPD0007EVB02 Performance Plots – 3400 – 3600 MHz Reference Design



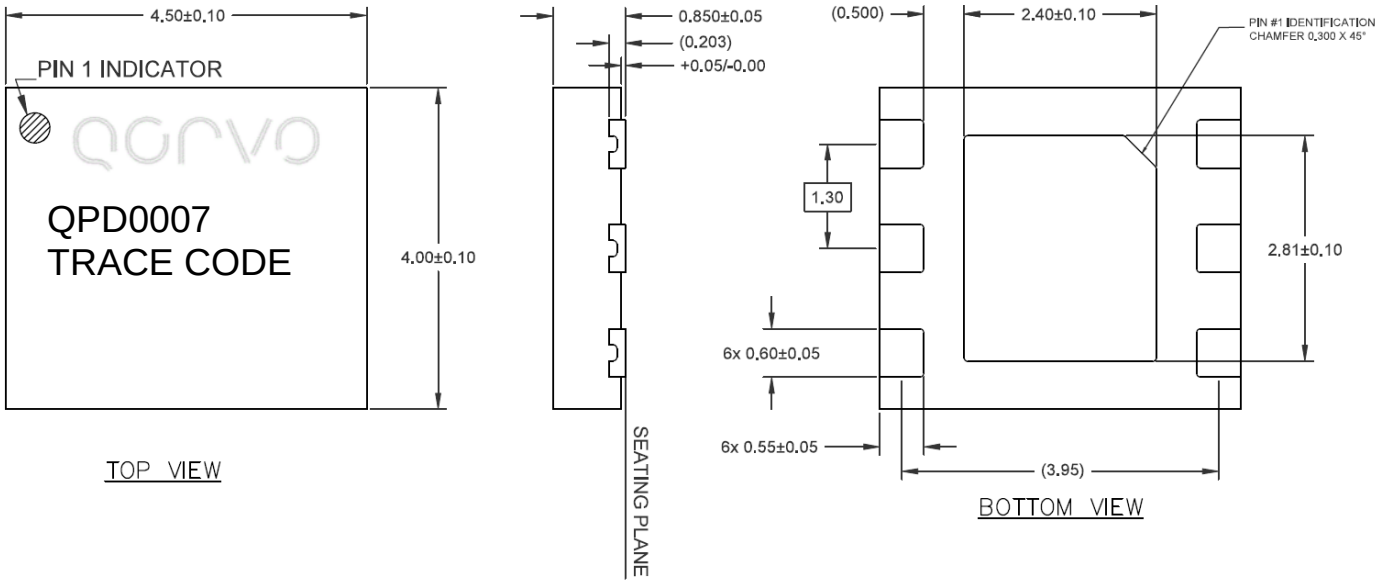




Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C on a reference design fixture tuned for 3400 – 3600 MHz.

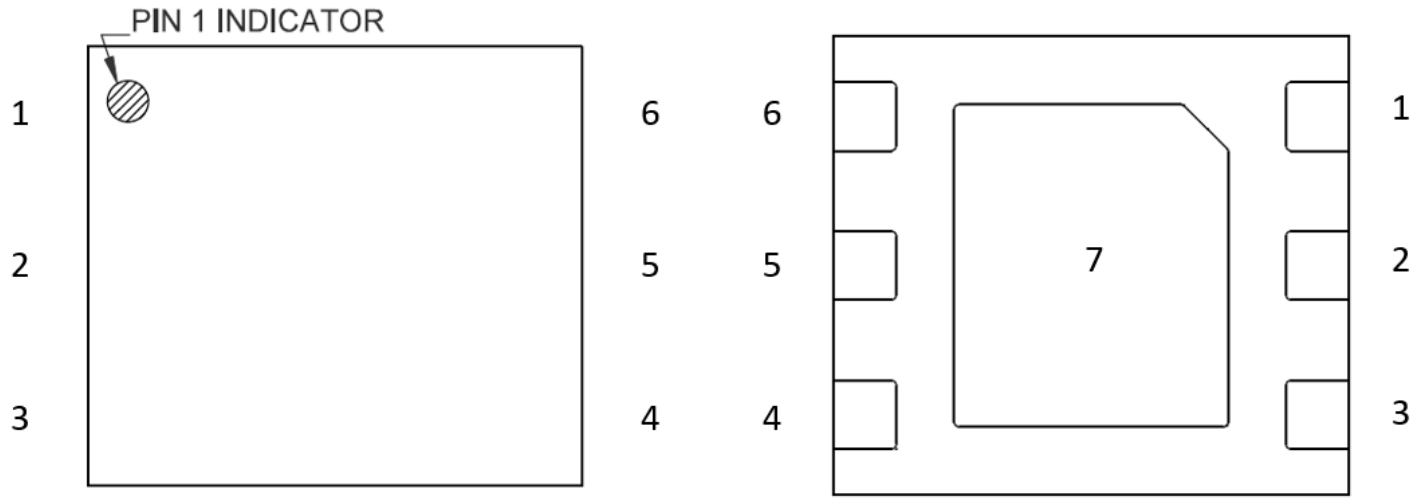
Package Marking and Dimensions

Marking: Qorvo Logo
Part Number – QPD0007
Trace Code – To be assigned by subcontractor



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. General tolerance is ±0.05 unless otherwise shown.
3. Part is overmold encapsulated.
4. Contact plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

Pin Configuration and Description



Top View

Bottom View

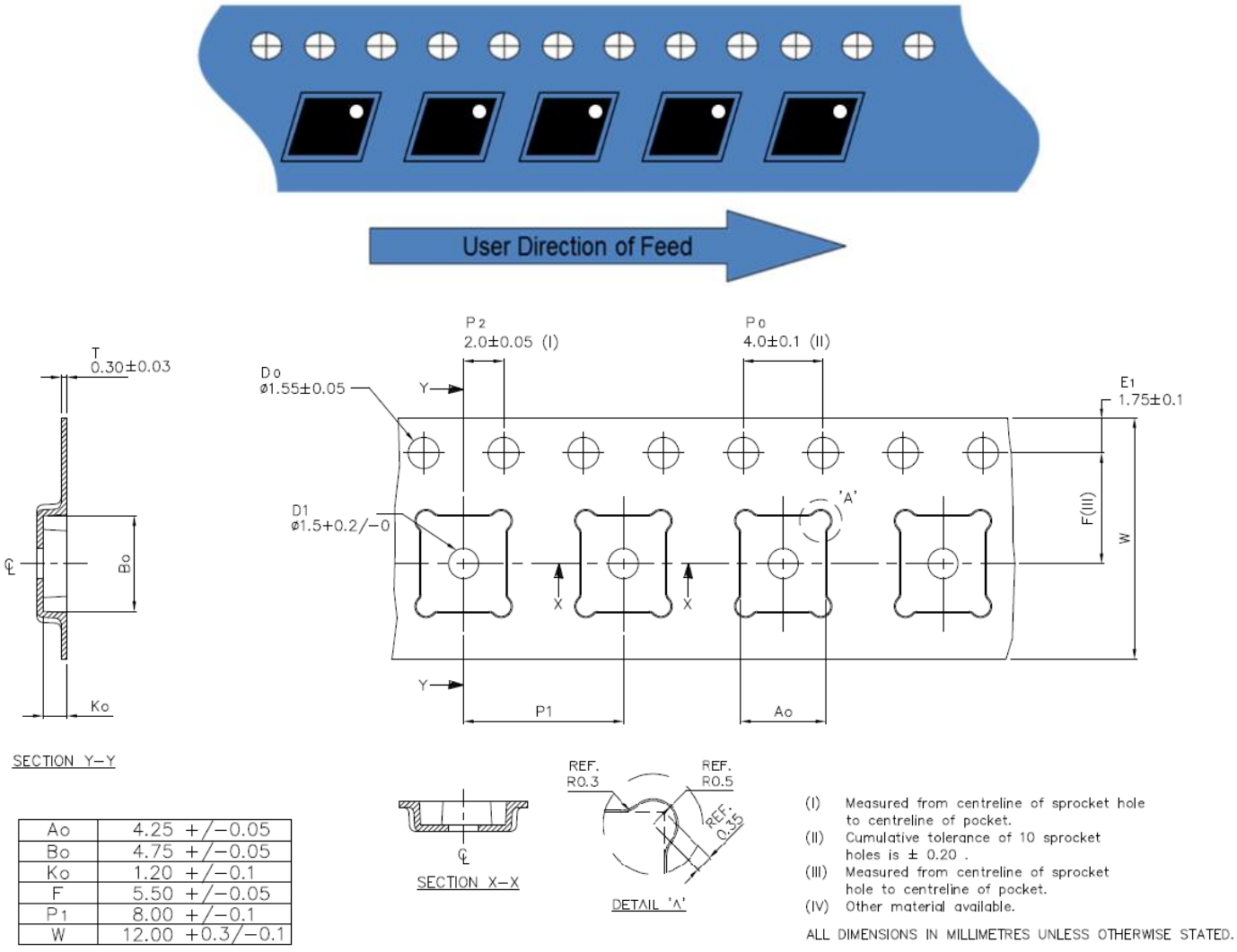
Pin Number	Label	Description
1	NC	No Connect
2	RF IN, VG	RF Input, Gate Bias
3	NC	No Connect
4	NC	No Connect
5	RF OUT, VD	RF Output, Drain Bias
6	NC	No Connect
7 (Backside Paddle)	GND	Ground

Biasing Procedure

Bias On	Bias Off
1. Turn ON V_G to −5 V. 2. Turn ON V_D to +48 V. 3. Slowly adjust V_G until I_D = 32.5 mA. (Typically, V_G = −2.7 V.) 4. Turn ON RF.	1. Turn OFF RF. 2. Adjust V_G to −5 V. 3. Turn OFF V_D. 4. Wait two (2) seconds to allow drain capacitors to discharge. 5. Turn OFF V_G.

Tape and Reel Information – Carrier and Cover Tape Dimensions

Tape and reel specifications for this part are also available on the Qorvo website.
Standard T/R size = 2500 pieces on a 13” reel.

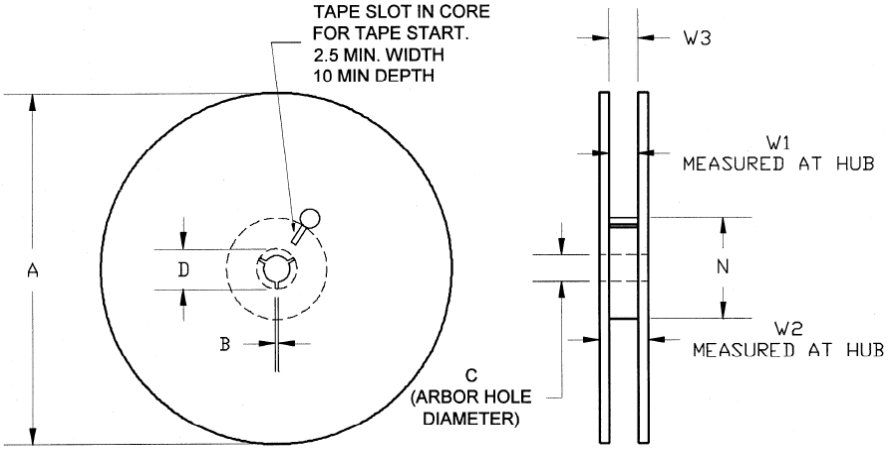


Ao	4.25 +/−0.05
Bo	4.75 +/−0.05
Ko	1.20 +/−0.1
F	5.50 +/−0.05
P1	8.00 +/−0.1
W	12.00 +0.3/−0.1

Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.167	4.25
	Width	B0	0.187	4.75
	Depth	K0	0.047	1.20
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12.00

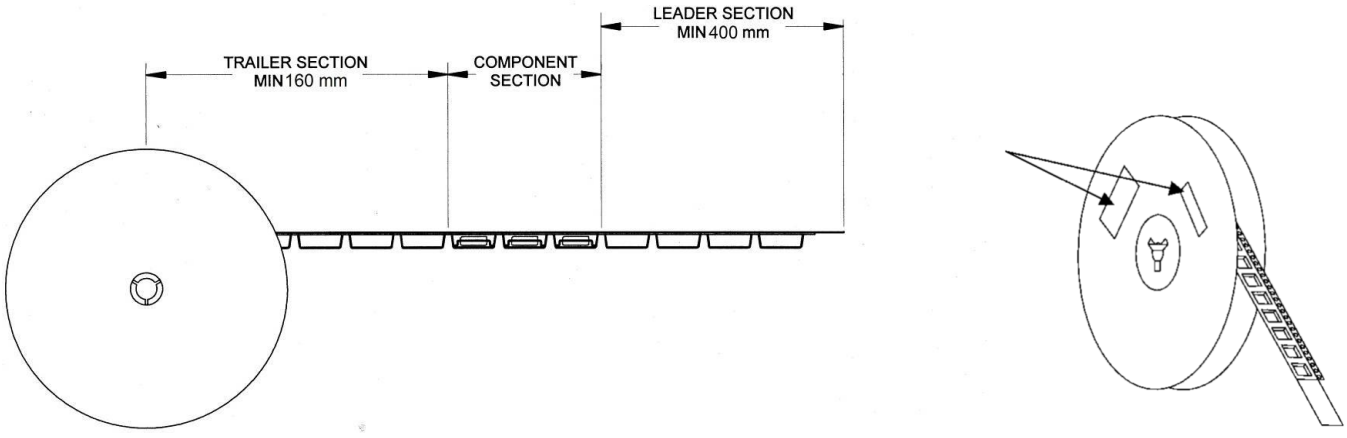
Tape and Reel Information – Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.



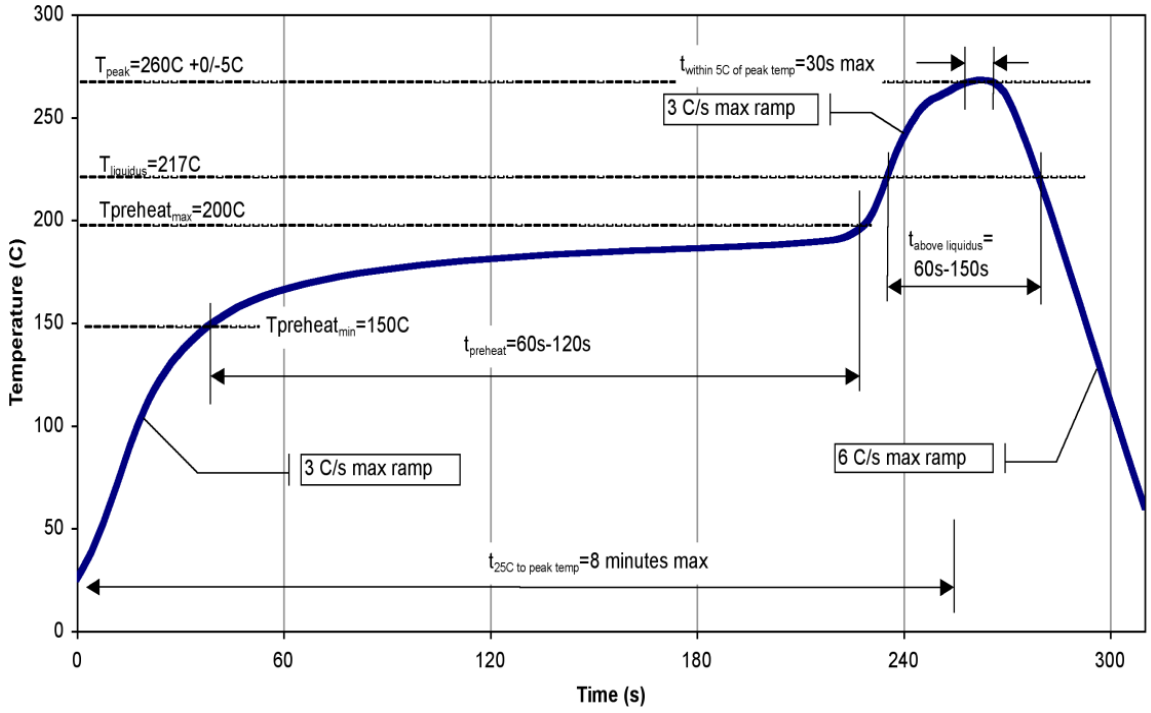
Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A (250V)	ANSI/ESDA/JEDEC Standard JS-001
ESD – Charged Device Model (CDM)	Class C3 (1000V)	ANSI/ESDA/JEDEC Standard JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC Standard J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering processes.

Package lead plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

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