ACT4921 Register Definitions – CMI 301

Abstract

This application note identifies and explains the ACT4921 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. This application note is specific to the Code Matrix Index, CMI 301.

Introduction

The ACT4921 is an ActivePMU eFuse and power loss protection IC from Qorvo. Its flexibility allows it to operate with a wide range of FPGA's, peripherals, microcontrollers, and solid-state drive applications. The ACT4921 includes a step up boost converter to charge a bank of storage capacitors and a DC/DC step down converter to convert the stored energy to maintain the desired output voltage during input voltage brownout or power loss. It also provide an on-board ADC converter to monitor the system's state of health. The I^2C interface provides access to the internal registers, which are configurable to make this IC flexible for many different applications.

Although the ACT4921 is programmed at the factory with a default configuration, these settings can be changed through the I^2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as fault thresholds and responses, status, and more. Qorvo identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT4910's CMI 301. Refer to the appropriate application note for register information for other CMI versions.

The ACT4921 contains the following register types:

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult customer.support@qorvo.com for custom options and minimum order quantities.

I2C REGISTER MAP

BASIC VOLATILE								
ADDR (HEX)	7	6	5	4	3	2	1	0
0	RFU	RFU	RFU	RFU	RFU	CURRENT_STATE [2:0]		
1	PVIN_OV	THERMAL_SHUTDOWN	THERMAL_PWRDWN	THERMAL_ALERT	FB_nPG	VINSPIN_OV	eFUSE_nPG	VB/STR_SHORT
2	eFUSE_ILIM_ALERT	eFUSE_OC_SHUTDOWN	LDO_UV	VINSPIN_UV	STR_UV	STR_OV	STR_PG	BUCKIN_UV
3	BUCK_ILIM_SHUTDOWN	BUCK_ILIM_ALERT	BUCK_nPG	BUCK_COMPFAIL	VB_nPG	HCHK_NG	SPLMNT_MODE	BOOTCAPFAIL
4	RFU							
5	MSTR_OK	RFU	RFU	CMP_BSET_HI	RFU	RFU	PVIN_nUV	eFUSE_ISETLOW
6	RFU	RFU	RFU	DISCHG_STR	EN_BFET	EN_STR10mASINK	FORCE_HLTHCHK	FORCE_PWROFF
7	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

BASIC NON-VOLATILE								
ADDR (HEX)	7	6	5	4	3	2	1	0
8	PVIN_OV_IRQ_MASK	THML_SD_IRQ_MASK	THML_PD_IRQ_MASK	THML_ALERT_IRQ MASK	FB_nPG_IRQ_MASK	ENPIN_OV_IRQ_MASK	eF_nPG_IRQ_MASK	STR_SHORT_IRQ_MASK
9	eF_ILIM_ALERT_IRQ MASK	eF_OC_SD_IRQ_MASK	LDO_UV_IRQ_MASK	ENPIN_UV_IRQ_MASK	STR_UV_IRQ_MASK	STR_OV_IRQ_MASK	STR_PG_IRQ_MASK	BUCKIN_UV_IRQ_MASK
A	BUCK_ILIM_SD_IRQ_MASK	BUCK_ILIM_ALERT_IRQ_MASK	BUCK_nPG_IRQ_MASK	BUCK_COMPFAIL_IRQ_MASK	VB_nPG_IRQ_MASK	HCHK_NG_IRQ_MASK	SPLMNT_IRQ_MASK	BOOTCAPFAIL_IRQ_MASK
B	GLOBAL_IRQ_MASK	EN_ENB_REG	EN_DISCHG_UVSTATE	DIS_HEALTH_CHK	HMON_TSET [3:0]			
C	HMON_THR [3:0]				EN_STARTDLY[2:0]			RFU
D	RFU	BST_CLIM [1:0]		BST_VSET [4:0]				
E	BUCK_HSD_SLEW_2X	BUCK_HSD_SLEW [1:0]		BUCK_LSD_SLEW [1:0]		VINS_OV_REF [2:0]		
F	STR_UV_TH [1:0]		RFU	BKILIM_OPT	EN_GMADJ_TRAN	ADJ_STH	BUCK_UV_TH [1:0]	
10	BUCK_FREQ [1:0]		RFU	RFU	SCALE_TEST_2X	SCALE_TEST_4X	SCALE_HCHK_2X	SCALE_HCHK_4X
11	MASK_BUCKIN_nUV	MASK_eF_OC	MASK_eF_ILM	MASK_LDO_FAULT	MASK_STR_OV	MASK_STR_UV	MASK_BUCK_OV	MASK_BUCK_UV
12	RFU							

STATUS0 – Status Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[4:0]					CURRENT_STATE[2:0]		
Default	00000					000		
Access	RO					RO		

Name	Description	Notes
RFU[4:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
CURRENT_STATE[2:0]	000 = UV/POR 001 = SOFTSTART 010 = NORMAL 011 = HEALTH CHECK 100 = SUPPLEMENT 101 = SUPPLEMENT-DISABLE 110 = SHUTDOWN 111 = NA	Shows the current state of the state machine.

STATUS1 - Status Register

Address = 0x01h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PVIN_OV	THERMAL_ SHUTDOWN	THERMAL_ PWRDWN	THERMAL_ ALERT	FB_nPG	VINSPIN _OV	eFUSE_ nPG	VB/STR_ SHORT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
PVIN_OV	0 = VIN < OVLO 1 = VIN > OVLO	When this bit = 1, nIRQ goes low if this function is not masked.
THERMAL_SHUTDOWN	0 = Junction temperature < 155 deg C. 1 = Junction temperature > 155 deg C.	Asserts nIRQ when =1 and the function is not masked.
THERMAL_PWRDWN	0 = Junction temperature < 145 deg C. 1 = Junction temperature < 145 deg C.	Asserts nIRQ when =1 and the function is not masked.
THERMAL_ALERT	0 = Junction temperature < 120 deg C. 1 = Junction temperature > 120 deg C.	Asserts nIRQ when =1 and the function is not masked.
FB_nPG	0 = FB pin is > 95% of the 0.8V reference voltage 1 = FB pin is < 95% of the 0.8V reference voltage	Asserts nIRQ when =1 and the function is not masked. This function is only active when the IC is in supplement mode.
VINSPIN_OV	0 = VINS is < VINS_OV_REF 1 = VINS is > VINS_OV_REF	Used to check for VIN OV. Asserts nIRQ when =1 and the function is not masked.
eFUSE_nPG	0 = VIN - VOUT < 200mV 1 = VIN - VOUT > 300mV	When this bit = 1 (drop in output voltage), nIRQ goes low if this function is not masked.
VB/STR_SHORT	0 = VB voltage is greater than BFET_PG 1 = VB voltage is less than BFET_PG	Asserts nIRQ when =1 and the function is not masked.

STATUS2 - Status Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	eFUSE_ILIM_ALERT	eFUSE_OC_SHUTDOWN	LDO_UV	VINSPIN_UV	STR_UV	STR_OV	STR_PG	BKIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
eFUSE_ILIM_ALERT	0 = eFuse current < 90% of overcurrent threshold. 1 = eFuse current > 90% of overcurrent threshold.	Asserts nIRQ when =1 and the function is not masked.
eFUSE_OC_SHUTDOWN	0 = eFuse current is below shutdown level 1 = eFuse current is above shutdown level	Asserts nIRQ when =1 and the function is not masked.
LDO_UV	0 = REF voltage is ready 1 = REF voltage is not ready	Asserts nIRQ when =1 and the function is not masked.
VINSPIN_UV	0 = VINS pin > 0.64V 1 = VINS pin < 0.64V	Asserts nIRQ when = 1 and the function is not masked.
STR_UV	0 = STR voltage is > programmed under voltage limit 1 = STR voltage is < programmed under voltage limit	Asserts nIRQ when =1 and the function is not masked.
STR_OV	0 = STR voltage is < programmed over voltage limit 1 = STR voltage is > programmed over voltage limit	Asserts nIRQ when =1 and the function is not masked.
STR_PG	0 = STR voltage is < 90% of the setpoint 1 = STR voltage is target voltage	Asserts nIRQ when =1 and the function is not masked.
BKIN_UV	0 = STR > 4.0V 1 = STR < 3.6V at supplement state	When this bit = 1 (drop in input voltage), goes to UV/POR state

STATUS3 - Status Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	BUCK_ILIM_SHUTDOWN	BUCK_ILIM_ALERT	BUCK_nPG	BUCK_COMPFAIL	VB_nPG	HCHK_NG	SPLMNT_MODE	BOOTCAPFAIL
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
BUCK_ILIM_SHUTDOWN	0 = Buck peak FET current is less than 140% of the overcurrent threshold set by the I2C register BKILIM_OPT 1 = Buck peak FET current is greater than 140% of the BKILIM_OPT current threshold	When this bit = 1, the IC shuts down the buck converter and enters the UV/POR state
BUCK_ILIM_ALERT	0 = Buck peak FET current is less than the overcurrent threshold set by the I2C register BKILIM_OPT 1 = Buck is above the BKILIM_OPT threshold	Asserts nIRQ when =1 and the function is not masked.
BUCK_nPG	0 = Buck output is above the UV threshold 1 = Buck output is below the UV threshold	When this bit = 1, goes to UV/POR state
BUCK_COMPFAIL	0 = External impedance on COMP pin is ok 1 = COMP pin is shorted	Asserts nIRQ when =1 and the function is not masked.
VB_nPG	0 = Indicates the blocking FET is turned on. 1 = Indicates the blocking FET is turned off.	Asserts nIRQ when =1 and the function is not masked.
HCHK_NG	0 = No error at Health check 1 = Error at Health check	Asserts nIRQ when =1 and the function is not masked.
SPLMNT_MODE	0 = IC not in supplement mode 1 = IC is in supplement mode	Asserts nIRQ when =1. This bit is latched until read.
BOOTCAPFAIL	0 = HSB voltage is ready for switching 1 = HSB voltage is not ready for switching	Asserts nIRQ when =1 and the function is not masked.

RFU – Reserved for Future Use

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU[7:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.

STATUS4 - Status Register

Address = 0x05h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	MSTR_OK	RFU	CMP_BSET_LO	CMP_BSET_HI	RFU[1:0]		PVIN_nUV	eFUSE_ISETLOW
Default	0	0	0	0	00		0	0
Access	RO	RO	RO	RO	RO		RO	RO

Name	Description	Notes
MSTR_OK	0 = Internal bias voltages are not OK 1 = Internal bias are OK	
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
RFU	Reserved for future use	This register always returns a 1 after startup.
CMP_BSET_HI	0 = BSET voltage < 1.2V 1 = BSET voltage > 1.2V	
RFU[1:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
PVIN_nUV	0 = VIN < UVLO 1 = VIN > UVLO	
eFUSE_ISETLOW	0 = ISET pin voltage > 0.1V 1 = ISET pin voltage < 0.1V	

Control Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[2:0]			DISCHG_STR	EN_BFET	EN_STR10mASINK	FORCE_HLTHCHK	FORCE_PWROFF
Default	000			0	0	0	0	0
Access	R/W			R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[2:0]	Reserved for future use	Can write to this register, but it always returns a 0 when read.
DISCHG_STR	0 = Normal Operation 1 = Forces the discharge FET to turn on	Used to manually discharge the storage capacitors via I2C
EN_BFET	0 = Normal Operation 1 = Forces the Blocking FET to turn on even if the ENB pin is low	This register is active when EN_ENB_REG (Register 0x0B bit 3) = 1 and inactive when EN_ENB_REG = 0.
EN_STR10mASINK	0 = Normal Operation 1 = Turns on the 10mA sink current to discharge the storage capacitors	
FORCE_HLTHCHK	0 = Normal operation 1 = Forces a one-shot health check cycle	Forces health check even if EN_HCHK=0. This bit automatically resets to 0 after the health check is completed.
FORCE_PWROFF	0 = Normal operation 1 = Forces IC into the UV/POR state	

RFU – Reserved for Future Use

Address = 0x07h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU[7:0]	Reserved for future use	Always returns 00000000

Masking Register

Address = 0x08h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PVIN_OV_IRQ_MASK	THML_SD_IRQ_MASK	THML_PD_IRQ_MASK	THML_ALERT_IRQ_MASK	FB_nPG_IRQ_MASK	ENPIN_OV_IRQ_MASK	eF_nPG_IRQ_MASK	STR_SHORT_IRQ_MASK
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PVIN_OV_IRQ_MASK	0 – unmasks the PVIN_OV register 1 – masks the PVIN_OV register	When 1, PVIN_OV register will not assert nIRQ. PVIN_OV register still provides a real-time status
THML_SD_IRQ_MASK	0 – unmasks the THERMAL_SHUTDOWN register 1 – masks the THERMAL_SHUTDOWN register	When 1, THERMAL_SHUTDOWN register will not assert nIRQ. THERMAL_SHUTDOWN register still provides a real-time status
THML_PD_IRQ_MASK	0 – unmasks the THERMAL_PWRDOWN register 1 – masks the THERMAL_PWRDOWN register	When 1, THERMAL_PWRDOWN register will not assert nIRQ. THERMAL_PWRDOWN register still provides a real-time status
THML_ALERT_IRQ_MASK	0 – unmasks the THERMAL_ALERT register 1 – masks the THERMAL_ALERT register	When 1, THERMAL_ALERT register will not assert nIRQ. THERMAL_ALERT register still provides a real-time status
FB_nPG_IRQ_MASK	0 – unmasks the FB_nPG register 1 – masks the FB_nPG register	When 1, FB_nPG register will not assert nIRQ. FB_nPG register still provides a real-time status
ENPIN_OV_IRQ_MASK	0 – unmasks the ENPIN_OV register 1 – masks the ENPIN_OV register	When 1, ENPIN_OV register will not assert nIRQ. ENPIN_OV register still provides a real-time status
eF_nPG_IRQ_MASK	0 – unmasks the eF_nPG register 1 – masks the eF_nPG V register	When 1, eF_nPG register will not assert nIRQ. eF_nPG register still provides a real-time status
STR_SHORT_IRQ_MASK	0 – unmasks the STR_SHORT register 1 – masks the STR_SHORT register	When 1, STR_SHORT register will not assert nIRQ. STR_SHORT register still provides a real-time status

Masking Register

Address = 0x09h	Default = 0x1Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	eF_ILIM_ALERT_IRQ_MASK	eF_OC_SD_IRQ_MASK	LDO_UV_IRQ_MASK	ENPIN_UV_IRQ_MASK	STR_UV_IRQ_MASK	STR_OV_IRQ_MASK	STR_PG_IRQ_MASK	BKIN_UV_IRQ_MASK
Default	0	0	0	1	1	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
eF_ILIM_ALERT_IRQ_MASK	0 – unmasks the eFUSE_ILIM_ALERT register 1 – masks the eFUSE_ILIM_ALERT register	When 1, eFUSE_ILIM_ALERT register will not assert nIRQ. eFUSE_ILIM_ALERT register still provides a real-time status
eF_OC_SD_IRQ_MASK	0 – unmasks the eFUSE_OC_SHUTDOWN register 1 – masks the eFUSE_OC_SHUTDOWN register	When 1, eFUSE_OC_SHUTDOWN register will not assert nIRQ. eFUSE_OC_SHUTDOWN register still provides a real-time status
LDO_UV_IRQ_MASK	0 – unmasks the LDO_UV register 1 – masks the LDO_UV register	When 1, LDO_UV register will not assert nIRQ. LDO_UV register still provides a real-time status
ENPIN_UV_IRQ_MASK	0 – unmasks the ENPVIN_UV register 1 – masks the ENPVIN_UV register	When 1, ENPVIN_UV register will not assert nIRQ. ENPVIN_UV register still provides a real-time status
STR_UV_IRQ_MASK	0 – unmasks the STR_UV register 1 – masks the STR_UV register	When 1, STR_UV register will not assert nIRQ. STR_UV register still provides a real-time status
STR_OV_IRQ_MASK	0 – unmasks the STR_OV register 1 – masks the STR_OV register	When 1, STR_OV register will not assert nIRQ. STR_OV register still provides a real-time status
STR_PG_IRQ_MASK	0 – unmasks the STR_PG register 1 – masks the STR_PG register	When 1, STR_PG register will not assert nIRQ. STR_PG register still provides a real-time status
BKIN_UV_IRQ_MASK	0 – unmasks the BKIN_UV register 1 – masks the BKIN_UV register	When 1, BKIN_UV register will not assert BKIN_UV register still provides a real-time status

Masking Register

Address = 0x0Ah	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BK_ILIM_SD_IRQ_MASK	BK_ILIM_ALERT_IRQ_MASK	BK_nPG_IRQ_MASK	BK_COMPFAIL_IRQ_MASK	VB_nPG_IRQ_MASK	HCHK_NG_IRQ_MASK	SPLMNT_IRQ_MASK	BOOTCAPFAIL_IRQ_MASK
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
BK_ILIM_SD_IRQ_MASK	0 – unmasks the BUCK_ILIM_SHUTDOWN register 1 – masks the BUCK_ILIM_SHUTDOWN register	When 1, BUCK_ILIM_SHUTDOWN register will not assert nIRQ. BUCK_ILIM_SHUTDOWN register still provides a real-time status
BK_ILIM_ALERT_IRQ_MASK	0 – unmasks the BUCK_ILIM_ALERT register 1 – masks the BUCK_ILIM_ALERT register	When 1, BUCK_ILIM_ALERT register will not assert nIRQ. BUCK_ILIM_ALERT register still provides a real-time status
BK_nPG_IRQ_MASK	0 – unmasks the BUCK_nPG register 1 – masks the BUCK_nPG register	When 1, BUCK_nPG register will not assert nIRQ. BUCK_nPG register still provides a real-time status
BK_COMPFAIL_IRQ_MASK	0 – unmasks the BUCK_ COMPFAIL register 1 – masks the BUCK_ COMPFAIL register	When 1, BUCK_ COMPFAIL register will not assert nIRQ. BUCK_ COMPFAIL register still provides a real-time status
VB_nPG_IRQ_MASK	0 – unmasks the VB_nPG register 1 – masks the VB_nPG register	When 1, VB_nPG register will not assert nIRQ. VB_nPG register still provides a real-time status
HCHK_NG_IRQ_MASK	0 – unmasks the HCHK_NG register 1 – masks the HCHK_NG register	When 1, HCHK_NG register will not assert nIRQ. HCHK_NG register still provides a real-time status
SPLMNT_IRQ_MASK	0 – unmasks the SPLMNT_MODE register 1 – masks the SPLMNT_MODE register	When 1, SPLMNT_MODE register will not assert nIRQ. SPLMNT_MODE register still provides a real-time status
BOOTCAPFAIL_IRQ_MASK	0 – unmasks the BOOTCAPFAIL register 1 – masks the BOOTCAPFAIL register	When 1, BOOTCAPFAIL register will not assert nIRQ. BOOTCAPFAIL register still provides a real-time status

Control Register

Address = 0x0Bh	Default = 0x24h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	GLOBAL_IRQ_MASK	EN_ENB_REG	EN_DISCHG_UVSTATE	DIS_HEALTH_CHK	HMON_TSET<3:0>			
Default	0	0	1	0	0100			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
GLOBAL_IRQ_MASK	0 – globally enables all MASK bits. 1 – globally masks all MASK bits	When 0, all status register bits are enabled and can assert nIRQ low depending on each of their specific MASK bits. When 1, all status register bits are masked.
EN_ENB_REG	0 = the EN pin controls the blocking FET 1 = EN_BFET register (register 0x06h bit 3) controls the blocking FET	
EN_DISCHG_UVSTATE	0 = Internal DISCHG FET is not enabled when the IC enters the POR/UV state 1 = Internal DISCHG FET is enabled when the IC enters the POR/UV state	
DIS_HEALTH_CHK	0 – Health check is enabled 1 – Health check is disabled	When disabled, Health Check can still be run by writing 1 into FORCE_HCHK
HMON_TSET<3:0>	0000 = 2ms 0001 = 4ms 0010 = 8ms 0011 = 16ms 0100 = 32ms 0101 = 64ms 0110 = 128ms 0111 = 256ms 1000 = 384ms 1001 = 512ms 1010 = 640ms 1011 = 768ms 1100 = 896ms 1101 = 1024ms 1110 = 1152ms 1111 = 1280ms	Sets the Health Check current discharge time.

Control Register

Address = 0x0Ch	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	HMON_THR[3:0]				EN_STARTDLY[2:0]			RFU
Default	0000				001			1
Access	R/W				R/W			R/W

Name	Description	Notes
HMON_THR[3:0]	0000 = 95.0% 0001 = 95.2% 0010 = 95.4% 0011 = 95.6% 0100 = 95.8% 0101 = 96.0% 0110 = 96.2% 0111 = 96.4% 1000 = 96.6% 1001 = 96.8% 1010 = 97.0% 1011 = 97.2% 1100 = 97.4% 1101 = 97.6% 1110 = 97.8% 1111 = 98.0%	Health Check voltage threshold.
EN_STARTDLY[2:0]	000 = not valid. Do not set this register to 000 001 = 1ms 010 = 5ms 011 = 10ms 100 = 20ms 101 = 40ms 110 = 80ms 111 = 125ms	
FACTORY	Factory only register	Do not change this value. Changing this value may result in unexpected IC behavior.

Control Register

Address = 0x0Dh	Default = 0x57h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	BST_CLIM[1:0]		BST_VSET[4:0]				
Default	0	10		10111				
Access	R/W	R/W		R/W				

Name	Description		Notes
RFU	Reserved for future use		Can write to this register, but it always returns a 0 when read.
BST_CLIM[1:0]	00 = 250mA 01 = 500mA 10 = 950mA 11 = 1500mA		Sets the boost convert peak switch current.
BST_VSET[4:0]	00000 = 5V 00001 = 5.6V 00010 = 7V 00011 = 8V 00100 = 9V 00101 = 10V 00110 = 11V 00111 = 12V 01000 = 13V 01001 = 14V 01010 = 15V 01011 = 16V 01100 = 17V 01101 = 18V 01110 = 19V 01111 = 20V	10000 = 21V 10001 = 22V 10010 = 23V 10011 = 24V 10100 = 25V 10101 = 26V 10110 = 27V 10111 = 28V 11000 = 28V 11001 = 28V 11010 = 28V 11011 = 28V 11100 = 28V 11101 = 28V 11110 = 28V 11111 = 28V	STR voltage set point

Control Register

Address = 0x0Eh	Default = 0x79h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FACTORY[4:0]					VINS_OV_REF[2:0]		
Default	01111					001		
Access	R/W					R/W		

Name	Description	Notes
FACTORY[4:0]	Factory only registers	Do not change these values. Changing these values may result in unexpected IC behavior.
VINS_OV_REF[2:0]	000 = Disable 001 = 0.82V 010 = 0.92V 011 = 1.00V 100 = 1.08V 101 = 1.16V 110 = 1.24V 111 = 1.32V	VINS_OV_REF reference voltage.

Control Register

Address = 0x0Fh	Default = 0x92h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	STR_UV_TH[1:0]		RFU	BKILIM_OPT	FACTORY[1:0]		BKUV_TH[1:0]	
Default	10		0	1	00		10	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
STR_UV_TH[1:0]	00 = 90% 01 = 92.5% 10 = 95% 11 = 97.5%	Sets the storage voltage under voltage threshold
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
BKILIM_OPT	0 = 3A 1 = 6A	Adjusts the buck converter's peak current limit value.
FACTORY[1:0]	Factory only registers	Do not change these values. Changing these values may result in unexpected IC behavior.
BKUV_TH[1:0]	00 = 60% 01 = 70% 10 = 80% 11 = 90%	Sets the buck output voltage under voltage threshold.

Control Register

Address = 0x10h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BK_FREQ[1:0]		RFU[1:0]		SCALE_TSET_2x	SCALE_TSET_4x	SCALE_HCHK_2x	SCALE_HCHK_4x
Default	01		00		0	0	0	0
Access	R/W		R/W		R/W	R/W	R/W	R/W

Name	Description	Notes
BK_FREQ[1:0]	00 = 562kHz 01 = 1.125MHz 10 = 1.5MHz 11 = 2.25MHz	Buck switching frequency in supplement mode.
RFU[1:0]	RFU	Reserved for future use
SCALE_TSET_2x	0 – Normal HMON_TSET 1 – HMON_TSET timing slowed by 2x	SCALE_TSET_2x takes priority over SCALE_TSET_4x. The timing is slowed by 2x if both registers = 1.
SCALE_TSET_4x	0 – Normal HMON_TSET 1 – HMON_TSET timing slowed by 4x	SCALE_TSET_2x takes priority over SCALE_TSET_4x. The timing is slowed by 2x if both registers = 1.
SCALE_HCHK_2x	0 – Health check performed every 4 minutes 1 – Health check performed every 8 minutes	SCALE_TSET_2x takes priority over SCALE_TSET_4x. The timing is scaled to 8 minutes if both registers = 1.
SCALE_HCHK_4x	0 – Health check performed every 4 minutes 1 – Health check performed every 16 minutes	SCALE_TSET_2x takes priority over SCALE_TSET_4x. The timing is scaled to 8 minutes if both registers = 1.

Masking Register

Address = 0x11h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Mask_BKIN_nUV	Mask_eF_OC	Mask_eF_ILIM	Mask_LDO_FAULT	Mask STR_OV	Mask STR_UV	Mask_BK_OV	Mask_BK_UV
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
Mask_BKIN_nUV	0 – Normal operation 1 – Prevents IC from changing states when the buck input voltage (storage voltage) goes below 3.6V.	
Mask_eF_OC	0 – Normal operation 1 – Prevents IC from changing states when the eFuse goes overcurrent.	
Mask_eF_ILIM	0 – Normal operation 1 – Prevents IC from changing states when the eFuse current goes above ISET threshold.	
Mask_LDO_FAULT	0 – Normal operation 1 – Prevents IC from changing states when the LDO has a fault	
Mask STR_OV	0 – Normal operation 1 – Prevents IC from changing states when the storage voltage goes over voltage.	
Mask STR_UV	0 – Normal operation 1 – Prevents IC from changing states when the storage voltage goes under voltage.	
Mask_BK_OV	0 – Normal operation 1 – Prevents IC from changing states when the buck voltage goes over voltage.	
Mask_BK_UV	0 – Normal operation 1 – Prevents IC from changing states when the buck voltage goes under voltage.	

RFU Register

Address = 0x12h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU[7:0]	Reserved for future use	Always returns 00000000

DEVICE ID – Device ID Register

Address = 0x2Ah	Default = 0x00h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DEVICE ID [7:0]							
Default	0x00h							
Access	RO							

Name	Description	Notes
DEVICE ID [7:0]	8 bit word to identify the CMI in the IC. Refer to IC DS for Device IDs.	