PAC5524 Device User Guide

Power Application Controller®

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

Arm® Cortex®-M4F Controller Core

active-semi®
Solutions for Sustainability

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1 OVERVIEW

This document is the PAC5524 Device User Guide. It details the operation of the analog peripherals in the PAC5524.

For detailed information on the MCU and Digital Peripherals in the PAC5524, see the *PAC55XX Family User Guide*.

2 STYLE AND FORMATTING CONVENTIONS

This chapter describes the formatting and styles used throughout this document.

2.1 Number Representation

Numbers other than decimal will have a postfix indicator. All numbers use little endian formatting, with the most significant bit/digit to the left. Digits for binary and hexadecimal representation are grouped with a single space every four digits to improve readability. Binary numbers use “b” as a postfix and hexadecimal numbers use “h” as a postfix.

For example, 1011b binary = Bh hexadecimal = 11 decimal.

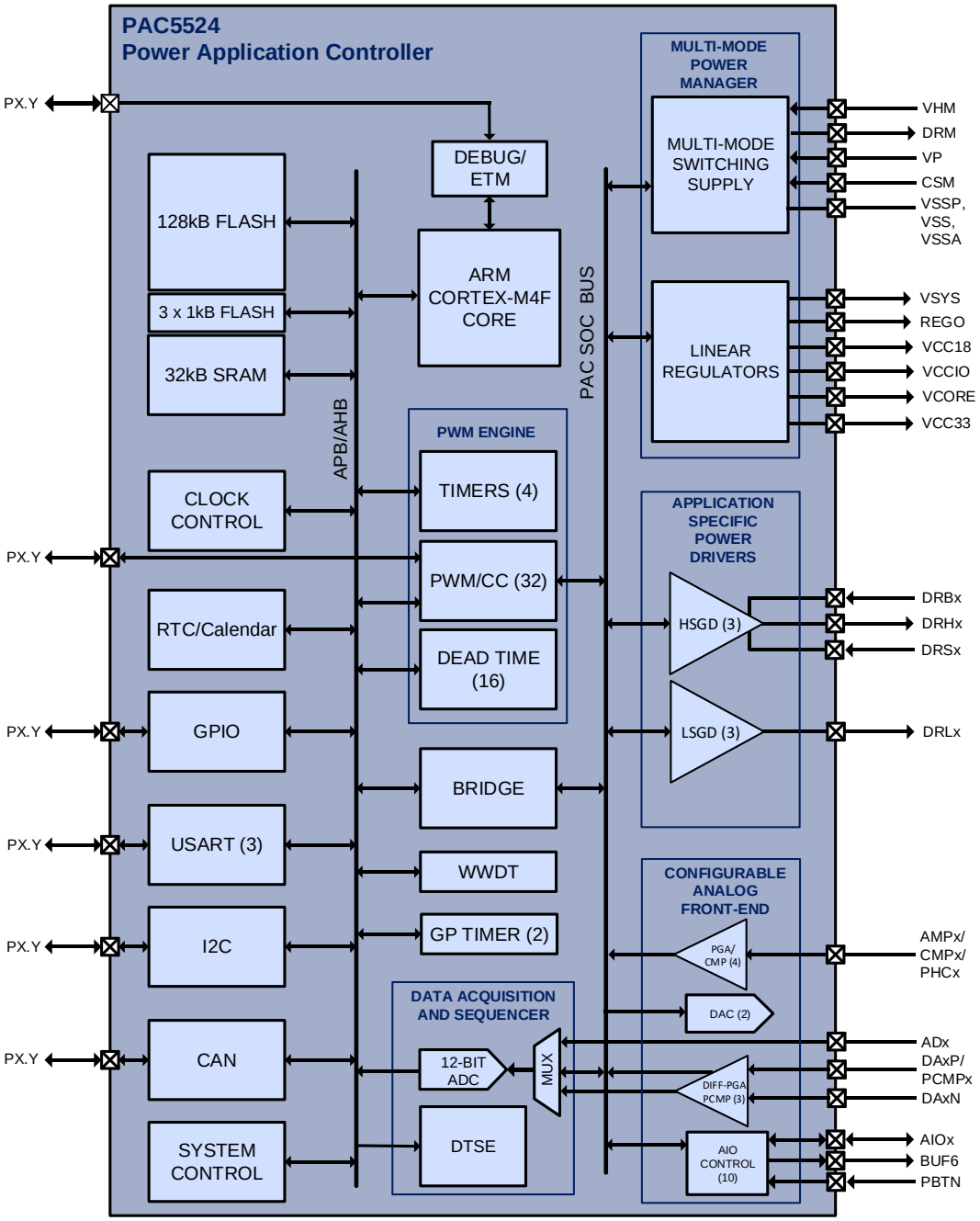
2.2 Formatting Styles

TYPE	EXAMPLE	DESCRIPTION
Register Name	**RTCCTL**	Register names use a capital letter and **boldface** type.
Register Bit(s)	**RTCCTL.RTCCLKDIV**	Register bits are always represented with the register name separated with a period.
Function selected by register bit(s)	**[RTCCTL.RTCCLKDIV]**	Within text blocks, functions selected with a register bit setting are set in brackets. For example **[RTCCTL.RTCCLKDIV]** means divider settings /2 to /65536.
Pin Function	PA5	Pin functions use capital letters
Internal signals	*PWMA3*	Internal signals use *italicized* font.
Formulas	`CLK = FCLK / DIV`	Formulas use `monospaced` text.
Links	Link	Hyperlinks are underlined and blue.
CPU Mnemonic	`MRS`	CPU Mnemonic uses `monospaced` text.
Operands	*`{Rd, }, Rn, Rm`*	Operands use *`monospaced italic`* text.
Code examples	`b loopA`	Code examples use monospaced text.

3 ARCHITECTURAL BLOCK DIAGRAM

For Below is an architecture block diagram of the PAC5524 device.

Figure 3-1 PAC5524 Architectural Block Diagram



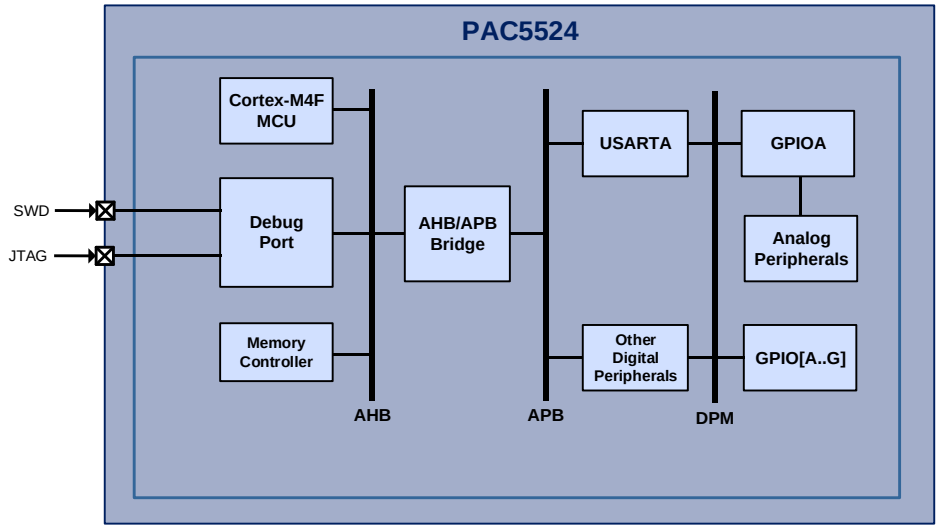
4 ANALOG REGISTER ACCESS

4.1 Overview

All analog registers in the PAC5524 are accessible through a SOC bus in the device. Unlike registers in the MCU (SRAM and digital peripheral registers), these analog registers are not memory mapped.

The block diagram below shows the different system busses that the MCU uses to access the different system registers.

Figure 4-1 PAC5524 Register Access



The PAC5524 contains two register buses: the AHB bus and the APB bus.

The AHB bus allows the MCU and Debug Port access to FLASH and SRAM via the Memory Controller. To access other digital peripheral connected to the APB bus, there is a bridge from the AHB to the APB bus so that the MCU or Debug Port can perform memory-mapped register access to all digital peripherals. Some digital peripherals such as timers are flexibly connected to IO using the DPM bus.

To access the Analog peripherals, the USARTA SPI peripheral is used to generate read and write transactions to the Analog registers using the DPM and GPIOA.

4.2 Functional Description

External programming interfaces such as JTAG and SWD or the Arm® Cortex®-M4F MCU may perform memory-mapped accesses to USART A through the AHB and APB busses on the device.

USART A is a serial communication peripheral that supports a SPI-like protocol that can be used to communicate to the Analog Peripherals for read and write transactions. The Digital Peripheral MUX (DPM) may be configured to connect the USART A SPI signals to GPIO A, where they are connected to the Analog peripherals.

4.3 USART Configuration

USART A acts as a SPI bus master to communicate with the Analog Peripherals. The USART A signals that are used for this communication are:

- *USASCLK* – USART A SPI Clock
- *USAMOSI* – USART A Master-Out/Slave-In
- *USAMISO* – USART A Master-In/Slave-Out
- *USASS* – USART A Slave Select

In order to communicate with the Analog Peripherals, the USART A should have the following configuration:

- 8-bit mode
- SCLK active high
- CPH is sample/setup
- SS active low

When communicating with the Analog Peripherals, the maximum SCLK frequency is 25MHz.

4.4 Protocol

The protocol for communicating with the Analog Peripherals is a simple two-byte protocol.

The first byte is always the address, which includes a 7-bit address [7:1] and a write bit [0]. For write operations, the write bit [0] is set to 1b. For read operations, the write bit [0] is set to 0b.

For write operations, the 2nd byte will be the 8-bit data to write to the given address.

For read operations, the 2nd byte is ignored and MISO will contain the 8-bit data read from the given address.

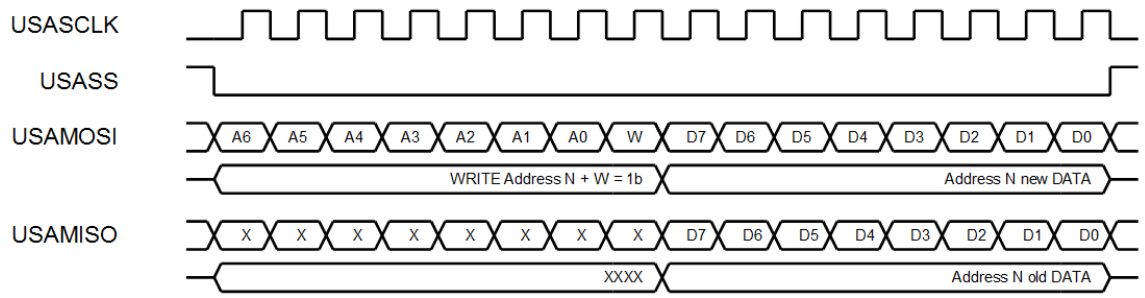
4.5 Write Register Example

To write the **HPDAC** register (address 2Bh) with the value 28h, issue the following transactions to USART A:

- Write **SSPADAT** with the value 57h (2Bh << 1 | 1b for write transaction)
- Write **SSPADAT** with the value 28h

The timing diagram from a write operation is shown below.

Figure 4-2 Analog Peripheral Register Write Timing



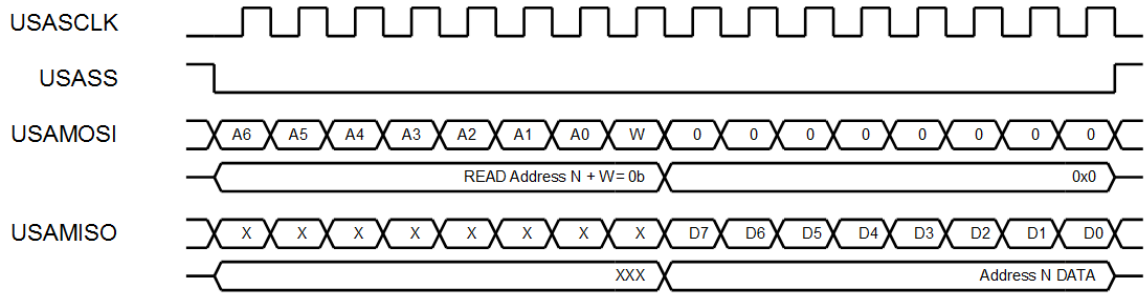
4.6 Read Register Example

To read the contents of the **HPDAC** register, issue the following transactions to USART A:

- Write **SSPADAT** with the value 56h (2Bh << 1 | 0b for read transaction)
- Write **SSPADAT** with a dummy character
- Read last data from MISO from **SSPADAT**, this is the register value

The timing diagram from a read operation is shown below.

Figure 4-3 Analog Peripheral Register Read Timing



For more information on how to configure the DPM to support the USART A peripheral for communicating with the Analog Registers, see the PAC55XX Family User Guide.

5 PAC5524 IO

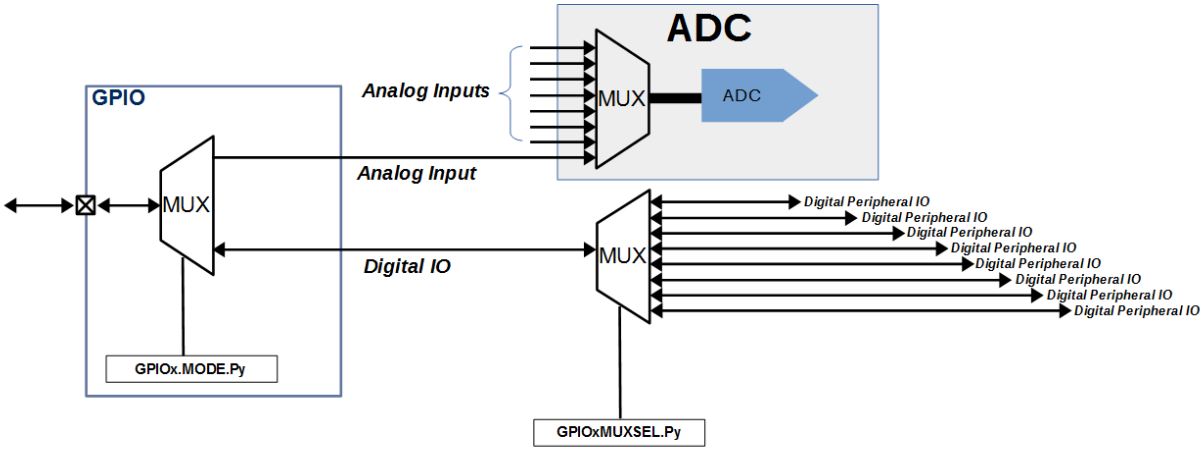
5.1 Overview

The Digital Peripheral MUX (DPM) on the PAC55XX family allows flexible assignment of peripheral functions to IO pins.

Each member of the family has a different set of IO pins that are available. It is important during application design that the designer consider the available IO pins to make sure the necessary peripherals will be available.

Below is a diagram of the GPIO and MUX structure.

Figure 5-1 GPIO and DPM Block Diagram



Each IO can be configured to select 1 of up to 8 digital peripheral signals. Some IOs also may be used as an ADC input. For information on how to configure the IO for each of these situations, see the PAC55XX Family User Guide.

The PAC5524 has the following IO pins available for application use:

- PA[7:0] – Reserved for MMPM, ASPD, CAFE
- PB[7:0] – Reserved for ASPD
- PC[7:0]
- PD[6:0]
- PE[3:0]
- PF[6:0]
- PG[3:0]

5.2 ADC Channels

The ADC channels that are available on the PAC5524 are shown in the table below.

Table 5-1 PAC5524 ADC Input Pins

ADC Channel	IO PIN
ADC0	PG7[1]
ADC1	PD3
ADC2	PD2
ADC3	PD1
ADC4	PD0/PF4
ADC5	PF5
ADC6	PF6
ADC7	PF7

[1] Available for sampling channels in the CAFE only

5.3 Digital Peripheral Pins

The digital peripheral functions that are available in the PAC5524 are shown below.

Table 5-2 PAC5524 Digital Peripheral Pins

PORT	Pin	GPIOxMUXS.Py							
		000b	001b	010b	011b	100b	101b	110b	111b
GPIOA	P0	**GPIOA0**							
	P1	GPIOA1	**EMUXD**						
	P2	GPIOA2	**EMUXC**						
	P3	GPIOA3	**USASCLK**	USBSCLK					
	P4	GPIOA4	**USAMOSI**	USBMOSI					
	P5	GPIOA5	**USAMISO**	USBMISO					
	P6	GPIOA6	**USASS**	USBSS					
	P7	**GPIOA7**							
GPIOB	P0	**GPIOB0**	TAPWM0	TBPWM0		TCPWM0	TDPWM0		
	P1	**GPIOB1**	TAPWM1	TBPWM1		TCPWM1	TDPWM1		
	P2	**GPIOB2**	TAPWM2	TBPWM2		TCPWM2	TDPWM2		
	P4	**GPIOB4**	TAPWM4	TBPWM4		TCPWM4	TDPWM4		
	P5	**GPIOB5**	TAPWM5	TBPWM5		TCPWM5	TDPWM5		
	P6	**GPIOB6**	TAPWM6	TBPWM6		TCPWM6	TDPWM6		
GPIOC	P0	**GPIOC0**	TBPWM0	TCPWM0	TBQEPIDX	USBMOSI	USCSCLK	CANRXD	I2CSCL
	P1	**GPIOC1**	TBPWM1	TCPWM1	TBQEPPHA	USBMISO	USCSS	CANTXD	I2CSDA
	P2	**GPIOC2**	TBPWM2	TCPWM2	TBQEPPHB	USBSCLK	USCMOSI		EMUXD
	P3	**GPIOC3**	TBPWM3	TCPWM3		USBSS	USCMISO		EMUXC
	P4	**GPIOC4**	TBPWM4	TCPWM4	TCQEPIDX	USBMOSI	USCSCLK	CANRXD	I2CSCL
	P5	**GPIOC5**	TBPWM5	TCPWM5	TCQEPPHA	USBMISO	USCSS	CANTXD	I2CSDA
	P6	**GPIOC6**	TBPWM6	TCPWM6	TCQEPPHB	USBSCLK	USCMOSI		EMUXD
	P7	**GPIOC7**	TBPWM7	TCPWM7		USBSS	USCMISO	FRCLK	EMUXC
GPIOD	P0	**GPIOD0**	TBPWM0	TCPWM0	TDQEPIDX		USCSCLK	CANTXD	EMUXD
	P1	**GPIOD1**	TBPWM1	TCPWM1	TDQEPPHA		USCSS	CANRXD	EMUXC
	P2	**GPIOD2**	TBPWM2	TCPWM2	TDQEPPHB		USCMOSI		
	P3	**GPIOD3**	TBPWM3	TCPWM3			USCMISO	FRCLK	TRACED3
	P4	**GPIOD4**	TBPWM4	TCPWM4	TDQEPIDX	TBQEPIDX	USDSCLK	TRACED3	USDMOSI
	P5	**GPIOD5**	TBPWM5	TCPWM5	TDQEPPHA	TBQEPPHA	USDSS	CANRXD	USDMISO
	P6	**GPIOD6**	TBPWM6	TCPWM6	TDQEPPHB	TBQEPPHB	USDMOSI	CANTXD	I2CSDA

GPIOE	**P0**	**GPIOE0**	TCPWM4	TDPWM0	TAQEPIDX	TBQEPIDX	USCSCLK	I2CSCL	EMUXC
	P1	**GPIOE1**	TCPWM5	TDPWM1	TAQEPPHA	TBQEPPHA	USCSS	I2CSDA	EMUXD
	P2	**GPIOE2**	TCPWM6	TDPWM2	TAQEPPHB	TBQEPPHB	USCMOSI	CANRXD	EXTCLK
	P3	**GPIOE3**	TCPWM7	TDPWM3	FRCLK		USCMISO	CANTXD	
GPIOF	**P0**	GPIOF0	TCPWM0	TDPWM0	**TMS/SWDCLK**	TBQEPIDX	USBSCLK	TRACECLK	
	P1	GPIOF1	TCPWM1	TDPWM1	**TMS/SWDIO**	TBQEPPHA	USBSS	TRACED0	
	P2	GPIOF2	TCPWM2	TDPWM2	**TDI**	TBQEPPHB	USBMOSI	TRACED1	
	P3	GPIOF3	TCPWM3	TDPWM3	**TDO**	FRCLK	USBMISO	TRACED2	
	P4	**GPIOF4**	TCPWM4	TDPWM4		TCQEPIDX	USDSCLK	TRACED3	EMUXC
	P5	**GPIOF5**	TCPWM5	TDPWM5		TCQEPPHA	USDSS		EMUXD
	P6	**GPIOF6**	TCPWM6	TDPWM6		TCQEPPHB	USDMOSI	CANRXD	I2CSCL
	P7	**GPIOF7**	TCPWM7	TDPWM7			USDMISO	CANTXD	I2CSDA
GPIOG	**P0**	**GPIOG0**	TCPWM0	TDPWM0	EMUXC		USDSCLK	TRACECLK	TCQEPIDX
	P1	**GPIOG1**	TCPWM1	TDPWM1	EMUXD		USDSS	TRACED0	TCQEPPHA
	P2	**GPIOG2**	TCPWM2	TDPWM2	FRCLK		USDMOSI	TRACED1	TCQEPPHB
	P3	**GPIOG3**	TCPWM3	TDPWM3			USDMISO	TRACED2	

For more information on how to configure the DPM for the PAC5524, see the PAC55XX Family User Guide.

6 MULTI-MODE POWER MANAGER

6.1 Overview

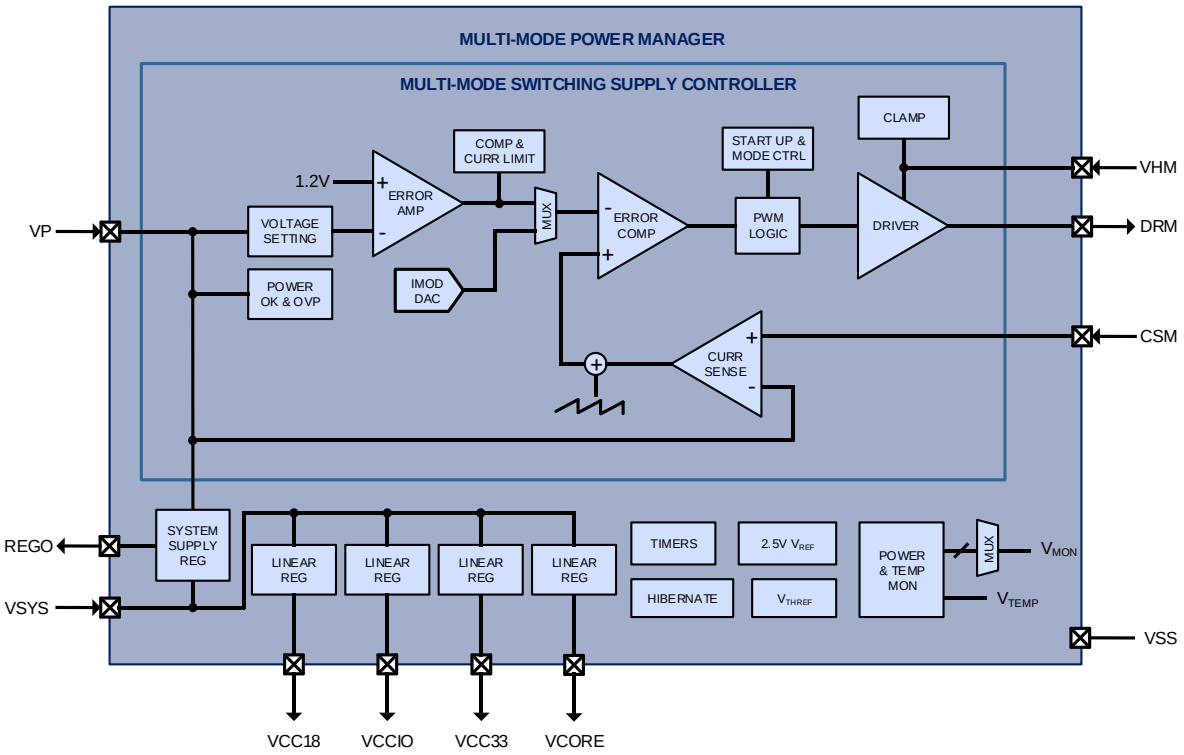
The Multi-Mode Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a buck or SEPIC converter to efficiently con vert power from a DC input source to generate a main supply output V_P. Four linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CORE} supplies for 5V system, 3.3V I/O, 3.3V mixed signal, and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

6.2 Features

- Multi-mode switching supply controller configurable as Buck or SEPIC
- DC supply up to 70V input
- Direct DC input of up to 20V with no DC/DC
- 4 linear regulators with power and hibernate management, including V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

6.3 System Block Diagram

Figure 6-1 MMPM System Block Diagram



6.4 Functional Description

The Multi-Mode Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a BUCK or SEPIC DC/DC controller to efficiently convert power from a DC input source to generate a main supply output V_P. Four linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CORE} supplies for 5V system, 3.3V I/O, 3.3V mixed signal, and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

6.5 Register Summary

Table 6-1 MMPM Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
00h	**SYSSTAT**	System Status	00h
10h	**PWRCTL**	Power Manager Control	00h
11h	**PWRSTAT**	Power Manager Status	-
12h	**PWRSET**	Power Manager Setting	00h
14h	**SCFG**	Switching Supply Configuration	00h
15h	**PWRCFG**	Power Manager Configuration	Varies

6.6 Register Detail

6.6.1 SYSSTAT

Register 6-1SYSSTAT (Analog System Status, SOC 00h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**PBSTAT**	RW	0x0	Push button status. When not masked, bit set on interrupt and cleared when written to 1b. When masked, bit is transparent.
6	**TMPWARN**	R	0x0	Temperature warning to indicate the temperature is over 140°c. When **TMPWARN** is not masked, this bit is latch when temperature is out of valid range and cleared when bit is read. When masked, bit is transparent.
5:4	**VTHREF**	RW	0x0	Programmable threshold voltage. Used for AMP6 through AMP9 in comparator mode. 00b: 0.1V 01b: 0.2V 10b: 0.5V 11b: 1.25V
3	**RFU**	RO	0x0	Reserved
2	**nPBMSK**	RW	0x0	Push-button interrupt mask (active low). 0b: masked 1b: not masked
1	**FLTM**	RW	0x0	Fault mask (active high). Set to 1b to mask temperature fault. 0b:not masked 1b: masked
0	**nINTM**	RW	0x0	Interrupt mask (active low). Temperature warning will trigger the interrupt. 0b: masked 1b: not masked

6.6.2 PWRCTL

Register 6-2 PWRCTL (Power Manager Control, 10h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HIB**	RW	0x0	Hibernate mode. This bit is cleared and power up sequence is initiated after the wake up timer delay or external event. 0b: normal 1b: shutdown mode
6	**MCUALIVE**	RW	0x0	Micro-controller alive flag. Bit that MCU can set in the Power Manager to indicate that it has already initialized itself. Can be used by MCU to detect that it has been reset by the AFE. The convention is for the MCU to write this bit to 1b on initialization of the AFE, and test that it is not 1 during start-up.
5:3	**PWRMON**	RW	0x0	Power monitor select. Selects the voltage signal for power monitoring at A/D converter on AB11: 000b: V_{CORE} 001b: V_{CC33} scaled by 4/10 010b: V_{CCIO} scaled by 4/10 011b: V_{SYS} scaled by 4/10 100b: V_{REGO} scaled by 1/10 101b: V_P scaled by 1/10 110b: Reserved 111b: V_{COMP} internal error amplifier output
2:0	**WUTIMER**	RW	0x0	Wake-up timer delay. 000b: infinite 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

6.6.3 PWRSTAT

Register 6-3 PWRSTAT (Power Manager Status, 11h, Persistent in Hibernate Mode)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HWRSTAT**	R	-	Hardware reset status. When not masked, bit is set on Hardware Reset and cleared when written to 1b.
6	**WDTRSTAT**	R	-	Watchdog timer reset status. When enabled, it is set on Watchdog Timer Reset and cleared when written to 1b.
5	**MMSSFLT**	R	-	Multi-mode switching supply fault status. Bit set on fault and cleared when written to 1b.
4	**TMPFLT**	R	-	Temperature fault status. Bit set on fault and cleared when written to 1b.
3	**VSYSFLT**	R	-	V_{SYS} fault status. Bit set on fault and cleared when written to 1b.
2	**VCCIOFLT**	R	-	V_{CCIO} fault status. Bit set on fault and cleared when written to 1b.
1	**VCC33FLT**	R	-	V_{CC33} fault status. Bit set on fault and cleared when written to 1b.
0	**VCC18FLT**	R	-	V_{CC18} fault status. Bit set on fault and cleared when written to 1b.

6.6.4 PWRSET

Register 6-4 PWRSET (Power Manager Setting, 12h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**UNLOCK**	RW	0x0	Software unlock. Write to 1b to enable writing to **SCFG** and **PWRCFG**. 0b: **SCFG** locked 1b: **SCFG** unlocked
6	**nSU**	RW	0x0	Start-up bit. This bit is cleared to 0b on power-on reset by the device. This bit will retain its state during hibernate mode if the power supply on VHM remains on. This bit may be use by firmware to indicate if power-up is through power-on reset or hibernate if the user sets it to 1b before entering hibernate mode.
5	**VPLOW**	RW1C	0x0	V_p low status. When not masked, bit set on interrupt and cleared when written to 1b.
4	**GP**	RW	0x0	General purpose bit. This bit will return its state during hibernate mode if the power supply on VHM remains on.
3	**nVPINTM**	RW	0x0	V_p low interrupt mask (active low). 0b: mask 1b: not masked
2	**TWD**	RW	0x0	Watchdog timer delay. 0b: 8s 1b: 4s
1	**WDTEN**	RW	0x0	Watchdog timer enable. 0b: disabled 1b: enabled
0	**PBEN**	RW	0x0	Push button enable. 0b: disabled 1b: enabled

6.6.5 SCFG

Register 6-5 SCFG (Switching Supply Configuration, 14h)

BIT	NAME	ACCESS[2]	RESET	DESCRIPTION
7	**SRST**	RW	0x0	Soft reset. Write to 1b to assert nRST and generate system soft reset. 0b: normal 1b: reset
6	**DIGCTL**	RW	0x0	Digital control enable. 0b: disabled 1b: enabled
5	**VCLAMPSEL**	RW	0x0	V_{HM} voltage clamp selection. 0b: 20V 1b: 62V
4	**FMODE**	RW	0x0	Frequency mode. 0b: low frequency range (45kHz to 125kHz) 1b: high frequency range (181kHz to 500kHz)
3:1	**FSWM**	RW	0x0	Switching frequency. **FMODE** = 0b / **FMODE** = 1b 000b: 45kHz / 000b: 181kHz 001b: 50kHz / 001b: 200kHz 010b: 55kHz / 010b: 220kHz 011b: 62.5kHz / 011b: 250kHz 100b: 72.25kHz / 100b: 289kHz 101b: 82.5kHz / 101b: 330kHz 110b: 100kHz / 110b: 400kHz 111b: 125kHz / 111b: 500kHz
0	**DMAX**	RW	0x0	Maximum duty. 0b: 500ns minimum off time 1b: 75% maximum duty

[2] This byte is unlocked for writing when **UNLOCK** = 1b.

6.6.6 PWRCFG

Register 6-6 PWRCFG (Power Status Configuration, 15h)

BIT	NAME	ACCESS[3]	RESET	DESCRIPTION
7:6	**VP**	RW	10b	VP voltage setting when DC/DC is enabled. 00b: Reserved 01b: 9V 10b: 12V 11b: 15V
5	**SMPSOFF**	RW	0	DC/DC enable configuration: 0b: DC/DC enabled 1b: DC/DC disabled
4	**Reserved**	RW	0	Reserved, write as 0.
3	**TRST**	RW	0	Reset time after POR for MCU: 0b: 1ms 1b: 32ms
2:1	**Reserved**	RW	0	Reserved, write as 0.
0	**TDB**	RW	0	Push-button de-bouncing timer. 0b: 16ms 1b: 32ms

[3] Reset value for VP voltage setting varies. Consult the data sheet for the device for the reset value.

7 CONFIGURABLE ANALOG FRONT-END

7.1 Overview

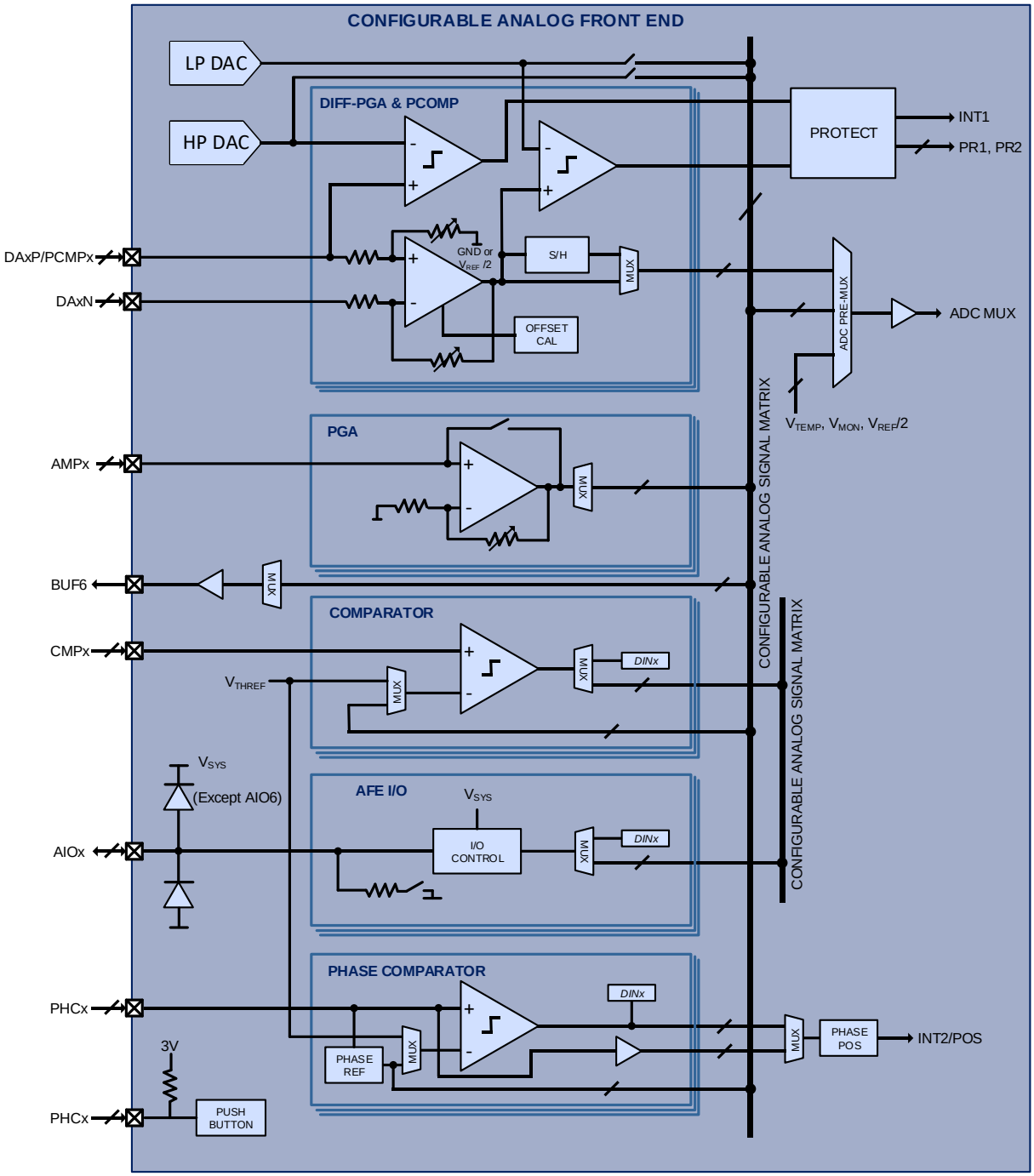
The PAC5524 includes a Configurable Analog Front End accessible through 8 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 10 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

7.2 Features

- 10 Analog Front-End IO pins
- 3 Differential Programmable Gain Amplifiers
- 4 Single-ended Programmable Gain Amplifiers
- Programmable Over-Current Protection
- 10 Comparators
- 2 DACs (10-bit and 8-bit)
- Integrated BEMF comparator mode with virtual center-tap
- Integrated BEMF phase to phase comparator
- Programmable comparator hysteresis and blanking time

7.3 System Block Diagram

Figure 7-1 CAFE System Block Diagram



7.4 Functional Description

7.4.1 Enabling the CAFE

Before the CAFE sub-system can be signal sampling, it must be enabled.

To enable this sub-system, set **SMCTL.SMEN** to 1b.

7.4.2 Integrated Temperature Sensor

The PAC5524 contains an integrated temperature sensor that can be sampled on the AB10 analog bus. To read the temperature, sample this ADC channel and convert the ADC counts to °C using the following formula:

°C = ((ADC counts – **TTEMPS**) >> 1) + **FTTEMP**.

The variables **TTEMPS** and **FTTEMP** can be found in INFO-1 memory.

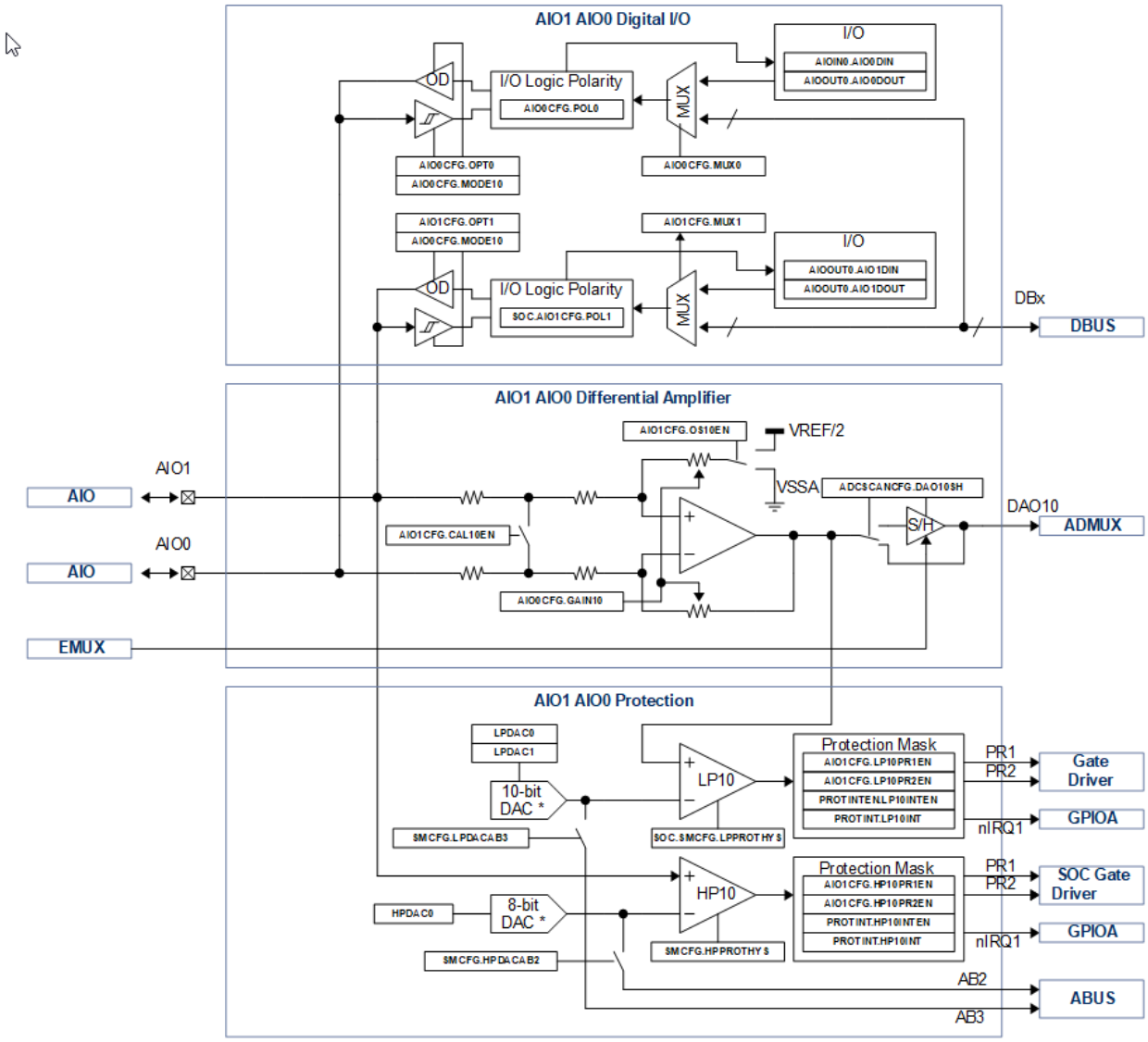
For more information on these variables, see the PAC55XX Family User Guide.

7.5 AIO10

AIO10 may be configured as digital inputs or as a differential amplifier with protection.

7.5.1 System Block Diagram

Figure 7-2 AIO10 Block Diagram



7.5.2 AIO0 IO Mode

To configure AIO0 to be digital input, set **CFGAIO0.MODE10** to 00b and set **CFGAIO0.OPT0** to 00b. The state of the input may be read from **AIOIN0.DIN0**.

To configure AIO0 as an open drain output, set **CFGAIO0.MODE10** to 00b and **CFGAIO0.OPT0** to 10b. Set **CFGAIO0.MUX0** to 00b to MUX the output state from **AIOOUT0.DOUT0.** **CFGAIO0.MUX0** may be used to MUX the output signal from DBUS DB1 to DB7.

To set the polarity of AIO0 between the IO and MUX0, use **AIO0CFG.POL0**.

7.5.3 AIO1 IO Mode

To configure AIO1 to be digital input, set **CFGAIO0.MODE10** to 00b and set **CFGAIO1.OPT1** to 00b. The state of the input may be read from **AIOIN0.DIN1**.

To configure AIO1 as an open drain output, set **CFGAIO0.MODE10** to 00b and **CFGAIO1.OPT1** to 10b. Set **CFGAIO1.MUX1** to 00b to MUX the output state from **AIOIN0.DIN1.** **CFGAIO1.MUX1** may be used to MUX the output signal from DBUS DB1 to DB7.

To set the polarity of AIO1 between the IO and MUX1, use **CFGAIO1.POL1**.

7.5.4 AIO10 Differential Amplifier Mode

To configure AIO10 for Differential Amplifier Mode, set **CFGAIO0.MODE10** = 10b.

The gain of the differential amplifier may be set between 1X to 48X using **CFGAIO0.GAIN10**.

When in Differential Amplifier mode, the reference may be set to either VSSA or VREF/2. To configure the reference use **AIO1CFG.OS10EN**. To short the input of the differential amplifier to allow reading of the amplifier offset, set **AIO1CFG.CAL10EN** to 1b.

7.5.5 AIO10 Protection

When AIO10 is in Differential Amplifier mode (**AIO0CFG.MODE10** = 10b), the high-side protection comparator HP10 and the low-side protection comparator LP10 are also active. These protection comparators may be configured to disable the high-side or low-side gate drivers in the Application Specific Power Drivers™ (ASPD) block.

7.5.6 HP10 Protection Comparator

The HP10 comparator takes the AIO1 voltage referenced to VSSA and compares it against the HPDAC voltage. The 8-bit HPDAC is programmable using **HPDAC**.

The HP10 comparator blanking times may be configured to 1μs, 2μs, 4μs or disabled by using **CFGAIO1.HP10OPT**. The HP10 comparator hysteresis may be enabled by setting **SMCFG.HPROTHYS** to 1b.

The output of the HP10 comparator may be configured to trigger protection signal PR1 using **CFGAIO1.HP10PR1EN** and PR2 using **CFGAIO1.HP10PR2EN**.

The output of HP10 may also trigger the nIRQ1 interrupt to the MCU by using **PROTINTEN.HP10INTEN**. The interrupt status may be observed with **PROTINT.HP10INT**.

7.5.7 LP10 Protection Comparator

The LP10 comparator takes the output of the differential amplifier and compares it against the LPDAC voltage. The 10-bit LPDAC is programmable with **LPDAC0** and **LPDAC1**.

The LP10 comparator blanking times may be configured to 1μs, 2μs, 4μs or disabled by using **CFGAIO0.LP10OPT**. The LP10 comparator hysteresis may be enabled by setting **SMCFG.LPROTHYS** to 1b.

The output of the LP10 comparator may be configured to trigger protection signal PR1 using **CFGAIO1.LP10PR1EN** and PR2 using **CFGAIO1.LP10PR2EN**.

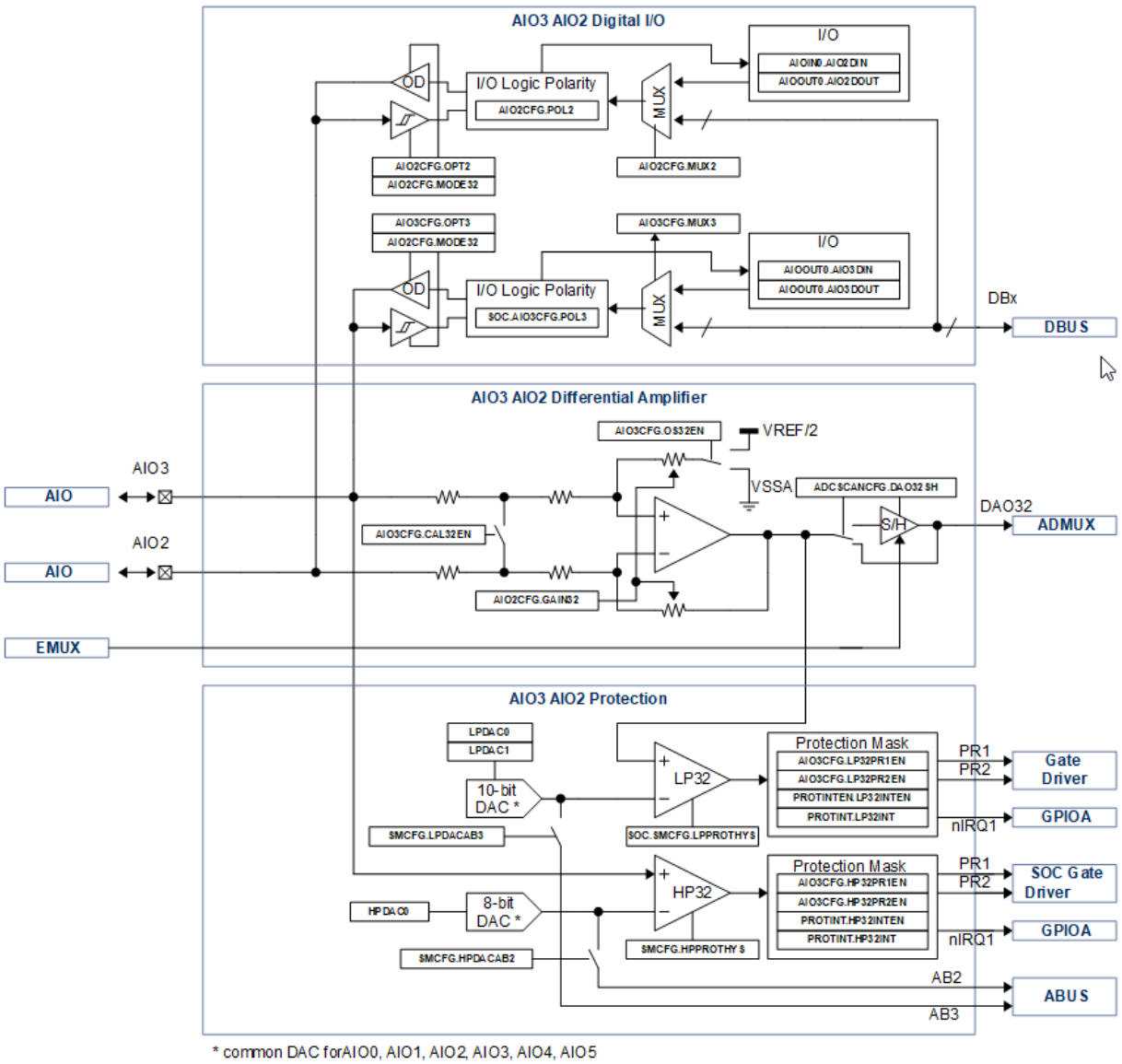
The output of LP10 may also trigger the nIRQ1 interrupt to the MCU by using **PROTINTEN.LP10INTEN**. The interrupt status may be observed with **PROTINT.LP10INT**.

7.6 AIO32

AIO32 may be configured as digital inputs or as a differential amplifier with protection.

7.6.1 System Block Diagram

Figure 7-3 AIO32 Block Diagram



* common DAC forAIO0, AIO1, AIO2, AIO3, AIO4, AIO5

7.6.2 AIO2 IO Mode

To configure AIO2 to be digital input, set **CFGAIO2.MODE32** to 00b and set **CFGAIO2.OPT2** to 00b. The state of the input may be read from **AIOIN0.DIN2**.

To configure AIO2 as an open drain output, set **CFGAIO2.MODE32** to 00b and **CFGAIO2.OPT2** to 10b. Set **CFGAIO2.MUX2** to 00b to MUX the output state from **AIOOUT0.DOUT2. CFGAIO2.MUX2** may be used to MUX the output signal from DBUS DB1 to DB7.

To set the polarity of AIO2 between the IO and MUX2, use **CFGAIO2.POL2**.

7.6.3 AIO3 IO Mode

To configure AIO3 to be digital input, set **CFGAIO2.MODE32** to 00b and set **CFGAIO3.OPT3** to 00b. The state of the input may be read from **AIO1IN.DIN3**.

To configure AIO3 as an open drain output, set **CFGAIO2.MODE32** to 00b and **CFGAIO3.OPT3** to 10b. Set **CFGAIO3.MUX3** to 00b to MUX the output state from **AIOOUT0.DOUT3. CFGAIO3.MUX3** may be used to MUX the output signal from DBUS DB1 to DB7.

To set the polarity of AIO3 between the IO and MUX3, use **CFGAIO3.POL3**.

7.6.4 AIO32 Differential Amplifier Mode

To configure AIO32 for Differential Amplifier Mode, set **CFGAIO2.MODE32** = 10b.

The gain of the differential amplifier may be set between 1X to 48X using **CFGAIO2.GAIN32**.

When in Differential Amplifier mode, the reference may be set to either VSSA or VREF/2. To configure the reference use **CFGAIO3.OS32EN**. To short the input of the differential amplifier to allow reading of the amplifier offset, set **CFGAIO3.CAL32EN** to 1b.

7.6.5 AIO32 Protection

When AIO32 is in Differential Amplifier mode (**CFGAIO2.MODE32** = 10b), the high-side protection comparator HP32 and the low-side protection comparator LP32 are also active. These protection comparators may be configured to disable the high-side or low-side gate drivers in the Application Specific Power Drivers™ (ASPD) block.

7.6.6 HP32 Protection Comparator

The HP32 comparator takes the AIO3 voltage referenced to VSSA and compares it against the HPDAC voltage. The 8-bit HPDAC is programmable using **HPDAC**.

The HP32 comparator blanking times may be configured to 1μs, 2μs, 4μs or disabled by using **CFGAIO3.HP32OPT**. The HP32 comparator hysteresis may be enabled by setting **SMCFG.HPROTHYS** to 1b.

The output of the HP32 comparator may be configured to trigger protection signal PR1 using **CFGAIO3.HP32PR1EN** and PR2 using **CFGAIO3.HP32PR2EN**.

The output of HP32 may also trigger the nIRQ1 interrupt to the MCU by using **PROTINTEN.HP32INTEN**. The interrupt status may be observed with **PROTINT.HP32INT**.

7.6.7 LP32 Protection Comparator

The LP32 comparator takes the output of the differential amplifier and compares it against the LPDAC voltage. The 10-bit LPDAC is programmable with **LPDAC0** and **LPDAC1**.

The LP32 comparator blanking times may be configured to 1μs, 2μs, 4μs or disabled by using **CFGAIO2.LP32OPT**. The LP32 comparator hysteresis may be enabled by setting **SMCFG.LPROTHYS** to 1b.

The output of the LP32 comparator may be configured to trigger protection signal PR1 using **CFGAIO3.LP32PR1EN** and PR2 using **CFGAIO3.LP32PR2EN**.

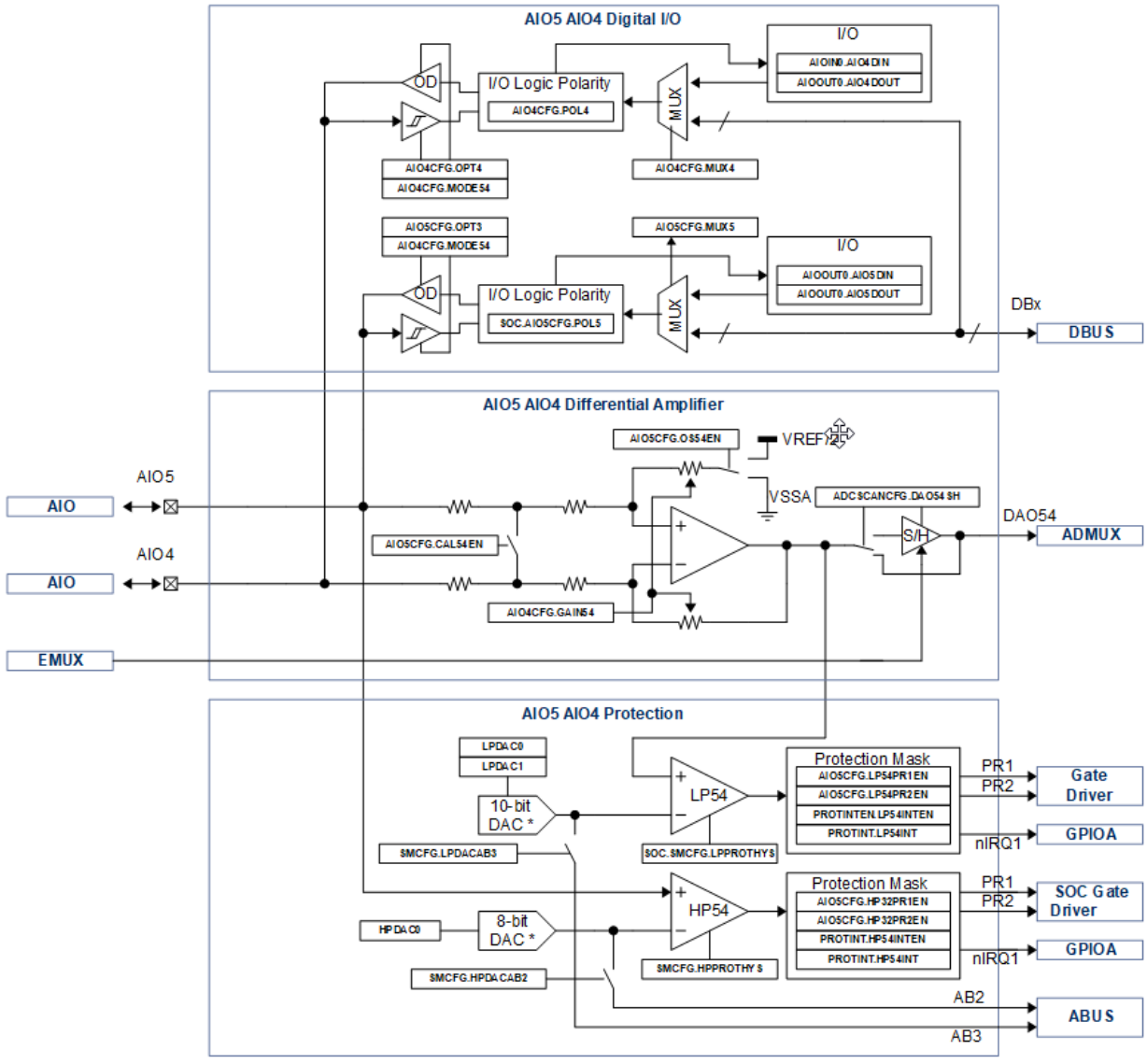
The output of LP32 may also trigger the nIRQ1 interrupt to the MCU by using **PROTINTEN.LP32INTEN**. The interrupt status may be observed with **PROTINT.LP32INT**.

7.7 AIO54

AIO54 may be configured as digital inputs or as a differential amplifier with protection.

7.7.1 System Block Diagram

Figure 7-4 AIO54 Block Diagram



* common DAC forAIO0, AIO1, AIO2, AIO3, AIO4, AIO5

7.7.2 AIO4 IO Mode

To configure AIO4 to be digital input, set **CFGAIO4.MODE54** to 00b and set **CFGAIO4.OPT4** to 00b. The state of the input may be read from **AIO0IN.DIN4**.

To configure AIO4 as an open drain output, set **CFGAIO4.MODE54** to 00b and **CFGAIO4.OPT4** to 10b. Set **CFGAIO4.MUX4** to 00b to MUX the output state from **AIOOUT0.DOUT4. CFGAIO4.MUX4** may be used to MUX the output signal from DBUS DB1 to DB7.

To set the polarity of AIO4 between the IO and MUX2, use **CFGAIO4.POL4**.

7.7.3 AIO5 IO Mode

To configure AIO5 to be digital input, set **CFGAIO4.MODE54** to 00b and set **CFGAIO5.OPT5** to 00b. The state of the input may be read from **AIO1IN.AIO5DIN**.

To configure AIO5 as an open drain output, set **CFGAIO5.MODE54** to 00b and **CFGAIO5.OPT5** to 10b. Set **CFGAIO5.MUX5** to 00b to MUX the output state from **AIOOUT0.DOUT5. CFGAIO5.MUX5** may be used to MUX the output signal from DBUS DB1 to DB7.

To set the polarity of AIO5 between the IO and MUX5, use **CFGAIO5.POL5**.

7.7.4 AIO54 Differential Amplifier Mode

To configure AIO54 for Differential Amplifier Mode, set **CFGAIO4.MODE54** = 10b.

The gain of the differential amplifier may be set between 1X to 48X using **CFGAIO5.GAIN54**.

When in Differential Amplifier mode, the reference may be set to either VSSA or VREF/2. To configure the reference use **CFGAIO5.OS54EN**. To short the input of the differential amplifier to allow reading of the amplifier offset, set **CFGAIO5.CAL54EN** to 1b.

7.7.5 AIO54 Protection

When AIO54 is in Differential Amplifier mode (**CFGAIO4.MODE54** = 10b), the high-side protection comparator HP54 and the low-side protection comparator LP54 are also active. These protection comparators may be configured to disable the high-side or low-side gate drivers in the Application Specific Power Drivers™ (ASPD) block.

7.7.6 HP54 Protection Comparator

The HP54 comparator takes the AIO5 voltage referenced to VSSA and compares it against the HPDAC voltage. The 8-bit HPDAC is programmable using **HPDAC**.

The HP54 comparator blanking times may be configured to 1μs, 2μs, 4μs or disabled by using **CFGAIO5.HP54OPT**. The HP54 comparator hysteresis may be enabled by setting **SMCFG.HPROTHYS** to 1b.

The output of the HP54 comparator may be configured to trigger protection signal PR1 using **CFGAIO5.HP54PR1EN** and PR2 using **CFGAIO5.PR2EN**.

The output of HP54 may also trigger the nIRQ1 interrupt to the MCU by using **PROTINTEN.HP54INTEN**. The interrupt status may be observed with **PROTINT.HP54INT**.

7.7.7 LP54 Protection Comparator

The LP54 comparator takes the output of the differential amplifier and compares it against the LPDAC voltage. The 10-bit LPDAC is programmable with **LPDAC0** and **LPDAC1**.

The LP54 comparator blanking times may be configured to 1μs, 2μs, 4μs or disabled by using **CFGAIO4.LP54OPT**. The LP54 comparator hysteresis may be enabled by setting **SMCFG.LPROTHYS** to 1b.

The output of the LP54 comparator may be configured to trigger protection signal PR1 using **CFGAIO5.LP54PR1EN** and PR2 using **CFGAIO5.LP54PR2EN**.

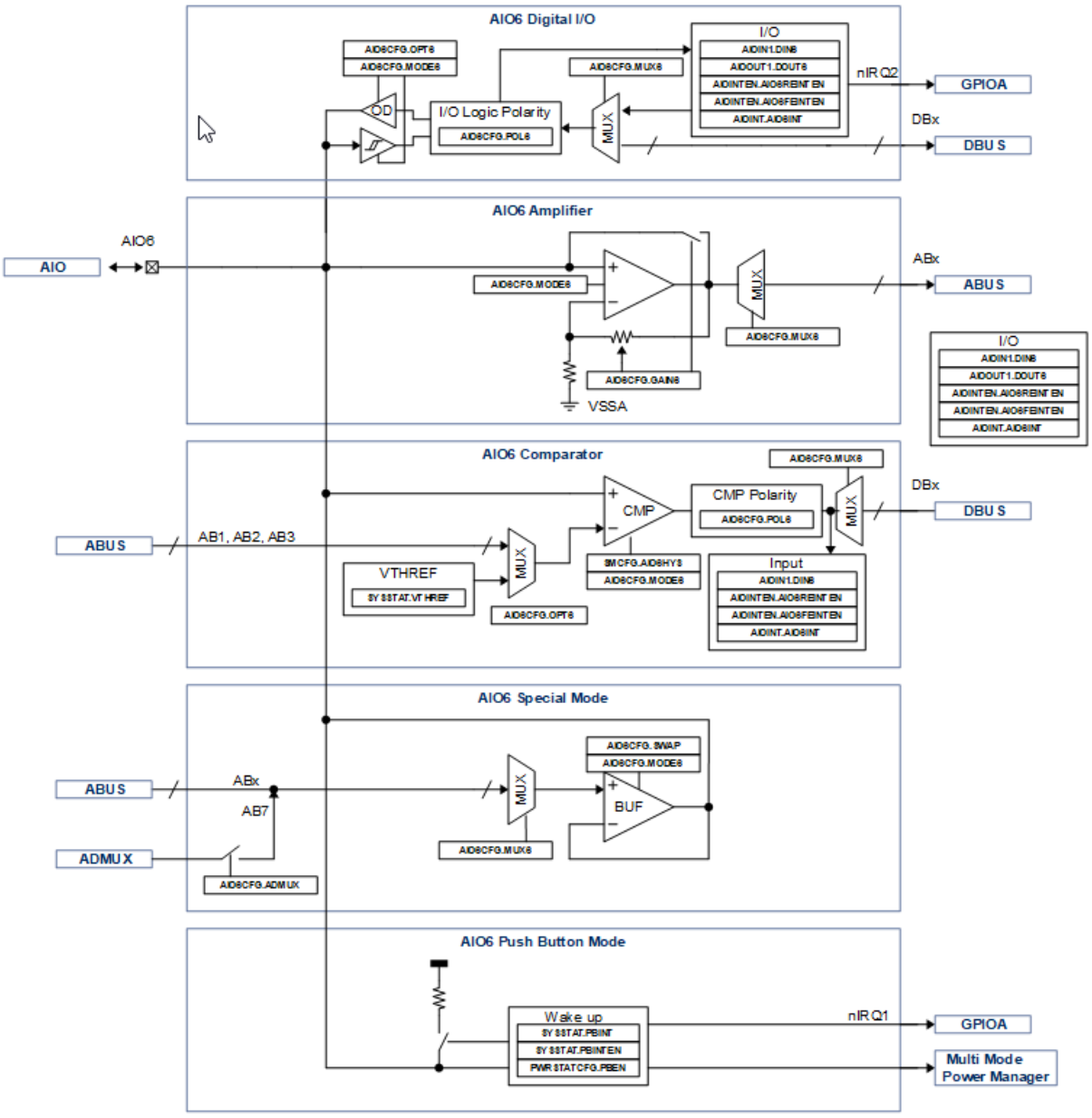
The output of LP54 may also trigger the nIRQ1 interrupt to the MCU by using **PROTINTEN.LP54INTEN**. The interrupt status may be observed with **PROTINT.LP54INT**.

7.8 AIO6

AIO6 may be configured as a digital input, single-ended programmable gain amplifier, comparator, output from analog ABUS or as a push-button input to wake up the device from total hibernate mode.

7.8.1 System Block Diagram

Figure 7-5 AIO6 System Block Diagram



7.8.2 AIO6 IO Mode

To configure AIO6 for IO mode, set **PWRSET.PBEN** to 0b and **CFGAIO6.MODE6** to 00b.

To use AIO6 as a digital input, set **CFGAIO6.OPT6** to 00b. The digital input state may be read from **AIOIN1.DIN6**.

To use AIO6 as an open-drain output, set **CFGAIO6.OPT6** to 10b. Set **CFGAIO6.MUX6** to 00b to MUX the output state from **AIOOUT1.DOUT6**. Use **CFGAIO6.MUX6** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

To generate an interrupt on nIRQ2 on an AIO6 low to high transition, set **AIOINTEN.AIO6REINTEN** to 1b.

To generate an interrupt on nIRQ2 on an AIO6 high-to-low transition, set **AIOINTEN.AIO6FEINTEN** to 1b.

To set the polarity between AIO6 and MUX6 when in IO mode, use **CFGAIO6.POL6**.

7.8.3 AIO6 Gain Amplifier Mode

To configure AIO6 for gain amplifier mode, set **PWRSET.PBEN** to 0b and **CFGAIO6.MODE6** to 01b.

In this mode, the gain of the amplifier can be set between 1X and 48X. To set the gain, set **CFGAIO6.GAIN6** to the desired value. To switch the output of the amplifier to analog channel AB1 to AB7 on the ABUS, set **CFGAIO6.MUX6** to the desired channel.

7.8.4 AIO6 Comparator Mode

To configure AIO6 for comparator mode, set **PWRSET.PBEN** to 0b and **CFGAIO6.MODE6** to 10b.

In this mode, the comparator hysteresis may be enabled by setting **SMCFG.AIO6HYS** to 1b, and disabled by writing this field to 0b.

The compare value of this comparator can be set to AB1, AB2, AB3 or VTHREF. To select the compare value, set **CFGAIO6.OPT6**. The VTHREF may be set by using **SYSSTAT.VTHREF**.

The output polarity of the comparator may be set by setting **CFGAIO6.POL6** to the desired value.

The output of the comparator may be configured by setting the **CFGAIO6.MUX6**. The output can be set to DB1 to DB7 or to **AIOIN1.DIN6**.

7.8.5 AIO6 Special Mode

In special mode, AIO6 can output a buffered signal from the internal ABUS AB1 to AB7. To configure AIO6 for special mode, set **PWRSET.PBEN** to 0b and **CFGAIO6.MODE6** to 11b.

To set the ABUS channel output to AIO6, use **CFGAIO6.MUX6**. To set the ADMUX output to AB7, set **CFGAIO6.ADMUX**. To swap the random offset of the buffer for calibration, use **CFGAIO6.SWAP**.

7.8.6 AIO6 Push-Button Mode

AIO6 can be used as a push-button input to exit the system from hibernate mode. To configure AIO6 for push-button input mode, set **PWRSET.PBEN** to 1b. When in hibernate mode, AIO6 has a weak pull-up.

To enable the nIRQ interrupt, set **PWRSTAT.PBINTEN** to 1b. **PWRSTAT.PBINT** may be used to monitor the interrupt status. To clear the interrupt, write **PWRSTAT.PBINT** to 1b.

The push-button de-bouncing period may be set by unlocking the **PWRCFG** register (write **PWRSET.UNLOCK** to 1b) and then by setting **PWRCFG.TDB** to the de-bouncing period (16ms or 32ms).

If the AIO6 push-button mode is active during hibernate mode, if AIO6 is pulled low for the de-bouncing period then **PWRCTL.HIB** is cleared and the device powers up.

During normal operation, the system may enter hibernate mode when AIO6 is pulled low for the de-bouncing period. The system can also be put into hibernate mode by setting **PWRCTL.HIB** to 1b.

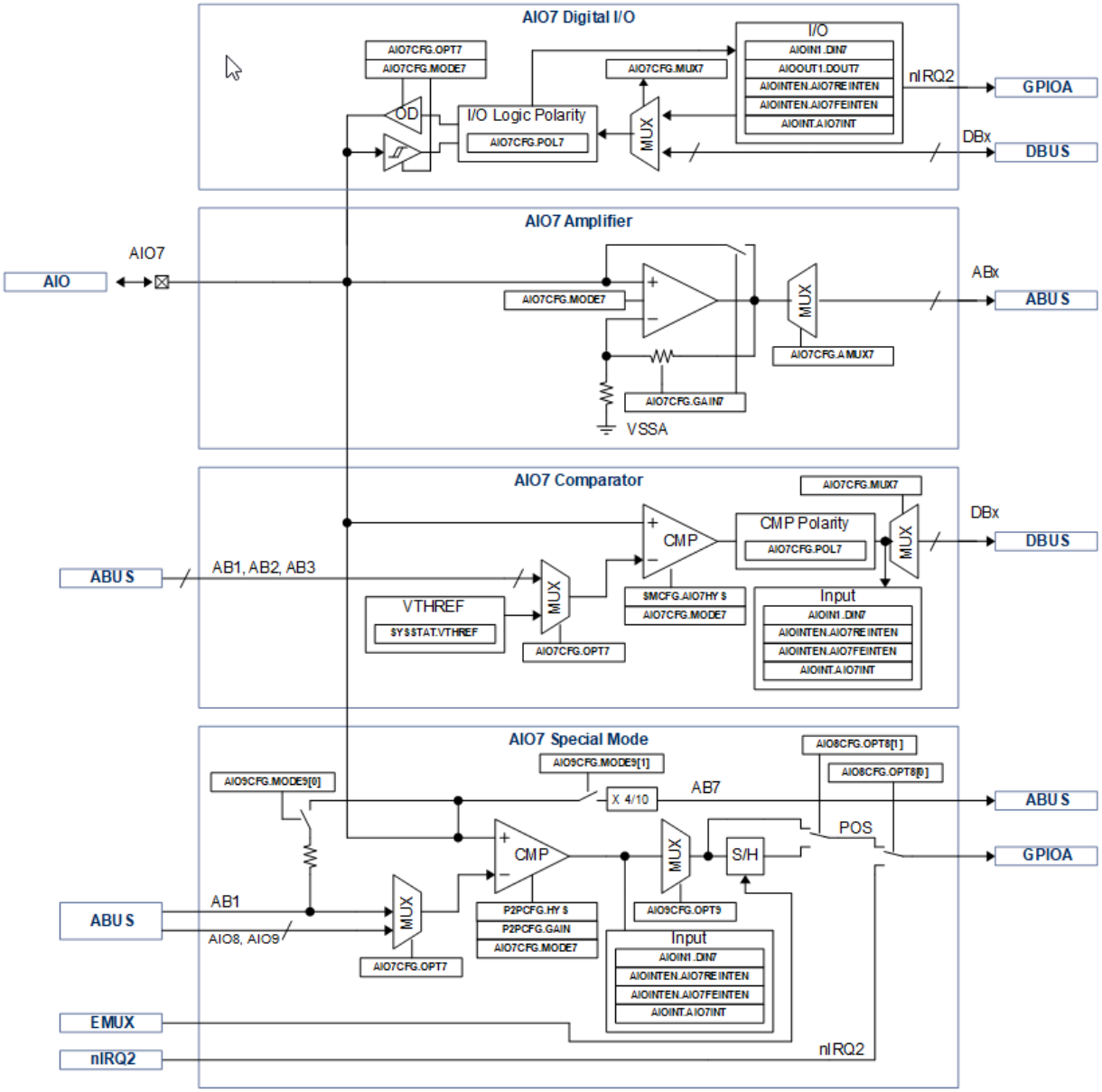
Push-button mode also has a hard-reset function. If AIO6 is pulled low for more than 8 seconds, the reset signal will be asserted and the MCU will perform a reset. The **PWRSTAT.HWRESET** bit will be set to indicate this condition.

7.9 AIO7

AIO7 may be configured as a digital input, single-ended programmable gain amplifier, comparator or output from analog ABUS.

7.9.1 System Block Diagram

Figure 7-6 AIO7 System Block Diagram



7.9.2 AIO7 IO Mode

To configure AIO7 for as a digital input, set **CFGAIO7.MODE7** to 00b and set **CFGAIO7.OPT7** to 00b. The digital input state may be read from **AIOIN1.DIN7**.

To configure AIO7 as an open-drain output, set **CFGAIO7.MODE7** to 00b and set **CFGAIO7.OPT7** to 10b. Set **CFGAIO7.MUX7** to 00b to MUX the output state from **AIOOUT1.DOUT7**. Use **CFGAIO7.MUX7** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

To generate an interrupt on nIRQ2 on an AIO7 low to high transition, set **AIOINTEN.AIO7REINTEN** to 1b.

To generate an interrupt on nIRQ2 on an AIO7 high-to-low transition, set **AIOINTEN.AIO7FEINTEN** to 1b.

To set the polarity between AIO7 and MUX7 when in IO mode, use **CFGAIO7.POL7**.

7.9.3 AIO7 Gain Amplifier Mode

To configure AIO7 for gain amplifier mode, set **CFGAIO7.MODE7** to 01b.

In this mode, the gain of the amplifier can be set between 1X and 48X. To set the gain, set **CFGAIO7.GAIN7** to the desired value. To switch the output of the amplifier to analog channel AB1 to AB7 on the ABUS, set **CFGAIO7.MUX7** to the desired channel.

7.9.4 AIO7 Comparator Mode

To configure AIO7 for comparator mode, set **CFGAIO7.MODE7** to 10b.

In this mode, the comparator hysteresis may be enabled by setting **SMCFG.AIO7HYS** to 1b, and disabled by writing this field to 0b.

The compare value of this comparator can be set to AB1, AB2, AB3 or VTHREF. To select the compare value, set **CFGAIO7.OPT7**. The VTHREF may be set by using **SYSSTAT.VTHREF**.

The output polarity of the comparator may be set by setting **CFGAIO7.POL7** to the desired value.

The output of the comparator may be configured by setting the **CFGAIO7.MUX7**. The output can be set to DB1 to DB7 or to **AIOIN1.DIN7**.

7.9.5 AIO7 Special Mode

In special mode, the AIO7 comparator is enabled. To configure AIO7 for special mode, set **CFGAIO7.MODE7** to 11b.

In special mode, AIO7 allows the user to configure bi-directional asymmetric comparator hysteresis. See the section below for more information.

The user may set the AIO7 comparator input to AB1, AB2, AB3 or VTHREF. The user may also use the comparator for phase to phase comparisons by setting the comparator input to AIO8 or AIO9. The user may configure the comparator input by setting **SOC.CFGAIO7.OPT7** to the desired value.

In special mode, AIO7 allows the user to configure the comparator star point.

Set **CFGAIO9.MODE9[0]** to 1b to connect AIO7, AIO8 and AIO9 to AB1 with a 100kOhm resistor to create a star point reference for the comparator.

Set **CFGAIO9.MODE9[0]** to 0b to set the AB1 reference to come from AIO6 in amplifier mode. To set AIO6 to amplifier mode, set **CFGAIO6.MODE6** to 01b and **CFGAIO6.GAIN6** to 000b for direct mode, and **CFGAIO6.MUX6** to 1b.

To read the voltage on AIO7, set **CFGAIO9.MODE9[1]** to 1b. This setting will MUX AIO7 to AB7 with 40% attenuation so the ADC can read the AIO7 voltage.

To read the comparator output for AIO7, AIO8 or AIO9 for position (POS), set **CFGAIO9.OPT9** to the desired value.

The AIO7 Sample and Hold (S/H) bypass may be configured as well. To bypass the POS S/H, set **CFGAIO8.OPT8[1]** to 0b. To use POS S/H for use with the EMUX, set **CFGAIO8.OPT8[0]** to the 1b.

To select the POS or nIRQ2 output, set the **CFGAIO8.OPT8[0]** to the desired value.

When configured in special mode, the user may select the comparator input using a MUX by writing the **CFGAIO7.MUX** field. The table below shows the comparator input selections that may be used.

Table 7-1 AIO7 Special Mode Comparator Input Selections

CFGAIO7.MODE	AIO Mode	CFGAIO7.MUX	Comparator Input MUX Select	Function
11b	Special Mode	000b	VTHREF	Fixed Threshold
		001b	AB1	Virtual Center-tap for BEMF Zero-Cross
		010b	AB2	
		011b	AB3	
		100b	AIO8	Phase to phase
		101b	AIO9	Phase to phase
		110b	RFU	
		111b	RFU	

The user may configure the comparator hysteresis separately for rising and falling hysteresis as shown in the table below.

Table 7-2 AIO7 Phase to Phase Comparator Hysteresis Configuration

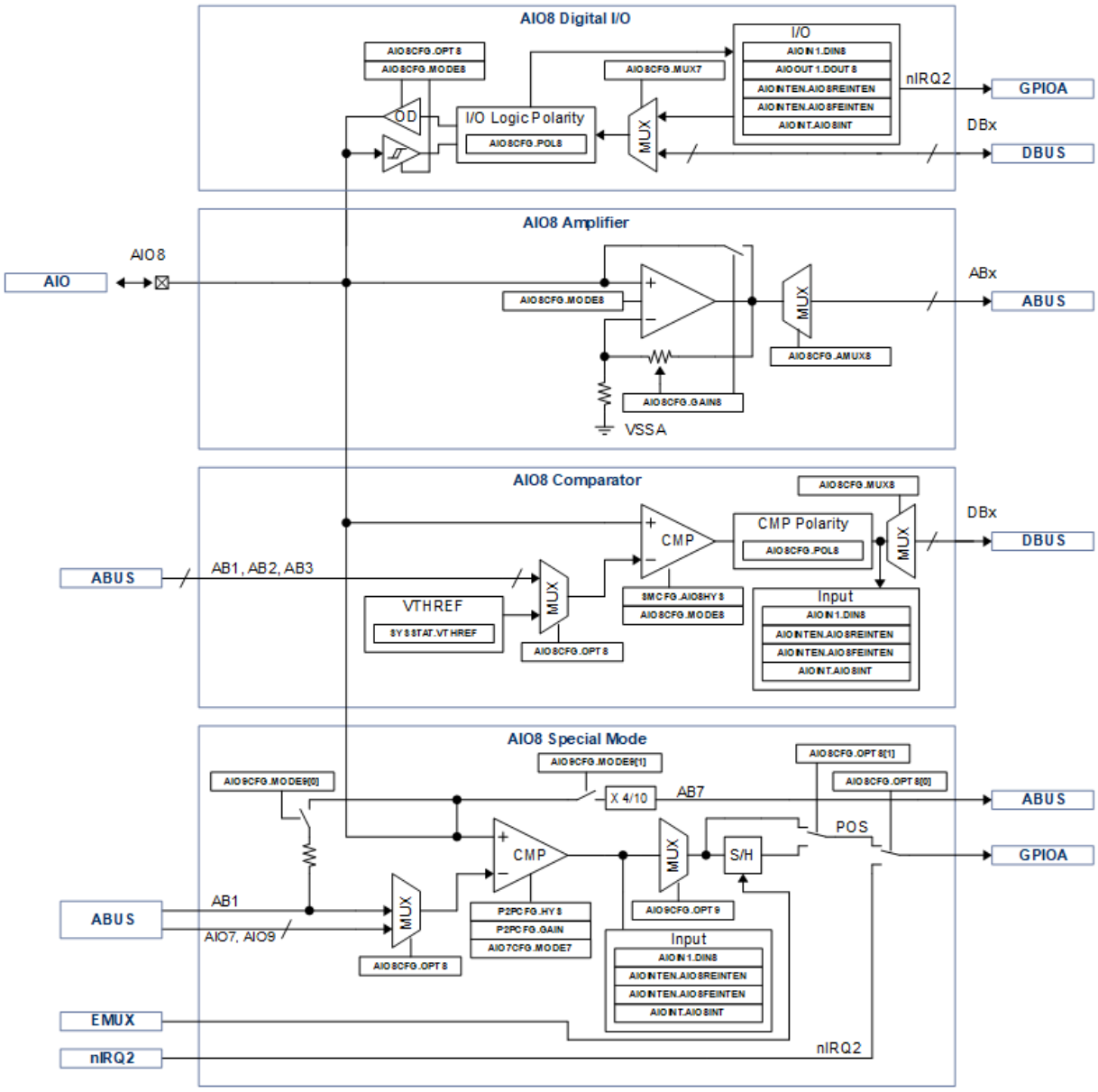
SPECFG2.HYSAIO7	SIGSET.HYSMODE	Rising Hysteresis	Falling Hysteresis
0000b	0b	0 mV	0 mV
0001b		0 mV	10 mV
0010b		0 mV	20 mV
0011b		0 mV	40 mV
0100b		10 mV	0 mV
0101b		10 mV	10 mV
0110b		10 mV	20 mV
0111b		10 mV	40 mV
1000b		20 mV	0 mV
1001b		20 mV	10 mV
1010b		20 mV	20 mV
1011b		20 mV	40 mV
1100b		40 mV	0 mV
1101b		40 mV	10 mV
1110b		40 mV	20 mV
1111b		40 mV	40 mV
0000b	1b	0 mV	0 mV
0001b		0 mV	35 mV
0010b		0 mV	70 mV
0011b		0 mV	140 mV
0100b		35 mV	0 mV
0101b		35 mV	35 mV
0110b		35 mV	70 mV
0111b		35 mV	140 mV
1000b		70 mV	0 mV
1001b		70 mV	35 mV
1010b		70 mV	70 mV
1011b		70 mV	140 mV
1100b		140 mV	0 mV
1101b		140 mV	35 mV
1110b		140 mV	70 mV
1111b		140 mV	140 mV

7.10 AIO8

AIO8 may be configured as a digital input, single-ended programmable gain amplifier, comparator or output from analog ABUS.

7.10.1 System Block Diagram

Figure 7-7 AIO8 System Block Diagram



7.10.2 AIO8 IO Mode

To configure AIO8 for as a digital input, set **CFGAIO8.MODE8** to 00b and set **CFGAIO8.OPT8** to 00b. The digital input state may be read from **AIOIN1.DIN8**.

To configure AIO8 as an open-drain output, set **CFGAIO8.MODE8** to 00b and set **CFGAIO8.OPT8** to 10b. Set **CFGAIO8.MUX8** to 00b to MUX the output state from **AIOOUT1.DOUT8**. Use **CFGAIO8.MUX8** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

To generate an interrupt on nIRQ2 on an AIO8 low to high transition, set **AIOINTEN.AIO8REINTEN** to 1b.

To generate an interrupt on nIRQ2 on an AIO8 high-to-low transition, set **AIOINTEN.AIO8FEINTEN** to 1b.

To set the polarity between AIO8 and MUX8 when in IO mode, use **CFGAIO8.POL8**.

7.10.3 AIO8 Gain Amplifier Mode

To configure AIO8 for gain amplifier mode, set **CFGAIO8.MODE8** to 01b.

In this mode, the gain of the amplifier can be set between 1X and 48X. To set the gain, set **CFGAIO8.GAIN8** to the desired value. To switch the output of the amplifier to analog channel AB1 to AB7 on the ABUS, set **CFGAIO8.MUX8** to the desired channel.

7.10.4 AIO8 Comparator Mode

To configure AIO8 for comparator mode, set **CFGAIO8.MODE8** to 10b.

In this mode, the comparator hysteresis may be enabled by setting **SMCFG.AIO8HYS** to 1b, and disabled by writing this field to 0b.

The compare value of this comparator can be set to AB1, AB2, AB3 or VTHREF. To select the compare value, set **CFGAIO8.OPT8**. The VTHREF may be set by using **SYSSTAT.VTHREF**.

The output polarity of the comparator may be set by setting **CFGAIO8.POL8** to the desired value.

The output of the comparator may be configured by setting the **CFGAIO8.MUX8**. The output can be set to DB1 to DB7 or to **AIOIN1.DIN8**.

7.10.5 AIO8 Special Mode

In special mode, the AIO8 comparator is enabled. To configure AIO8 for special mode, set **CFGAIO8.MODE8** to 11b.

To enable AIO8 comparator hysteresis, set **SMCFG.AIO8HYS** to 1b. To configure the compare value for the comparator to AB1, AB2 or AB3 use **CFGAIO7.OPT7**.

In special mode, AIO8 allows the user to configure the comparator start point.

Set **CFGAIO9.MODE9[0]** to 1b to connect AIO7, AIO8 and AIO9 to AB1 with a 100kOhm resistor to create a star point reference for the comparator.

Set **CFGAIO9.MODE9[0]** to 0b to set the AB1 reference to come from AIO6 in amplifier mode. To set AIO6 to amplifier mode, set **CFGAIO6.MODE6** to 01b and **CFGAIO6.GAIN6** to 000b for direct mode, and **CFGAIO6.MUX6** to 1b.

To read the voltage on AIO8, set **CFGAIO9.MODE9[1]** to 1b. This setting will MUX AIO8 to AB8 with 40% attenuation so the ADC can read the AIO8 voltage.

To read the comparator output for AIO7, AIO8 or AIO9 for position (POS), set **CFGAIO9.OPT9** to the desired value.

The AIO8 Sample and Hold (S/H) bypass may be configured as well. To bypass the POS S/H, set **CFGAIO8.OPT8[1]** to 0b. To use POS S/H for use with the EMUX, set **CFGAIO8.OPT8[0]** to the 1b.

To select the POS or nIRQ2 output, set the **CFGAIO8.OPT8[0]** to the desired value.

When configured in special mode, the user may select the comparator input using a MUX by writing the **CFGAIO8.MUX** field. The table below shows the comparator input selections that may be used.

Table 7-3 AIO7 Special Mode Comparator Input Selections

AIO8CFG.MODE	AIO Mode	AIO8CFG.MUX	Comparator Input MUX Select	Function
11b	Special Mode	000b	VTHREF	Fixed Threshold
		001b	AB1	Virtual Center-tap for BEMF Zero-Cross
		010b	AB2	
		011b	AB3	
		100b	AIO7	Phase to phase
		101b	AIO9	Phase to phase
		110b	RFU	
		111b	RFU	

The user may configure the comparator hysteresis separately for rising and falling hysteresis as shown in the table below.

Table 7-4 AIO8 Phase to Phase Comparator Hysteresis Configuration

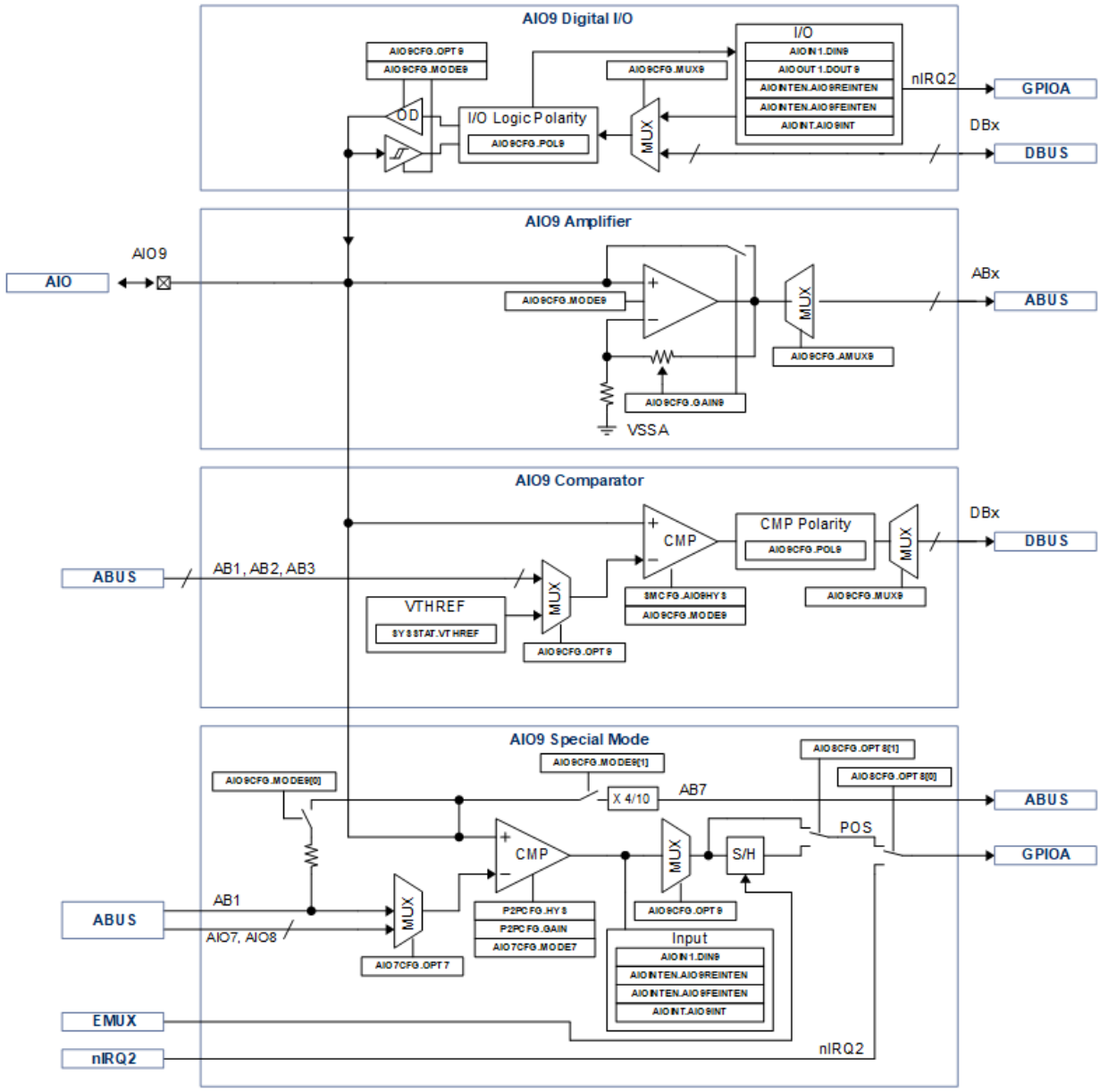
SPECFG1.HYSAIO8	SIGSET.HYSMODE	Rising Hysteresis	Falling Hysteresis
0000b	0b	0 mV	0 mV
0001b		0 mV	10 mV
0010b		0 mV	20 mV
0011b		0 mV	40 mV
0100b		10 mV	0 mV
0101b		10 mV	10 mV
0110b		10 mV	20 mV
0111b		10 mV	40 mV
1000b		20 mV	0 mV
1001b		20 mV	10 mV
1010b		20 mV	20 mV
1011b		20 mV	40 mV
1100b		40 mV	0 mV
1101b		40 mV	10 mV
1110b		40 mV	20 mV
1111b		40 mV	40 mV
0000b	1b	0 mV	0 mV
0001b		0 mV	35 mV
0010b		0 mV	70 mV
0011b		0 mV	140 mV
0100b		35 mV	0 mV
0101b		35 mV	35 mV
0110b		35 mV	70 mV
0111b		35 mV	140 mV
1000b		70 mV	0 mV
1001b		70 mV	35 mV
1010b		70 mV	70 mV
1011b		70 mV	140 mV
1100b		140 mV	0 mV
1101b		140 mV	35 mV
1110b		140 mV	70 mV
1111b		140 mV	140 mV

7.11 AIO9

AIO9 may be configured as a digital input, single-ended programmable gain amplifier, comparator or output from analog ABUS.

7.11.1 System Block Diagram

Figure 7-8 AIO9 System Block Diagram



7.11.2 AIO9 IO Mode

To configure AIO9 for as a digital input, set **CFGAIO9.MODE9** to 00b and set **CFGAIO9.OPT9** to 00b. The digital input state may be read from **AIOIN1.DIN9**.

To configure AIO9 as an open-drain output, set **CFGAIO9.MODE9** to 00b and set **CFGAIO9.OPT9** to 10b. Set **CFGAIO9.MUX9** to 00b to MUX the output state from **AIOOUT1.DOUT9**. Use **CFGAIO9.MUX9** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

To generate an interrupt on nIRQ2 on an AIO9 low to high transition, set **AIOINTEN.AIO9REINTEN** to 1b.

To generate an interrupt on nIRQ2 on an AIO9 high-to-low transition, set **AIOINTEN.AIO9FEINTEN** to 1b.

To set the polarity between AIO9 and MUX9 when in IO mode, use **CFGAIO9.POL9**.

7.11.3 AIO9 Gain Amplifier Mode

To configure AIO9 for gain amplifier mode, set **CFGAIO9.MODE9** to 01b.

In this mode, the gain of the amplifier can be set between 1X and 48X. To set the gain, set **CFGAIO9.GAIN9** to the desired value. To switch the output of the amplifier to analog channel AB1 to AB7 on the ABUS, set **CFGAIO9.MUX9** to the desired channel.

7.11.4 AIO9 Comparator Mode

To configure AIO9 for comparator mode, set **CFGAIO9.MODE9** to 10b.

In this mode, the comparator hysteresis may be enabled by setting **SMCFG.AIO9HYS** to 1b, and disabled by writing this field to 0b.

The compare value of this comparator can be set to AB1, AB2, AB3 or VTHREF. To select the compare value, set **CFGAIO9.OPT9**. The VTHREF may be set by using **SYSSTAT.VTHREF**.

The output polarity of the comparator may be set by setting **CFGAIO9.POL9** to the desired value.

The output of the comparator may be configured by setting the **CFGAIO9.MUX9**. The output can be set to DB1 to DB7 or to **AIOIN1.DIN9**.

7.11.5 AIO9Special Mode

In special mode, the AIO9 comparator is enabled. To configure AIO9 for special mode, set **CFGAIO9.MODE9** to 11b.

To enable AIO9 comparator hysteresis, set **SMCFG.AIO9HYS** to 1b. To configure the compare value for the comparator to AB1, AB2 or AB3 use **CFGAIO7.OPT7**.

In special mode, AIO9 allows the user to configure the comparator start point.

Set **CFGAIO9.MODE9[0]** to 1b to connect AIO7, AIO8 and AIO9 to AB1 with a 100kOhm resistor to create a star point reference for the comparator.

Set **CFGAIO9.MODE9[0]** to 0b to set the AB1 reference to come from AIO6 in amplifier mode. To set AIO6 to amplifier mode, set **CFGAIO6.MODE6** to 01b and **CFGAIO6.GAIN6** to 000b for direct mode, and **CFGAIO6.MUX6** to 1b.

To read the voltage on AIO9, set **CFGAIO9.MODE9[1]** to 1b. This setting will MUX AIO9 to AB9 with 40% attenuation so the ADC can read the AIO9 voltage.

To read the comparator output for AIO7, AIO8 or AIO9 for position (POS), set **CFGAIO9.OPT9** to the desired value.

The AIO9 Sample and Hold (S/H) bypass may be configured as well. To bypass the POS S/H, set **CFGAIO8.OPT8[1]** to 0b. To use POS S/H for use with the EMUX, set **CFGAIO8.OPT8[0]** to the 1b.

To select the POS or nIRQ2 output, set the **CFGAIO8.OPT8[0]** to the desired value.

When configured in special mode, the user may select the comparator input using a MUX by writing the AIO7CFG.MUX field. The table below shows the comparator input selections that may be used.

Table 7-5 AIO9 Special Mode Comparator Input Selections

CFGAIO9.MODE	AIO Mode	CFGAIO9.MUX	Comparator Input MUX Select	Function
11b	Special Mode	000b	VTHREF	Fixed Threshold
		001b	AB1	Virtual Center-tap for BEMF Zero-Cross
		010b	AB2	
		011b	AB3	
		100b	AIO7	Phase to phase
		101b	AIO9	Phase to phase
		110b	RFU	
		111b	RFU	

The user may configure the comparator hysteresis separately for rising and falling hysteresis as shown in the table below.

Table 7-6 AIO9 Phase to Phase Comparator Hysteresis Configuration

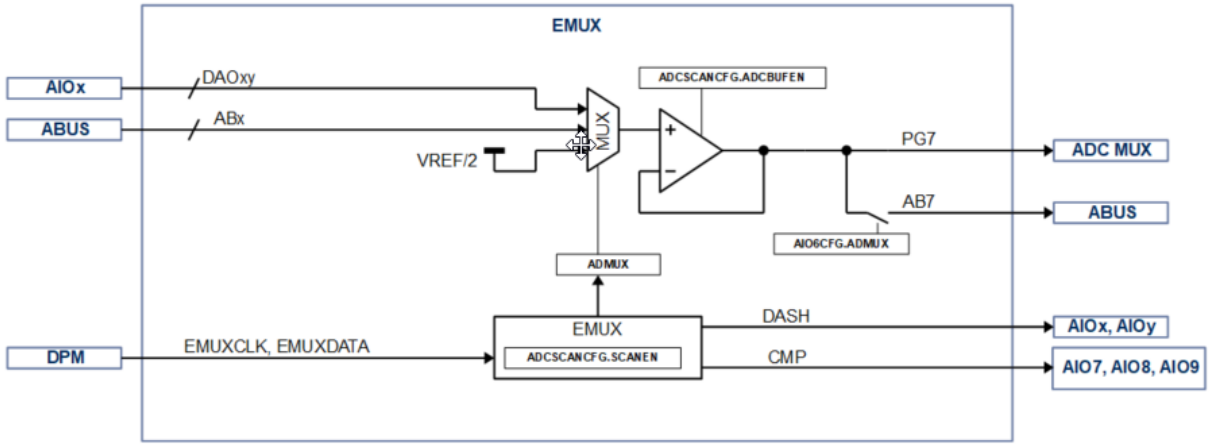
SPECFG1.HYSAIO9	SIGSET.HYSMODE	Rising Hysteresis	Falling Hysteresis
0000b	0b	0 mV	0 mV
0001b		0 mV	10 mV
0010b		0 mV	20 mV
0011b		0 mV	40 mV
0100b		10 mV	0 mV
0101b		10 mV	10 mV
0110b		10 mV	20 mV
0111b		10 mV	40 mV
1000b		20 mV	0 mV
1001b		20 mV	10 mV
1010b		20 mV	20 mV
1011b		20 mV	40 mV
1100b		40 mV	0 mV
1101b		40 mV	10 mV
1110b		40 mV	20 mV
1111b		40 mV	40 mV
0000b	1b	0 mV	0 mV
0001b		0 mV	35 mV
0010b		0 mV	70 mV
0011b		0 mV	140 mV
0100b		35 mV	0 mV
0101b		35 mV	35 mV
0110b		35 mV	70 mV
0111b		35 mV	140 mV
1000b		70 mV	0 mV
1001b		70 mV	35 mV
1010b		70 mV	70 mV
1011b		70 mV	140 mV
1100b		140 mV	0 mV
1101b		140 mV	35 mV
1110b		140 mV	70 mV
1111b		140 mV	140 mV

7.12 EMUX and ADMUX

The EMUX is a dedicated high-speed, low-latency serial interface to control the ADMUX, AIO7, AIO8, AIO9 POS S/H and the DAOxy S/H using the ADC DTSE sequencing engine.

7.12.1 System Block Diagram

Figure 7-9 EMUX and ADMUX System Block Diagram



7.12.2 EMUX

The EMUX is a dedicated high-speed low-latency serial interface to control the ADMUX, AIO7, AIO8, AIO9 POS S/H and the DAOxy S/H using the ADC DTSE.

To enable the EMUX, set **ADCSCANCFG.SCANEN** to 01b and enable the EMUX control of the ADMUX and the DAOxy S/H.

Table 7-7 EMUX Message Format

BIT	NAME	DESCRIPTION
7:6	**C**	Header, write to 01b
5	**CMP**	Comparator toggle: 1b: Hold POS value 0b: Sample POS value
4	**DASH**	DAxy S/H toggle: 1b: Hold DAOxy value 0b: Sample DAOxy
3:0	**MUX**	ADMUX Channel Selector: 1111b: VREF / 2 1110b: AB12 1101b: AB11 1100b: AB10 1011b: AB9 1010b: AB8 1001b: AB7 1000b: AB6 0111b: AB5

		0110b: AB4 0101b: AB3 0100b: AB2 0011b: AB1 0010b: DAO54 0001b: DAO32 0000b: DAO10

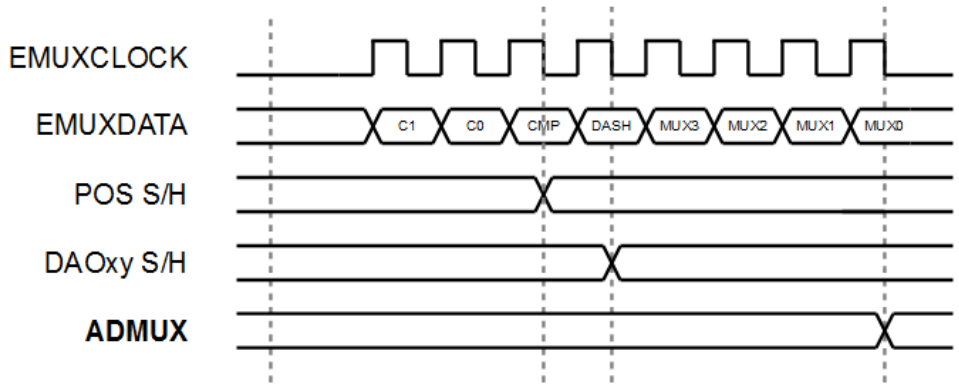
The EMUX serial message is transmitted MSB first. The header (C1, C2) is fixed and needs to be written to 01b.

The POS S/H is toggled based on the **CMP** bit in the EMUXD packet with the falling edge of the 3rd clock cycle.

The DAOxy S/H is toggled based on the **DASH** bit in the EMUXD packet with the falling edge of the 4th clock cycle.

The ADMUX is switched with the falling edge of the 8th clock based on the data of bits 3:1 of the EMUXD packet.

Figure 7-10 EMUX Timing Diagram



7.12.3 ADMUX

The ADMUX is a dedicated analog MUX in the CAFE.

To set the channel on the ADMUX, use the **ADMUX** register. When the EMUX is enabled, the ADMUX can be controlled directly from the ADC DTSE on the MCU using EMUXD.

To enable the ADMUX buffer, set **ADCSCANCFG.ADCBUFEN** to 1b.

To route the output of the ADMUX to AB7, set **AIO6CFG.ADMUX** to 1b.

7.13 Register Summary

Table 7-8 CAFE Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
20h	**CFGAIO0**	AIO0 Configuration	00h
21h	**CFGAIO1**	AIO1 Configuration	00h
22h	**CFGAIO2**	AIO2 Configuration	00h
23h	**CFGAIO3**	AIO3 Configuration	00h
24h	**CFGAIO4**	AIO4 Configuration	00h
25h	**CFGAIO5**	AIO5 Configuration	00h
26h	**CFGAIO6**	AIO6 Configuration	00h
27h	**CFGAIO7**	AIO7 Configuration	00h
28h	**CFGAIO8**	AIO8 Configuration	00h
29h	**CFGAIO9**	AIO9 Configuration	00h
2Ah	**SMCFG**	Signal manager Configuration	00h
2Bh	**HPDAC**	High Protection Threshold	00h
2Ch	**LPDAC0**	Low Protection Threshold	00h
2Dh	**LPDAC1**	Low Protection Threshold	00h
2Eh	**ADCSCANCFG**	ADC Scan Control	00h
2Fh	**ADMUX**	ADC MUX Select	00h
30h	**PROTINTEN**	Protection Interrupt Enable	00h
31h	**PROTINT**	Protection Status	00h
32h	**AIOOUT0**	AIO[5:0] digital output control	00h
33h	**AIOOUT1**	AIO[9:6] digital output control	00h
34h	**AIOIN0**	AIO[5:0] digital input control	00h
35h	**AIOIN1**	AIO[9:6] digital input control	00h
36h	**AIOINTEN**	AIO[9:6] interrupt enable	00h
37h	**AIOINT**	AIO[9:6] interrupt flag	00h
38h	**ENSIG**	Signal Manager Control	00h
39h	**SPECCFG1**	AIO[9:8] Hysteresis Configuration	00h
3Ah	**SPECCFG2**	AIO7 Hysteresis and Blanking Time Configuration	00h

7.14 Register Detail

7.14.1 CFGAIO0

Register 7-1 CFGAIO0 (AIO0 Configuration, 20h)

<table>
<tr><th>BIT</th><th>NAME</th><th>ACCESS</th><th>RESET</th><th>IO MODE</th><th>DIFFAMP MODE</th></tr>
<tr><td>7:6</td><td>MODE0</td><td>RW</td><td>00b</td><td>00b</td><td>01b</td></tr>
<tr><td>5</td><td rowspan="2">OPT0</td><td>RW</td><td>0b</td><td rowspan="2">AIO0 Option:

00b: Input, input state available at AIOIN0.AIO0DIN
01b: High-impedance
10b: Open-drain output
11b: High-impedance</td><td rowspan="3">GAIN10

Differential amplifier gain setting:

000b: 1x
001b: 1x
010b: 2x
011b: 4x
100b: 8x
101b: 16x
110b: 32x
111b: 48x</td></tr>
<tr><td>4</td><td>RW</td><td>0b</td></tr>
<tr><td>3</td><td>POL0</td><td>RW</td><td>0b</td><td>If CFGAIO0.OPT0 = 00b, AIO0 input polarity setting. If CFGAIO0.OPT0 = 10b, AIO0 output polarity setting:

0b: active high
1b: active low</td></tr>
<tr><td rowspan="3">2:0</td><td rowspan="3">MUX0</td><td>RW</td><td>0b</td><td rowspan="3">AIO0 Digital MUX setting:

000b: AIO0
001b: DB1
010b: DB2
011b: DB3
100b: DB4
101b: DB5
110b: DB6
111b: DB7</td><td>Reserved</td></tr>
<tr><td>RW</td><td>0b</td><td rowspan="2">LPOPT10

LP10 Comparator option:

00b: LP10 comparator disabled
01b: LP10 comparator enabled with 1µs blanking time
10b: LP10 comparator enabled with 2µs blanking time
11b: LP10 comparator enabled with 4µs blanking time</td></tr>
<tr><td>RW</td><td>0b</td></tr>
</table>

7.14.2 CFGAIO1

Register 7-2 CFGAIO1 (AIO1 Configuration, 21h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7	**MODE1**	RW	0b	Reserved	Reserved
6		RW	0b	Reserved	Reserved
5	**OPT1**	RW	0b	AIO1 IO Option: 00b: Input, input state available at **AIOIN0.AIO1DIN** 01b: Reserved 10b: Open-drain output 11b: Reserved	**HP10PREN** HPROT10 PR Protection enable: 0b: HP10 output to PR disabled 1b: HP10 output to PR enabled
4		RW	0b		**LP10PREN** LPROT10 PR Protection enable: 0b: LP10 output to PR disabled 1b: LP10 output to PR enabled
3	**POL1**	RW	0b	If **CFGAIO1.OPT1** = 00b, AIO1 input polarity setting. If **CFGAIO1.OPT1** = 10b, AIO1 output polarity setting: 0b: active high 1b: active low	**OS10EN** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by VREF/2
2:0	**MUX1**	RW	0b	If **CFGAIO1.OPT1** = 00b, Reserved If **CFGAIO1.OPT1** = 10b, Output polarity, set AIO1 state according to MUX1: 000b: AIO1 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL10EN** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
		RW	0b		**HP10OPT** HP10 Comparator setting: 00b: HP10 comparator disabled 01b: HP10 comparator enabled with 1µs blanking time 10b: HP10 comparator enabled with 2µs blanking time 11b: HP10 comparator enabled with 4µs blanking time
		RW	0b		

7.14.3 CFGAIO2

Register 7-3 CFGAIO2 (AIO2 Configuration, 22h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE2**	RW	00b	00b	01b
5	**OPT2**	RW	0b	AIO2 Option: 00b: Input, input state available at **AIOIN0.AI2DIN** 01b: High-impedance 10b: Open-drain output 11b: High-impedance	**GAIN32** Differential amplifier gain setting: 000b: 1x 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x
4		RW	0b		
3	**POL2**	RW	0b	If **CFGAIO2.OPT2** = 00b, AIO2 input polarity setting. If **CFGAIO2.OPT2** = 10b, AIO2 output polarity setting: 0b: active high 1b: active low	
2:0	**MUX2**	RW	0b	AIO0 Digital MUX setting: 000b: AIO2 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved
		RW	0b		**LP32OPT** LP32 Comparator option: 00b: LP32 comparator disabled 01b: LP32 comparator enabled with 1µs blanking time 10b: LP32 comparator enabled with 2µs blanking time 11b: LP32 comparator enabled with 4µs blanking time
		RW	0b		

7.14.4 CFGAIO3

Register 7-4 CFGAIO3 (AIO3 Configuration, 23h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7	**MODE3**	RW	0b	Reserved	Reserved
6		RW	0b	Reserved	Reserved
5	**OPT3**	RW	0b	AIO3 IO Option: 00b: Input, input state available at **AIOIN0.AIO3DIN** 01b: High-impedance 10b: Open-drain output 11b: High-impedance	**HP32PREN** HPROT32 PR Protection enable: 0b: HP32 output to PR disabled 1b: HP32 output to PR enabled
4		RW	0b		**LP32PREN** LPROT32 PR Protection enable: 0b: LP32 output to PR disabled 1b: LP32 output to PR enabled
3	**POL3**	RW	0b	If **CFGAIO3.OPT3** = 00b, AIO3 input polarity setting. If **CFGAIO3.OPT3** = 10b, AIO3 output polarity setting: 0b: active high 1b: active low	**OS32EN** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by VREF/2
2:0	**MUX3**	RW	0b	If **CFGAIO3.OPT3** = 00b, Reserved If **CFGAIO3.OPT3** = 10b, Output polarity, set AIO3 state according to MUX3: 000b: AIO3 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL32EN** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
		RW	0b		**HP32OPT** HP32 Comparator setting: 00b: HP32 comparator disabled 01b: HP32 comparator enabled with 1µs blanking time 10b: HP32 comparator enabled with 2µs blanking time 11b: HP32 comparator enabled with 4µs blanking time
		RW	0b		

7.14.5 CFGAIO4

Register 7-5 CFGAIO4 (AIO4 Configuration, 24h)

<table>
<tr><th>BIT</th><th>NAME</th><th>ACCESS</th><th>RESET</th><th>IO MODE</th><th>DIFFAMP MODE</th></tr>
<tr><td>7:6</td><td>MODE4</td><td>RW</td><td>00b</td><td>00b</td><td>01b</td></tr>
<tr><td>5</td><td rowspan="2">OPT4</td><td>RW</td><td>0b</td><td rowspan="2">AIO4 IO Option:

00b: Input, input state available at AIOIN0.AI4DIN
01b: High-impedance
10b: Open-drain output
11b: High-impedance</td><td rowspan="2">GAIN54

Differential amplifier gain setting:

000b: 1x
001b: 1x
010b: 2x
011b: 4x
100b: 8x
101b: 16x
110b: 32x
111b: 48x</td></tr>
<tr><td>4</td><td>RW</td><td>0b</td></tr>
<tr><td>3</td><td>POL4</td><td>RW</td><td>0b</td><td>If CFGAIO4.OPT4 = 00b, AIO4 input polarity setting. If CFGAIO4.OPT4 = 10b, AIO4 output polarity setting:

0b: active high
1b: active low</td></tr>
<tr><td rowspan="3">2:0</td><td rowspan="3">MUX4</td><td>RW</td><td>0b</td><td rowspan="3">If CFGAIO4.OPT4 = 00b, Reserved

If CFGAIO4.OPT4 = 10b, Output polarity, set to AIO4 state according to MUX4:

000b: AIO4
001b: DB1
010b: DB2
011b: DB3
100b: DB4
101b: DB5
110b: DB6
111b: DB7</td><td>Reserved</td></tr>
<tr><td>RW</td><td>0b</td><td rowspan="2">LP54OPT

LP54 Comparator option:

00b: LP54 comparator disabled
01b: LP54 comparator enabled with 1µs blanking time
10b: LP54 comparator enabled with 2µs blanking time
11b: LP54 comparator enabled with 4µs blanking time</td></tr>
<tr><td>RW</td><td>0b</td></tr>
</table>

7.14.6 CFGAIO5

Register 7-6 CFGAIO5 (AIO5 Configuration, 25h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7	**MODE5**	RW	0b	Reserved	Reserved
6		RW	0b	Reserved	Reserved
5	**OPT5**	RW	0b	AIO5 IO Mode: 00b: Input, input state available at **AIOIN0.AIO5DIN** 01b: Reserved 10b: Open-drain output 11b: Reserved	**HP54PREN** HPROT54 PR Protection enable: 0b: HP54 output to PR disabled 1b: HP54 output to PR enabled
4		RW	0b		**LP54PREN** LPROT54 PR Protection enable: 0b: LP54 output to PR disabled 1b: LP54 output to PR enabled
3	**POL5**	RW	0b	If **CFGAIO5.OPT5** = 00b, AIO5 input polarity setting. If **CFGAIO5.OPT5** = 10b, AIO5 output polarity setting: 0b: active high 1b: active low	**OS54EN** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by VREF/2
2:0	**MUX5**	RW	0b	If **CFGAIO5.OPT5** = 00b, Reserved If **CFGAIO5.OPT5** = 10b, Output polarity, set AIO5 state according to MUX5: 000b: AIO5 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL54EN** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
		RW	0b		**HP54OPT** HP54 Comparator option: 00b: HP54 comparator disabled 01b: HP54 comparator enabled with 1µs blanking time 10b: HP54 comparator enabled with 2µs blanking time 11b: HP54 comparator enabled with 4µs blanking time
		RW	0b		

7.14.7 CFGAIO6

Register 7-7 CFGAIO6 (AIO6 Configuration, 26h)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE6** 00b	**MODE6** 01b	**MODE6** 10b	**MODE6** 11b
5	**OPT6** AIO6 IO Setting: 00b: Input, input state available at **AIOIN1.AIO6DIN** 01b: Reserved 10b: Open-drain output 11b: Reserved	**GAIN6** Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT6** AIO6 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**ADMUX** ADMUX ADC output MUX: 0b: Do not MUX ADMUX output to AB7 1b: MUX ADMUX output to AB7
4				**SWAP** Buffer Swap: 0b: Do not swap buffer offset 1b: Swap buffer offset
3	**POL6** If **CFGAIO6.OPT6** = 00b, AIO6 Input Polarity Setting. If **CFGAIO6.OPT6** = 10b, AIO6 Output Polarity Setting. 00b: active-high 01b: active-low		**POL6** AIO6 Comparator output polarity setting: 0b: active-high 1b: active-low	Reserved, write to 0b
2:0	**MUX6** If **CFGAIO6.OPT6** = 00b, Reserved. If **CFGAIO6.OPT6** = 10b, Output Polarity, set AIO6 state according to MUX6: 000b: DOUT6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX6** Analog MUX Setting: 000b: AB6 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX6** Send AIO6 comparator output state to internal digital bus and **AIOIN1.AIO6DIN**: 000b: DB6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX6** Analog MUX Setting: 000b: AB6 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7

7.14.8 CFGAIO7

Register 7-8 CFGAIO7 (AIO7 Configuration, 27h)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE7** 00b	**MODE7** 01b	**MODE7** 10b	**MODE7** 11b
5	**OPT7** AIO7 IO Setting: 00b: Input, input state available at **AIOIN1.AIO7DIN** 01b: Reserved 10b: Open-drain output 11b: Reserved	**GAIN7** Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT7** AIO7 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write as 0
4				Reserved, write as 0
3	**POL7** If **CFGAIO7.OPT7** = 00b, AIO6 Input Polarity Setting. If **CFGAIO7.OPT7** = 10b, AIO7 Output Polarity Setting. 00b: active-high 01b: active-low		**POL7** AIO7 Comparator output polarity setting: 0b: active-high 1b: active-low	**POL7** AIO7 Comparator output polarity setting: 0b: active-high 1b: active-low
2:0	**MUX7** If **CFGAIO7.OPT7** = 00b, Reserved. If **CFGAIO7.OPT7** = 10b, Output Polarity, set AIO7 state according to MUX7: 000b: DOUT7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX7** Analog MUX Setting: 000b: AB7 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX7** Send AIO7 comparator output state to internal digital bus and **AIOIN1.AIO7DIN**: 000b: DB7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX7** Special Mode Comparator Input MUX Selection: 000b: VTHREF 001b: AB1 (Virtual center-tap) 010b: AB2 011b: AB3 100b: AIO8 (Phase to phase) 101b: AIO9 (Phase to phase) 110b: RFU 111b: RFU

7.14.9 CFGAIO8

Register 7-9 CFGAIO8 (AIO8 Configuration, 28h)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE8** 00b	**MODE8** 01b	**MODE8** 10b	**MODE8** 11b
5	**OPT8** AIO8 IO Setting: 00b: Input, input state available at **AIOIN1.AIO8DIN** 01b: Reserved 10b: Open-drain output 11b: Reserved	**GAIN8** Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT8** AIO8 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**OPT8[1]** Comparator S/H output: 0b: raw comparator output 1b: S/H of raw comparator output
4				**OPT8[0]** Comparator output MUX: 0b: nIRQ2 (AIO6/7/8/9 interrupt) 1b: POS (BEMF detection)
3	**POL8** If **CFGAIO8.OPT8** = 00b, AIO8 Input Polarity Setting. If **CFGAIO8.OPT8** = 10b, AIO8 Output Polarity Setting. 00b: active-high 01b: active-low		**POL8** AIO8 Comparator output polarity setting: 0b: active-high 1b: active-low	**POL8** AIO8 Comparator output polarity setting: 0b: active-high 1b: active-low
2:0	**MUX8** Digital MUX: 000b: DOUT 8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX8** Analog MUX Setting: 000b: AB8 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX8** Digital MUX: 000b: AIO8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX8** Special Mode Comparator Input MUX Selection: 000b: VTHREF 001b: AB1 (Virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (Phase to phase) 101b: AIO9 (Phase to phase) 110b: RFU 111b: RFU

7.14.10 CFGAIO9

Register 7-10 CFGAIO9 (AIO9 Configuration, 29h)

BIT	IO MODE	GAIN MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE9** 00b	**MODE9** 01b	**MODE9** 10b	**MODE9** 11b
5 4	**OPT9** AIO9 IO Setting: 00b: Input, input state available at **AIOIN1.AIO9DIN** 01b: Reserved 10b: Open-drain output 11b: Reserved	**GAIN9** Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT9** AIO9 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**OPT9** AIO789 comparator output to POS: 00b: not connected 01b: MUX AIO7 comparator output to POS 10b: MUX AIO8 comparator output to POS 11b: MUX AIO9 comparator output to POS
3	**POL9** If **CFGAIO9.OPT9** = 00b, AIO9 Input Polarity Setting. If **CFGAIO9.OPT9** = 10b, AIO9 Output Polarity Setting. 00b: active-high 01b: active-low		**POL9** AIO9 Comparator output polarity setting: 0b: active-high 1b: active-low	**POL9** AIO9 Comparator output polarity setting: 0b: active-high 1b: active-low
2:0	**MUX9** Digital MUX: 000b: DOUT 9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX9** Analog MUX Setting: 000b: AB9 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX9** Digital MUX: 000b: AIO9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX9** Special Mode Comparator Input MUX Selection: 000b: VTHREF 001b: AB1 (Virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (Phase to phase) 101b: AIO8 (Phase to phase) 110b: RFU 111b: RFU

7.14.11 SMCFG

Register 7-11 SMCFG (Signal Manager Configuration, 2Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HYSMODE**	RW	0b	Hysteresis mode
6:5	**BLANKMODE**	RW	0b	BEMF Comparator Blanking Mode: 00b: Disabled 01b: Leading Edge Blanking 10b: Trailing Edge Blanking 11b: Lead and Trailing Edge Blanking
4	**AIO6HYS**	RW	0b	AIO6 Comparator Hysteresis. 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
3	**HPROTHYS**	RW	0b	HPx Hysteresis. 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
2	**LPROTHYS**	RW	0b	LPx Hysteresis. 1b: Comparator Hysteresis enabled 0b: Comparator Hysteresis disabled
1	**LPDACAB3**	RW	0b	Connect LPDAC output to AB3. 1b: LPDAC output connected to AB3 0b: LPDAC output not connected to AB3
0	**HPDACAB2**	RW	0b	Connect HPDAC output to AB2. 1b: HPDAC output connected to AB2 0b: HPDAC output not connected to AB2

7.14.12 HPDAC

Register 7-12 HPDAC (HPDAC Setting, 2Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**HPDAC**	RW	0	HPDAC Setting: FFh: 255/256 * VREF .. 00h 0/256 * VREF

7.14.13 LPDAC0

Register 7-13 LPDAC0 (LPDAC0 Setting, 2Ch)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**LPDAC[9:2]**	RW	0b	LPDAC Setting bit 9 to bit 2.

7.14.14 LPDAC1

Register 7-14 LPDAC1 (LPDAC1 Setting, 2Dh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**Reserved**	RW	0b	Reserved, write to 0.
1:0	**LPDAC[1:0]**	RW	0b	LPDAC Setting bit 1 to bit 0.

7.14.15 ADCSCANCFG

Register 7-15 ADCSCANCFG (ADCSCAN Configuration, 2Eh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**Reserved**	RW	0b	Reserved, write to 0x0
4	**SCANEN**	RW	0b	ADC Scan Control Enable. 1b: enabled 0b: disabled
3	**ADCBUFEN**	RW	0b	ADC Buffer Enable. 1b: enabled 0b: disabled
2	**DAO10SH**	RW	0b	DAO10 Sample and Hold buffer enable. 1b: enable S/H 0b: disable and bypass S/H
1	**DAO32SH**	RW	0b	DAO32 Sample and Hold buffer enable. 1b: enable S/H 0b: disable and bypass S/H
0	**DAO54SH**	RW	0b	DAO54 Sample and Hold buffer enable. 1b: enable S/H 0b: disable and bypass S/H

7.14.16 ADCMUX

Register 7-16 ADCMUX (ADC MUX Selection, 2Fh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**Reserved**	RW	0b	Reserved, write to 0.
3:0	**MUXA**	RW	0b	ADC Mux Channel Selector **when** **ADCSCANCFG.SCANEN** = 0 (or when **ADCSCANCFG.SCANEN** = 1 and SH1 = 1): 1111b: VREF / 2 1110b: AB12 1101b: AB11 1100b: AB10 1011b: AB9 1010b: AB8 1001b: AB7 1000b: AB6 0111b: AB5 0110b: AB4 0101b: AB3 0100b: AB2 0011b: AB1 0010b: DAO54 0001b: DAO32 0000b: DAO10

7.14.17 PROTINTEN

Register 7-17 PROTINTEN (Protection Interrupt Enable, 30h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**Reserved**	RW	0b	Reserved, write to 0.
6	**HP54INTEN**	RW	0b	HPROT54 Interrupt enable. 1b: enable 0b: disabled
5	**HP32INTEN**	RW	0b	HPROT32 Interrupt enable. 1b: enable 0b: disabled
4	**HP10INTEN**	RW	0b	HPROT10 Interrupt enable. 1b: enable 0b: disabled
3	**Reserved**	RW	0b	Reserved, write to 0.
2	**LP54INTEN**	RW	0b	LPROT54 Interrupt enable. 1b: enable 0b: disabled
1	**LP32INTEN**	RW	0b	LPROT32 Interrupt enable. 1b: enable 0b: disabled
0	**LP10INTEN**	RW	0b	LPROT10 Interrupt enable. 1b: enable 0b: disabled

7.14.18 PROTINT

Register 7-18 PROTINT (Protection Interrupt Flag, 31h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**Reserved**	RW	0b	Reserved, write to 0.
6	**HP54INT**	RW	0b	HPROT54 Interrupt. 1b: Interrupt, write 1 to clear 0b: No interrupt
5	**HP32INT**	RW	0b	HPROT32 Interrupt. 1b: Interrupt, write 1 to clear 0b: No interrupt
4	**HP10INT**	RW	0b	HPROT10 Interrupt. 1b: Interrupt, write 1 to clear 0b: No interrupt
3	**Reserved**	RW	0b	Reserved, write to 0.
2	**LP54INT**	RW	0b	LPROT54 Interrupt. 1b: Interrupt, write 1 to clear 0b: No interrupt
1	**LP32INT**	RW	0b	LPROT32 Interrupt. 1b: Interrupt, write 1 to clear 0b: No interrupt
0	**LP10INT**	RW	0b	LPROT10 Interrupt. 1b: Interrupt, write 1 to clear 0b: No interrupt

7.14.19 AIOOUT0

Register 7-19 AIOOUT0 (AIO[5:0] Digital Output Control, 32h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**Reserved**	RW	0b	Reserved, write to 0.
5	**DOUT5**	RW	0b	Data output from AIO5.
4	**DOUT4**	RW	0b	Data output from AIO4.
3	**DOUT3**	RW	0b	Data output from AIO3.
2	**DOUT2**	RW	0b	Data output from AIO2.
1	**DOUT1**	RW	0b	Data output from AIO1.
0	**DOUT0**	RW	0b	Data output from AIO0.

7.14.20 AIOOUT1

Register 7-20 AIOOUT1 (AIO[9:6] Digital Output Control, 33h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**Reserved**	RW	0b	Reserved, write to 0.
3	**DOUT9**	RW	0b	Data output from AIO9.
2	**DOUT8**	RW	0b	Data output from AIO8.
1	**DOUT7**	RW	0b	Data output from AIO7.
0	**DOUT6**	RW	0b	Data output from AIO6.

7.14.21 AIOIN0

Register 7-21 AIOIN0 (AIO[5:0] Digital Input Control, 34h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**Reserved**	RW	0b	Reserved, write to 0.
5	**DIN5**	R	0b	Data input from AIO5.
4	**DIN4**	R	0b	Data input from AIO4.
3	**DIN3**	R	0b	Data input from AIO3.
2	**DIN2**	R	0b	Data input from AIO2.
1	**DIN1**	R	0b	Data input from AIO1.
0	**DIN0**	R	0b	Data input from AIO0.

7.14.22 AIOIN1

Register 7-22 AIOIN1 (AIO[9:6] Digital Input Control, 35h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**Reserved**	RW	0b	Reserved, write to 0.
3	**DIN9**	R	0b	Data input from AIO9.
2	**DIN8**	R	0b	Data input from AIO8.
1	**DIN7**	R	0b	Data input from AIO7.
0	**DIN6**	R	0b	Data input from AIO6.

7.14.23 AIOINTEN

Register 7-23 AIOINTEN (AIO[9:6] Interrupt Enable, 36h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**AIO9REINTEN**	RW	0b	AIO9 digital input rising edge interrupt enable. 1b: enabled 0b: disabled
6	**AIO8REINTEN**	RW	0b	AIO8 digital input rising edge interrupt enable. 1b: enabled 0b: disabled
5	**AIO7REINTEN**	RW	0b	AIO7 digital input rising edge interrupt enable. 1b: enabled 0b: disabled
4	**AIO6REINTEN**	RW	0b	AIO6 digital input rising edge interrupt enable. 1b: enabled 0b: disabled
3	**AIO9FEINTEN**	RW	0b	AIO9 digital input falling edge interrupt enable. 1b: enabled 0b: disabled
2	**AIO8FEINTEN**	RW	0b	AIO8 digital input falling edge interrupt enable. 1b: enabled 0b: disabled
1	**AIO7FEINTEN**	RW	0b	AIO7 digital input falling edge interrupt enable. 1b: enabled 0b: disabled
0	**AIO6FEINTEN**	RW	0b	AIO6 digital input falling edge interrupt enable. 1b: enabled 0b: disabled

7.14.24 AIOINT

Register 7-24 AIOINT (AIO[9:6] Interrupt Flag, 37h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**Reserved**	RW	0b	Reserved, write to 0.
3	**AIO9INT**	RW	0b	AIO9 Interrupt. 1b: Interrupt, clear by writing 1b 0b: No Interrupt
2	**AIO8INT**	RW	0b	AIO8 Interrupt. 1b: Interrupt, clear by writing 1b 0b: No Interrupt
1	**AIO7INT**	RW	0b	AIO7 Interrupt. 1b: Interrupt, clear by writing 1b 0b: No Interrupt
0	**AIO6INT**	RW	0b	AIO6 Interrupt. 1b: Interrupt, clear by writing 1b 0b: No Interrupt

7.14.25 SMCTL

Register 7-25 SMCTL (Signal Manager Control, 38h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	**Reserved**	RW	0b	Reserved, write to 0.
0	**SMEN**	RW	0b	Signal Manager Enable. 1b: Enabled 0b: Disabled

7.14.26 SPECCFG1

Register 7-26 SPECCFG1 (AIO[9:8] Hysteresis Configuration, 39h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**HYSAIO8**	RW	0000b	AIO8 Special Mode Comparator Rising/Falling Hysteresis. If **SMCFG.HYSMODE** = 0b: 0000b: rising = 0 mV, falling = 0 mV 0001b: rising = 0 mV, falling = 10 mV 0010b: rising = 0 mV, falling = 20 mV 0011b: rising = 0 mV, falling = 40 mV 0100b: rising = 10 mV, falling = 0 mV 0101b: rising = 10 mV, falling = 10 mV 0110b: rising = 10 mV, falling = 20 mV 0111b: rising = 10 mV, falling = 40 mV 1000b: rising = 20 mV, falling = 0 mV 1001b: rising = 20 mV, falling = 10 mV 1010b: rising = 20 mV, falling = 20 mV 1011b: rising = 20 mV, falling = 40 mV 1100b: rising = 40 mV, falling = 0 mV 1101b: rising = 40 mV, falling = 10 mV 1110b: rising = 40 mV, falling = 20 mV 1111b: rising = 40 mV, falling = 40 mV If **SMCFG.HYSMODE** = 1b: 0000b: rising = 0 mV, falling = 0 mV 0001b: rising = 0 mV, falling = 35 mV 0010b: rising = 0 mV, falling = 70 mV 0011b: rising = 0 mV, falling = 140 mV 0100b: rising = 35 mV, falling = 0 mV 0101b: rising = 35 mV, falling = 35 mV 0110b: rising = 35 mV, falling = 70 mV 0111b: rising = 35 mV, falling = 140 mV 1000b: rising = 70 mV, falling = 0 mV 1001b: rising = 70 mV, falling = 35 mV 1010b: rising = 70 mV, falling = 70 mV 1011b: rising = 70 mV, falling = 140 mV 1100b: rising = 140 mV, falling = 0 mV 1101b: rising = 140 mV, falling = 35 mV 1110b: rising = 140 mV, falling = 70 mV 1111b: rising = 140 mV, falling = 140 mV
3:0	**HYSAIO9**	RW	0000b	AIO9 Special Mode Comparator Rising/Falling Hysteresis. If **SMCFG.HYSMODE** = 0b: 0000b: rising = 0 mV, falling = 0 mV 0001b: rising = 0 mV, falling = 10 mV 0010b: rising = 0 mV, falling = 20 mV 0011b: rising = 0 mV, falling = 40 mV 0100b: rising = 10 mV, falling = 0 mV 0101b: rising = 10 mV, falling = 10 mV 0110b: rising = 10 mV, falling = 20 mV 0111b: rising = 10 mV, falling = 40 mV 1000b: rising = 20 mV, falling = 0 mV 1001b: rising = 20 mV, falling = 10 mV 1010b: rising = 20 mV, falling = 20 mV 1011b: rising = 20 mV, falling = 40 mV 1100b: rising = 40 mV, falling = 0 mV 1101b: rising = 40 mV, falling = 10 mV

				1110b: rising = 40 mV, falling = 20 mV 1111b: rising = 40 mV, falling = 40 mV If **SMCFG.HYSMODE** = 1b: 0000b: rising = 0 mV, falling = 0 mV 0001b: rising = 0 mV, falling = 35 mV 0010b: rising = 0 mV, falling = 70 mV 0011b: rising = 0 mV, falling = 140 mV 0100b: rising = 35 mV, falling = 0 mV 0101b: rising = 35 mV, falling = 35 mV 0110b: rising = 35 mV, falling = 70 mV 0111b: rising = 35 mV, falling = 140 mV 1000b: rising = 70 mV, falling = 0 mV 1001b: rising = 70 mV, falling = 35 mV 1010b: rising = 70 mV, falling = 70 mV 1011b: rising = 70 mV, falling = 140 mV 1100b: rising = 140 mV, falling = 0 mV 1101b: rising = 140 mV, falling = 35 mV 1110b: rising = 140 mV, falling = 70 mV 1111b: rising = 140 mV, falling = 140 mV

7.14.27 SPECCFG2

Register 7-27 SPECCFG2 (AIO7 Hysteresis and Blanking Time Configuration, 3Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**HYSAIO8**	RW	0000b	AIO7 Special Mode Comparator Rising/Falling Hysteresis. If **SMCFG.HYSMODE** = 0b: 0000b: rising = 0 mV, falling = 0 mV 0001b: rising = 0 mV, falling = 10 mV 0010b: rising = 0 mV, falling = 20 mV 0011b: rising = 0 mV, falling = 40 mV 0100b: rising = 10 mV, falling = 0 mV 0101b: rising = 10 mV, falling = 10 mV 0110b: rising = 10 mV, falling = 20 mV 0111b: rising = 10 mV, falling = 40 mV 1000b: rising = 20 mV, falling = 0 mV 1001b: rising = 20 mV, falling = 10 mV 1010b: rising = 20 mV, falling = 20 mV 1011b: rising = 20 mV, falling = 40 mV 1100b: rising = 40 mV, falling = 0 mV 1101b: rising = 40 mV, falling = 10 mV 1110b: rising = 40 mV, falling = 20 mV 1111b: rising = 40 mV, falling = 40 mV If **SMCFG.HYSMODE** = 1b: 0000b: rising = 0 mV, falling = 0 mV 0001b: rising = 0 mV, falling = 35 mV 0010b: rising = 0 mV, falling = 70 mV 0011b: rising = 0 mV, falling = 140 mV 0100b: rising = 35 mV, falling = 0 mV 0101b: rising = 35 mV, falling = 35 mV 0110b: rising = 35 mV, falling = 70 mV 0111b: rising = 35 mV, falling = 140 mV 1000b: rising = 70 mV, falling = 0 mV 1001b: rising = 70 mV, falling = 35 mV 1010b: rising = 70 mV, falling = 70 mV 1011b: rising = 70 mV, falling = 140 mV 1100b: rising = 140 mV, falling = 0 mV 1101b: rising = 140 mV, falling = 35 mV 1110b: rising = 140 mV, falling = 70 mV 1111b: rising = 140 mV, falling = 140 mV
3:0	**BLANKTIME**	RW	0000b	Blanking time for special mode comparators (AIO[9:7]): 0000b: 66ns 0001b: 116ns 0010b: 215ns 0011b: 265ns 0100b: 314ns 0101b: 364ns 0110b: 415ns 0111b: 516ns 1000b: 566ns 1001b: 617ns 1010b: 769ns 1011b: 871ns 1100b: 973ns 1101b: 1229ns 1110b: 1847ns 1111b: 2468ns

8 APPLICATION SPECIFIC POWER DRIVER

8.1 Overview

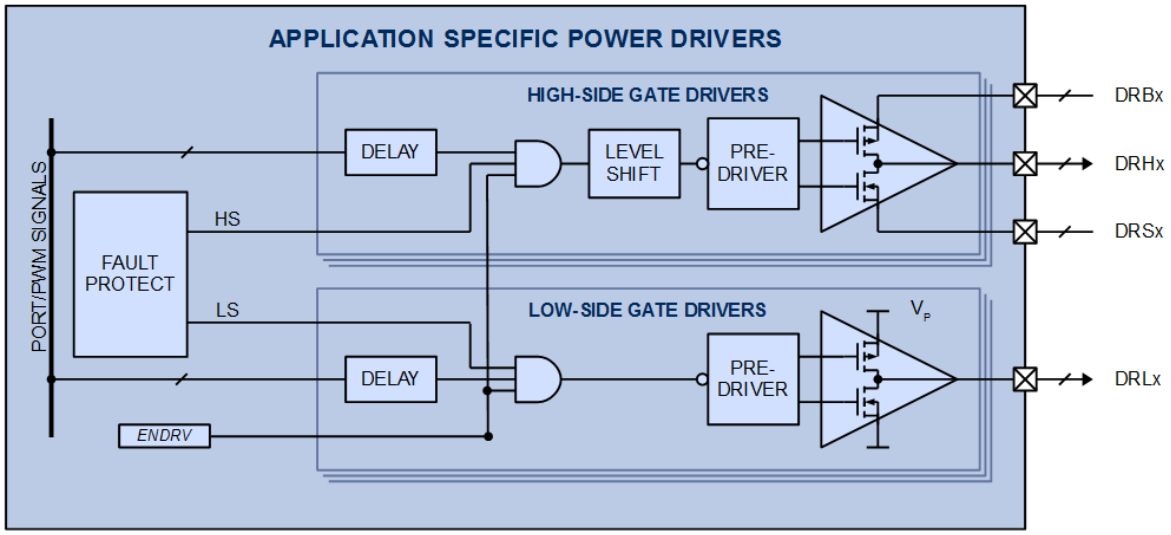
The Application Specific Power Drivers (ASPD) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

8.2 Features

- 3 low-side and 3 high-side gate drivers
- 1.5A gate driving capability
- Configurable delays and fast fault protection

8.3 System Block Diagram

Figure 8-1 ASPD System Block Diagram

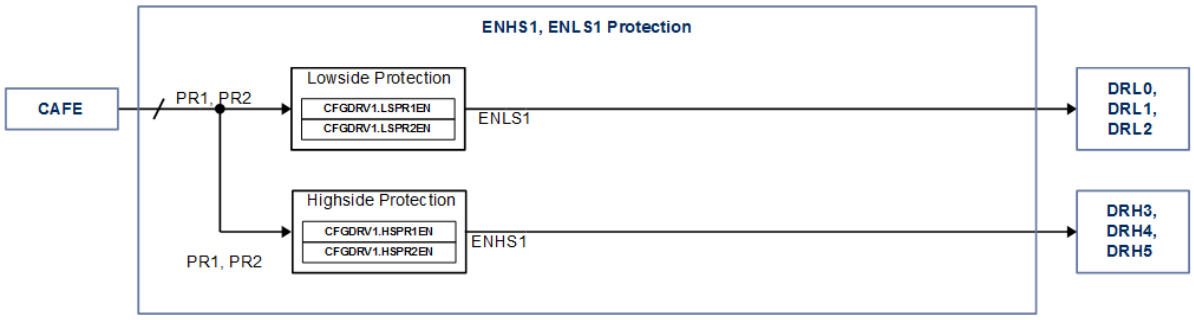


8.4 Enabling the ASPD

8.5 ENHS1, ENLS1 Protection

8.5.1 System Block Diagram

Figure 8-2 ENHS1, ENLS1 Protection



8.5.2 ENHS1, ENLS1 Protection

The PR1 and PR2 signals from the AIOx inputs in the CAFE can be used to disable the gate drivers in the ASPD, separated into two groups:

- The ENHS1 signal protects the high-side drivers DRH3, DRH4 and DRH5
- The ENLS1 signal protects the low-side drivers DRL0, DRL1 and DRL2

To enable the ENLS1 protection using PR1 as input, use **CFGDRV1.LSPR1EN**. To enable the ENHS1 protection using PR1 as input, use **CFGDRV1.HS1EN**.

To enable the ENLS1 protection using PR2 as input, use **CFGDRV1.LSPR2EN**. To enable the ENHS1 protection using PR2 as input, use **CFGDRV1.HS2EN**.

8.5.3 DRL0

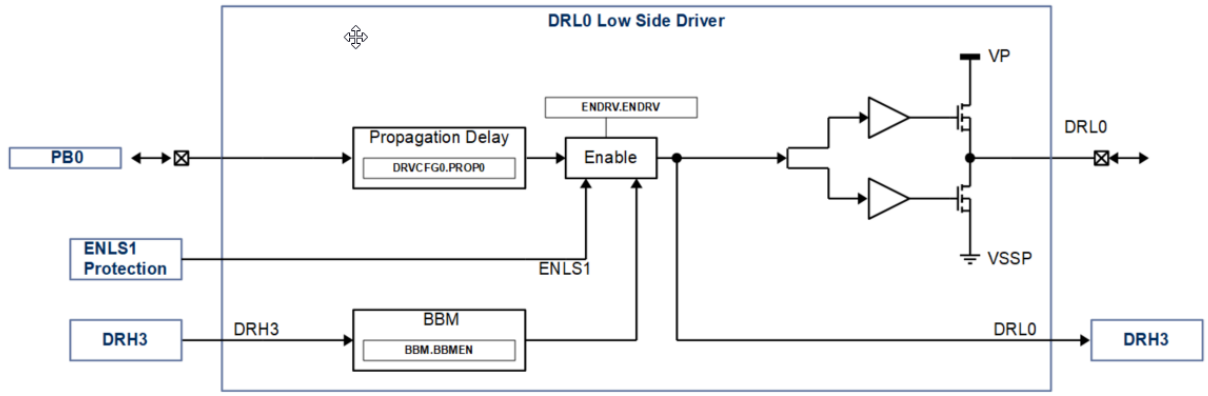
DRL0 is a push-pull low-side gate driver, controlled by a digital input from the MCU on pin PB0. The gate driver has configurable propagation delay, hardware dead-time, global driver enable, and configurable break-before-make with DRH3 and configurable protection disable with ENLS1 protection.

The propagation delay for the PB0 input to the DRL0 output may be configured using **CFGDRV0.PROP0** between 0 to 200ns.

To enable the ASPD (and DRL0) set **DRVCTL.DRVEN** to 1b. The protection signal ENLS1 will disable the ASPD if configured.

Break before make (BBM) control enforces that the high-side and low-side gate drivers for DRH3 and DRL0 are not on at the same time. To enable BBM control, set **ENBBM.ENBBM** to 1b.

Figure 8-3 DRL0 System Block Diagram



8.5.4 DRL1

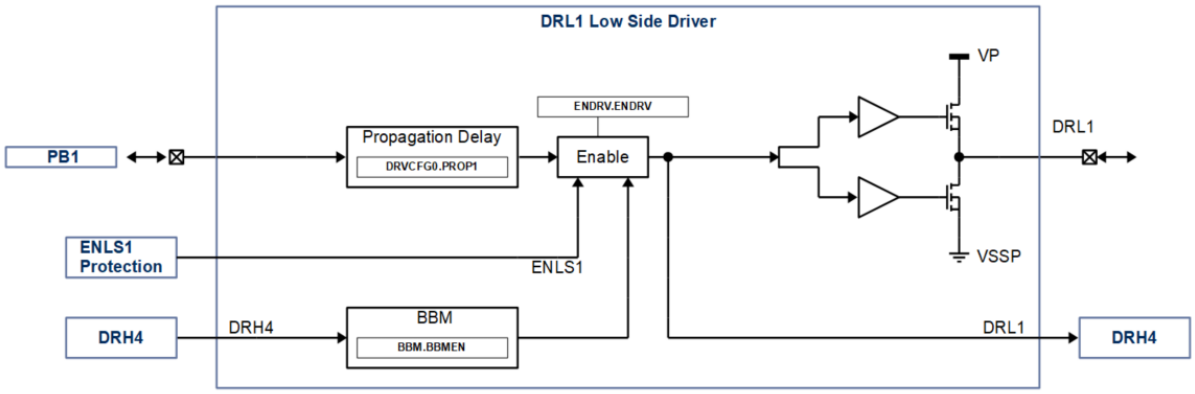
DRL1 is a push-pull low-side gate driver, controlled by a digital input from the MCU on pin PB1. The gate driver has configurable propagation delay, hardware dead-time, global driver enable, and configurable break-before-make with DRH4 and configurable protection disable with ENLS1 protection.

The propagation delay for the PB1 input to the DRL1 output may be configured using **DRVCFG0.PROP1** between 0 to 200ns.

To enable the ASPD (and DRL1) set **DRVCTL.DRVEN** to 1b. The protection signal ENLS1 will disable the ASPD if configured.

Break before make (BBM) control enforces that the high-side and low-side gate drivers for DRH4 and DRL1 are not on at the same time. To enable BBM control, set **BBMCTL.BBMEN** to 1b.

Figure 8-4 DRL1 System Block Diagram



8.5.5 DRL2

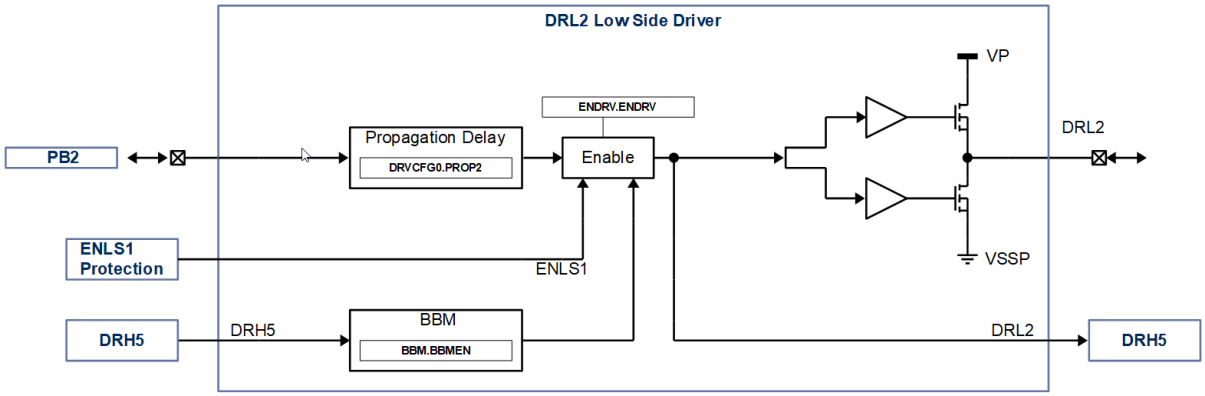
DRL2 is a push-pull low-side gate driver, controlled by a digital input from the MCU on pin PB2. The gate driver has configurable propagation delay, hardware dead-time, global driver enable, and configurable break-before-make with DRH5 and configurable protection disable with ENLS1 protection.

The propagation delay for the PB2 input to the DRL2 output may be configured using **DRVCFG0.PROP2** between 0 to 200ns.

To enable the ASPD (and DRL2) set **DRVCTL.DRVEN** to 1b. The protection signal ENLS1 will disable the ASPD if configured.

Break before make (BBM) control enforces that the high-side and low-side gate drivers for DRH5 and DRL2 are not on at the same time. To enable BBM control, set **BBMCTL.BBMEN** to 1b.

Figure 8-5 DRL2 System Block Diagram



8.5.6 DRH3

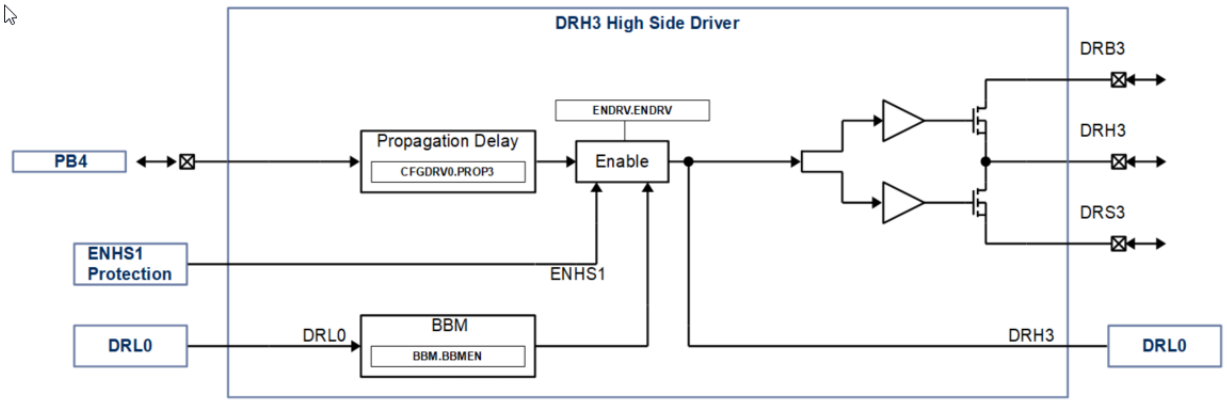
DRH3 is a push-pull high-side gate driver, controlled by a digital input from the MCU on pin PB4. The gate driver has configurable propagation delay, hardware dead-time, global driver enable, and configurable break-before-make with DRL0 and configurable protection disable with ENLS1 protection from the CAFE.

The propagation delay for the PB4 input to the DRH3 output may be configured using **DRVCFG0.PROP3** between 0 to 200ns.

To enable the ASPD (and DRH3) set **DRVCTL.DRVEN** to 1b. The protection signal ENLS1 will disable the ASPD if configured.

Break before make (BBM) control enforces that the high-side and low-side gate drivers for DRH3 and DRL0 are not on at the same time. To enable BBM control, set **BBMCTL.BBMEN** to 1b.

Figure 8-6 DRH3 System Block Diagram



8.5.7 DRH4

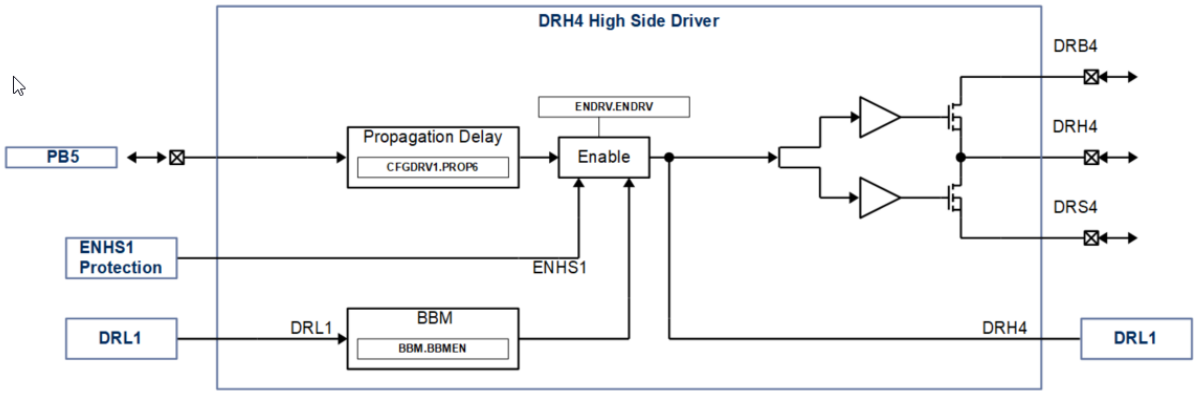
DRH4 is a push-pull high-side gate driver, controlled by a digital input from the MCU on pin PB5. The gate driver has configurable propagation delay, hardware dead-time, global driver enable, and configurable break-before-make with DRL1 and configurable protection disable with ENLS1 protection from the CAFE.

The propagation delay for the PB5 input to the DRH4 output may be configured using **DRVCFG1.PROP4** between 0 to 200ns.

To enable the ASPD (and DRH4) set **DRVCTL.DRVEN** to 1b. The protection signal ENLS1 will disable the ASPD if configured.

Break before make (BBM) control enforces that the high-side and low-side gate drivers for DRH4 and DRL1 are not on at the same time. To enable BBM control, set **BBMCTL.BBMEN** to 1b.

Figure 8-7 DRH4 System Block Diagram



8.5.8 DRH5

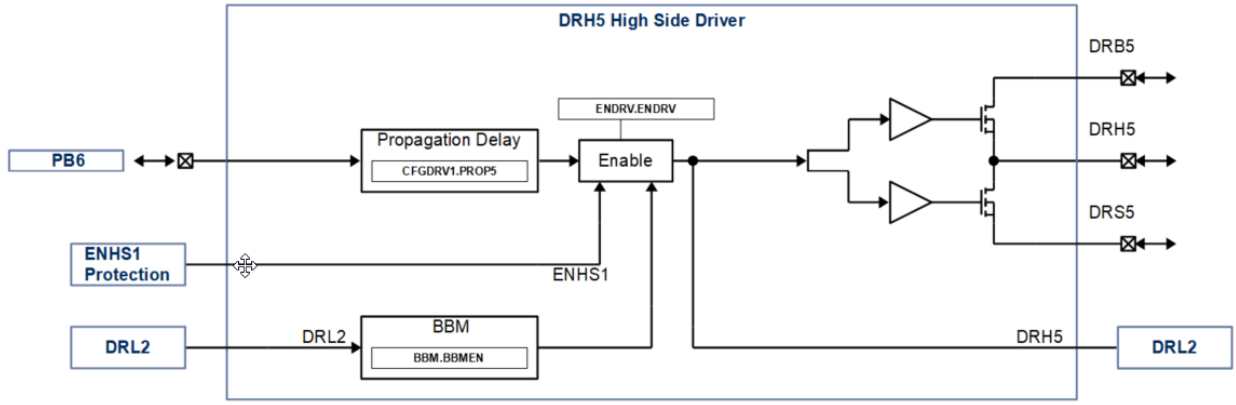
DRH5 is a push-pull high-side gate driver, controlled by a digital input from the MCU on pin PB6. The gate driver has configurable propagation delay, hardware dead-time, global driver enable, and configurable break-before-make with DRL1 and configurable protection disable with ENLS1 protection from the CAFE.

The propagation delay for the PB6 input to the DRH5 output may be configured using **DRVCFG1.PROP5** between 0 to 200ns.

To enable the ASPD (and DRH5) set **DRVCTL.DRVEN** to 1b. The protection signal ENLS1 will disable the ASPD if configured.

Break before make (BBM) control enforces that the high-side and low-side gate drivers for DRH5 and DRL2 are not on at the same time. To enable BBM control, set **BBMCTL.BBMEN** to 1b.

Figure 8-8 DRH5 System Block Diagram



8.6 Register Summary

Table 8-1 ASPD Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
60h	**DRVCFG0**	Driver Configuration 0	00h
61h	**DRVCFG1**	Driver Configuration 1	00h
62h	**CLKOUTCFG**	CLKOUT Configuration	00h
63h	**DRVCFG2**	Driver Configuration 2	00h
66h	**DRVCTL**	Gate Driver Control	00h
67h	**ENBBM**	Protection Control	00h
68h	**PROTCTL**	Driver Protection Control	00h

8.7 Register Detail

8.7.1 DRVCFG0

Register 8-1 DRVCFG0 (Driver Configuration 0, 60h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**PROP3**	RW	00b	Propagation delay for DRL3, DRH3 or OP3. 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
5:4	**PROP2**	RW	00b	Propagation delay for DRL2. 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
3:2	**PROP1**	RW	00b	Propagation delay for DRL1. 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
1:0	**PROP0**	RW	00b	Propagation delay for DRL0. 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns

8.7.2 DRVCFG1

Register 8-2 DRVCFG1 (Driver Configuration 1, 61h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HSPR1EN**	RW	0b	High side PR1 protection enable. 0b: PR1 disabled 1b: PR1 enabled
6	**HSPR2EN**	RW	0b	High side PR2 protection enable. 0b: PR2 disabled 1b: PR2 enabled
5	**LSPR1EN**	RW	0b	Low side PR1 protection enable. 0b: PR1 disabled 1b: PR1 enabled
4	**LSPR2EN**	RW	0b	Low side PR2 protection enable. 0b: PR2 disabled 1b: PR2 enabled
3:2	**PROP5**	RW	00b	Propagation delay for DRL5, DRH5 or OP5. 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns
1:0	**PROP4**	RW	00b	Propagation delay for DRL4, DRH4 or OP4. 00b: 0ns 01b: 50ns 10b: 100ns 11b: 200ns

8.7.3 CLKOUTCFG

Register 8-3 CLKOUTCFG (CLKOUT Configuration, 62h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**Reserved**	RW	00b	Reserved, write to 0.
2	**EN_CLKOUT**	RW	00b	Enable CLKOUT: 0b: disabled 1b: enabled
1:0	**CLKOUTSEL**	RW	0b	Setting for CLKOUT: 00b: High-Z 01b: 250Hz 10b: 580Hz 11b: 1.16kHz

8.7.4 DRVCFG2

Register 8-4 DRVCFG2 (Driver Manager Configuration 2, 63h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**Reserved**	RW	0	Reserved, write to 0.
1	**PULSEEXTDIS**	RW	0b	Disable Pulse extension: 0b: Pulse extension enabled 1b: Pulse extension disabled
0	**Reserved**	RW	0	Reserved, write as 0.

8.7.5 DRVCTL

Register 8-5 DRVCTL (ASPD Control, 66h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	**Reserved**	RW	0	Reserved, write to 0.
0	**DRVEN**	RW	0b	Application Specific Power Driver Enable. 0b: disabled 1b: enabled

8.7.6 ENBBM

Register 8-6 ENBBM (Enable break before make, 67h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	**Reserved**	RW	0	Reserved, write to 0.
0	**ENBBM**	RW	0b	Break before make enable: 0b: disabled 1b: enabled

8.7.7 PROTCTL

Register 8-7 PROTCTL (Driver Protection Control, 68h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	**Reserved**	RW	0	Reserved, write to 0.
0	**PROTCTL**	RW	0b	Select input signal for PROT: 0b: PR1 1b: nIRQ2

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