NOTES (UNLESS OTHERWISE SPECIFIED):

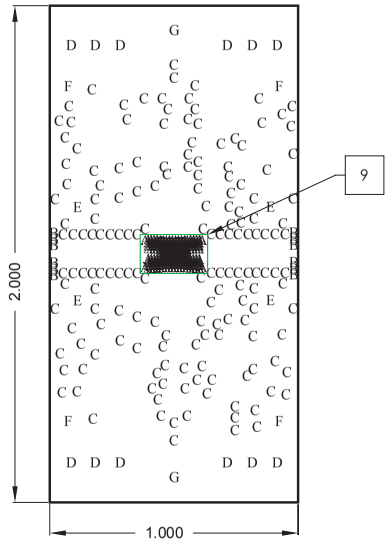
1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. MATERIAL:
   NUMBER OF LAYERS: 2 LAYERS
   METAL 1 (TOP): 0.5oz.
   CORE 1: ROGERS 4003C, 0.008in. THICK
   METAL 2 (BOTTOM): 0.5oz.
   SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), BLUE.
   OR LDI (LASER DIRECT IMAGEABLE), BLUE.
   MAX FINISH THICKNESS OF SOLDERMASK TO BE 0.001in.
   SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
4. FINISH PLATING:
   ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
   NICKEL PLATE per IPC-4552, 118 - 236µin. (3 - 6µm)
   IMMERSION GOLD (10uin) IAW IPC-4552, CLASS 3
5. FINISHED BOARD THICKNESS: (0.012in).
6. COPPER IS PULLED BACK 0.002in. GROUND PLANE ONLY FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM). THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
7. TOLERANCE: PC BOARD OUTLINE: ±0.002in.
8. BURRS SHALL NOT EXCEED 0.002in.
9. VIA PLATING/FILLING:
   ALL VIAS UNDER THE DUT ARE TO BE:
   COPPER-FILLED, OVER-PLATED AND PLANARIZED. FINISHED COPPER THICKNESS TO BE 0.0014 ±0.0004in.
   ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
10. METAL 1 TOP AND METAL 2 BOTTOM SHALL BE PLANARIZED AFTER PLATING HOLES SHUT.
    MAX ALLOWABLE NEGATIVE FEATURE 0.0008in. MAX ALLOWABLE POSITIVE FEATURE 0.0003in.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.003in. OF CAD DATABASE.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.001 OF CAD DATABASE.
14. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
15. DELIVER BOARDS BAGGED AS: SINGLES
16. NO ELECTRICAL TEST NEEDED.

DRILL TABLE

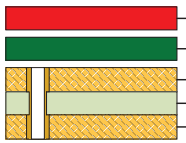
Symbol	Count	Hole Size	Plated	Via / Pad
A	168	0.006	Plated	Via
B	12	0.012	Plated	Via
C	167	0.020	Plated	Via
D	12	0.035	Plated	Pad
E	4	0.081	Plated	Pad
F	4	0.086	Non-Plated	Pad
G	2	0.120	Non-Plated	Pad

REVISION HISTORY

REV	DESCRIPTION	DATE	APPROVAL
B	UPDATE DOCUMENT TITLE TO MATCH DC FOR BOM RELEASE	01/30/18	KWEAY



Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type
	SILKSCREEN_TOP			Legend
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask
Copper	METAL1_TOP	0.0007in		Signal
Core		*0.0080in*	*ROGERS 4003C*	*Dielectric*
Copper	METAL2_BOTTOM	0.0007in		Signal

Total thickness: 0.0098in

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES

TOLERANCES
.XX = ±.01
.XXX = ±.005
.XXXX = ±.0010
ANGLES = ± 0.5°

INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009

THIRD ANGLE PROJECTION

DO NOT SCALE DRAWING

SAP NO. 283636

APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE

		DATE
DESIGNER	K. WEAY	02/13/17
ENGR.	B. LORAN	02/13/17

PDE CONTROLLED

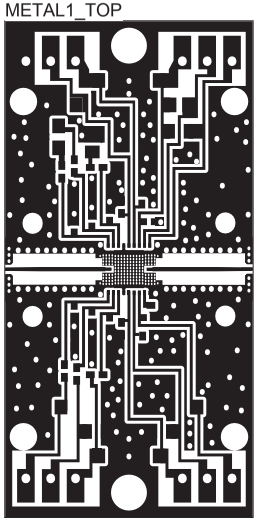
CAGE CODE 1CVM1

TITLE:
TGA4548-SM EVALUATION PCB DESIGN PACKAGE

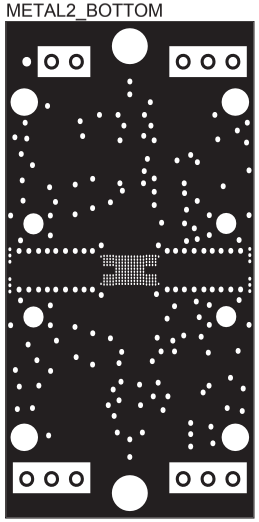
SIZE B | DWG. NO. TGA4548-SM-4000 | REV. B

SCALE: 1:1 | SHEET 1 OF 3

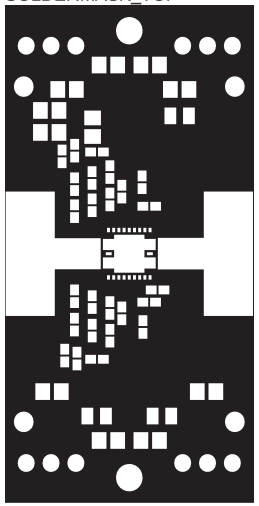
METAL1_TOP



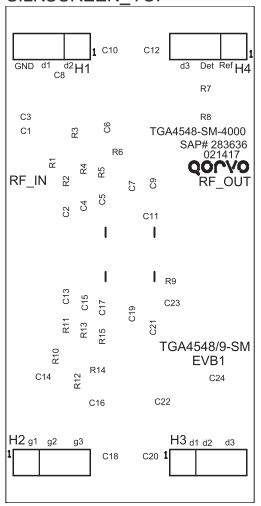
METAL2_BOTTOM



SOLDERMASK_TOP



SILKSCREEN_TOP



SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	TGA4548-SM-4000	B

SCALE: 1:1 SHEET 2 OF 3

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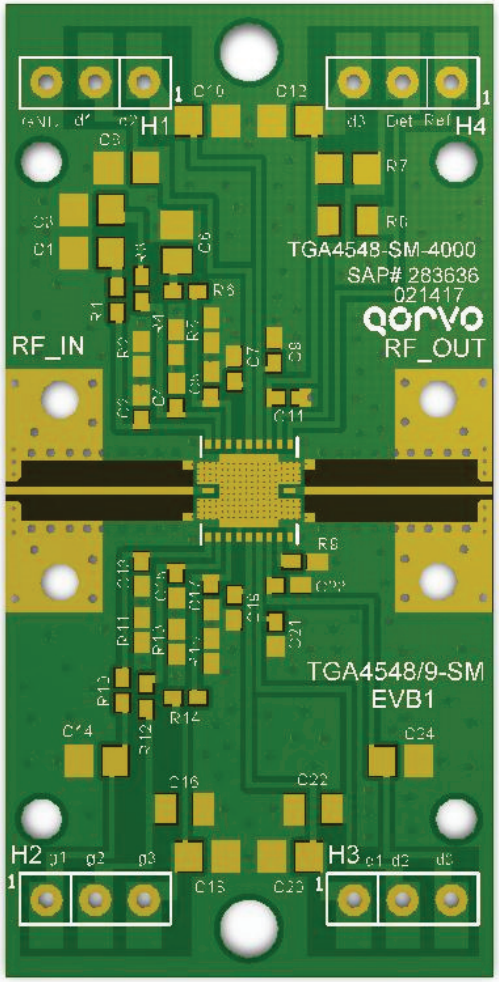

SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	TGA4548-SM-4000	B

SCALE: 1:1 SHEET 3 OF 3

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