WHITE PAPER

How to Identify a Suspected FEM Failure in a Wi-Fi System Board

A standard guideline for troubleshooting a system board when there is a suspected FEM failure

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Executive Summary

This white paper provides a standard set of steps for troubleshooting a Wi-Fi system board with a suspected front-end module (FEM) failure. It is based on the method used by Qorvo's Applications Engineering Group, which is responsible for successfully integrating Qorvo's products into customer systems. Applications and engineering personnel should be able to quickly isolate problems by following seven steps, which include checking the assembly and biasing the part, to determine whether the FEM meets specifications or if it is damaged. Checking the performance of other areas, such as the output power level from the transceiver and the post-FEM network insertion loss, which will further help to determine where the root cause lies. This painstaking work must be handled delicately, so that the system board is still in working condition after multiple tests.

Introduction

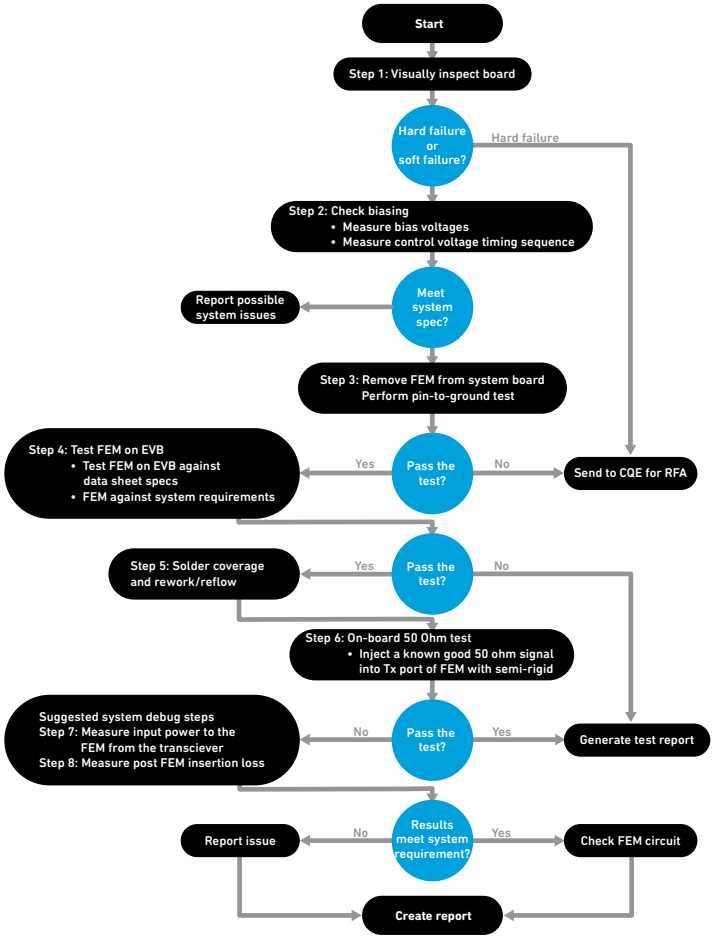
Qorvo's Applications Engineering Group is responsible for successfully integrating Qorvo's products into customer systems. Often, we are requested by a customer to debug or verify system boards or modules that are not working or not performing to expectations, in cases where the problems are suspected to be due to failure of a Qorvo FEM. We perform a standard set of steps and tests to resolve the problem in a timely way and determine whether the issue lies within the FEM. This white paper describes the steps in that process. The goal of the white paper is to help engineers at Wi-Fi product manufacturers troubleshoot problems.

This process would typically be used when Wi-Fi engineers find that their system outputs are not meeting specifications and need to diagnose the problem. In this white paper, we use the example of a design that utilizes the Qorvo QPF4519 Wi-Fi FEM.

Troubleshooting Process

The steps in the troubleshooting process are outlined in Figure 1 and described in more detail below.

Figure 1. System board FEM troubleshooting flow chart.



Step 1. Visually Inspect the Board

Before powering on the system board, disassemble and visually inspect the circuit board to make sure all components around the FEM are present and populated according to the system board schematic (Figures 2, 3). It is also important to examine the FEM for any visible damage, to determine if this is a *Hard Failure* or a *Soft Failure.*

Figure 2. System board disassembly drawing.

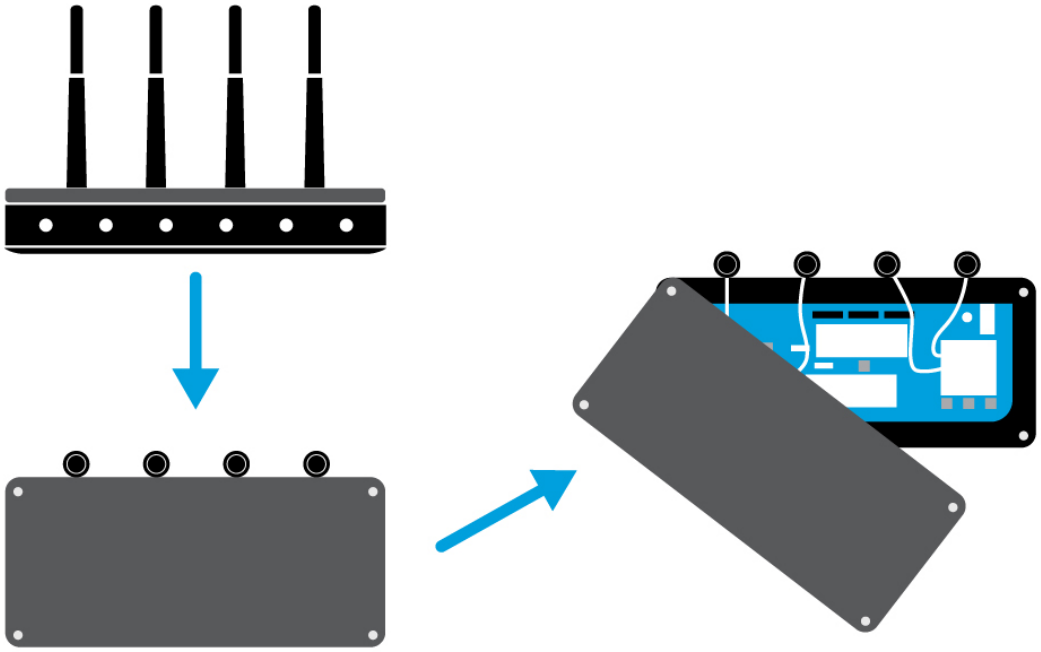
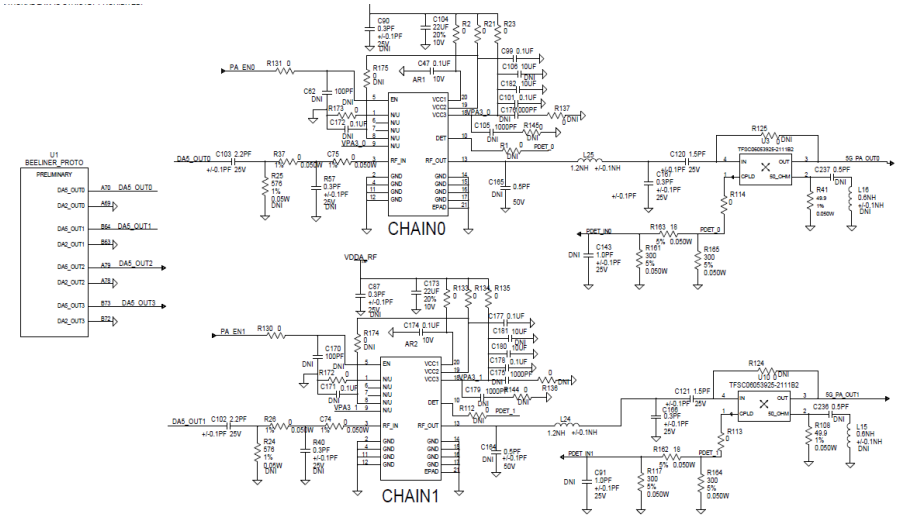


Figure 3. System board front-end schematic.



Visual inspection checklist:

a. Check for missing or incorrect components; i.e. make sure all series components are in place.
b. Check for shorted, incorrect or missing traces.
c. Check for solder balls, splatter or solder bridging.
d. Check for V_{CC} node shorts. A V_{CC} short to ground can be due to several reasons including a bad part, bad soldering or bad layout.
e. Check for visible damage to the FEM.

If the FEM is deformed or has other visible damage such as a burn spot or hole, it is obviously damaged, and the problem should be considered a Hard Failure. A FEM with a Hard Failure should be sent to the suppliers Quality Control Engineer (QCE) for a Return Failure Analysis (RFA). If there is no visible damage to the FEM the problem is assumed to be a Soft Failure; continue to step 2.

Step 2. Check Biasing

Step 2 is to check the FEM's biasing. Power up the system board with the output antenna connectors properly terminated and measure the FEM's V_{CC} and control voltages. When powering up the board for the first time, make certain that there is no smoke or burning, as this clearly demonstrates electrical issues such as a V_{CC} short or other short circuit to ground. If there is no V_{CC} issue on the system board, proceed to the next step in troubleshooting the RF front end.

How to check biasing:

a. Use a multimeter to measure the voltage at each pin of the FEM and determine which mode it is in (referring to the datasheet or application note).
b. Connect all control pins to an oscilloscope and check dynamic biasing against the QPF4519 Logic Truth Table (Table 1).
c. Does the control voltage timing sequence and levels match the datasheet? If not, then there may be a system design problem.
d. If yes, then check system performance.
e. If system performance does not meet specs, then move to step 3.

Table 1. QPF4519 logic truth table.

Logic Truth Table

Mode	PA_EN	C0	C1
Standby	Low	Low	Low
Transmit	High	Low	High
LNA On	Low	High	Low
Bypass	Low	High	High

Figures 4, 5 and 6 below demonstrate an example of where to place the oscilloscope probes when checking dynamic biasing, and how the voltage timing should appear on the oscilloscope when comparing the result to the QPF4519 Timing Diagram.

Figure 4. Oscilloscope probe locations.

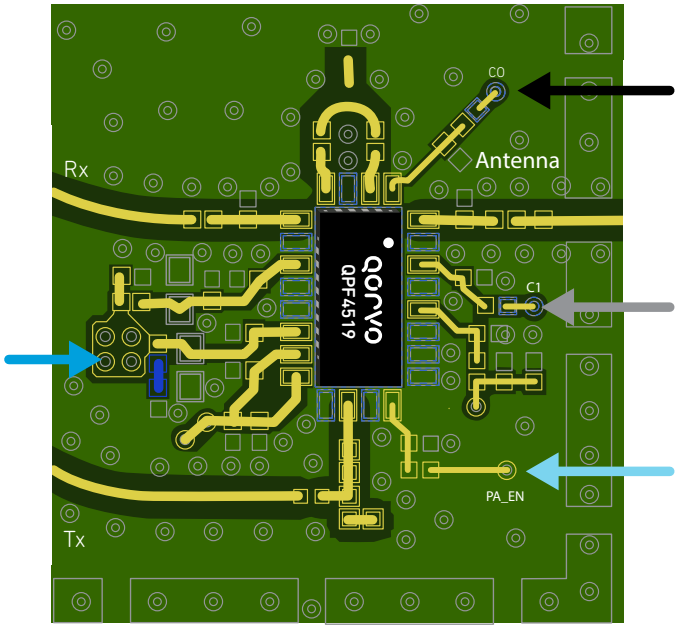


Figure 5. Oscilloscope screenshot.

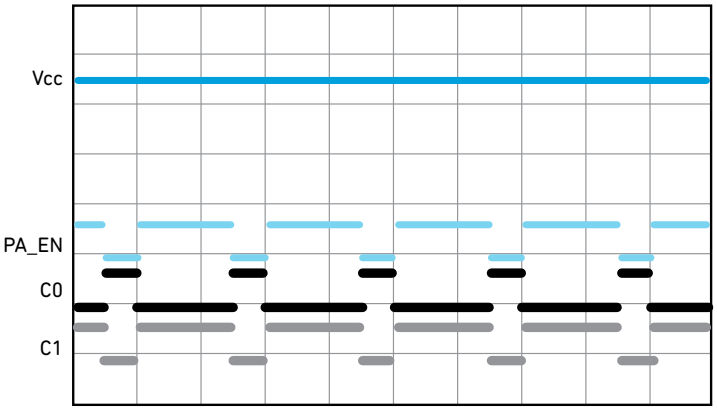
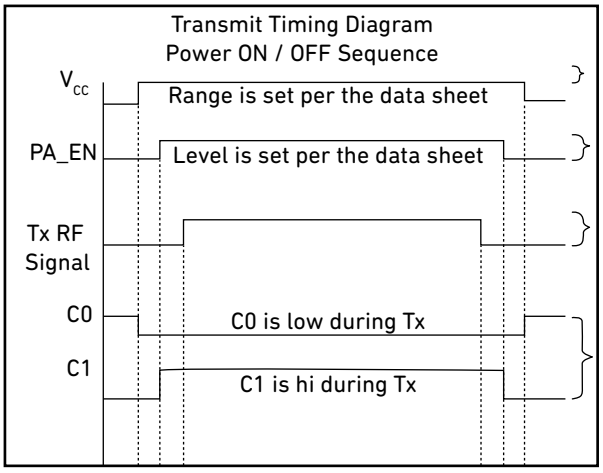


Figure 6. Application note transmit timing diagram.



Step 3. Test Pin-to-Ground

A Pin-to-ground test must be done on the FEM to determine if it is damaged. The Pin-to-ground test results should be compared to the results observed with a control part.

Test procedure:

a. Remove the device under test (DUT) from the system board and measure the Pin-to-ground resistance with a multimeter.
b. If the part passes the Pin-to-ground test (no short on V_{CC} and Control Pins), then move to step 4.
c. If it fails, the result suggests that the part is damaged. Submit a Return Failure Analysis (RFA) request to the suppliers' Customer Quality Engineering (CQE), which will perform more detailed failure analysis tests such as X-Ray Inspection, I-V Curve Tracing and Optical Die Inspection. Table 2 shows an example set of test results.

Table 2. Example of Pin-to-ground test report.

Pin	Function	CTRL-1	CTRL-2
	Trace Code	54 VN	54 VN
1	GND	0	0
2	Tx_IN	0	0
3	GND	0	0
4	PA_EN	1.16 M	1.16 M
5	NC	OL	OL
6	NC	OL	OL
7	GND	0	0
8	DC_PDET	2.1 K	2.11 K
9	GND	0	0
10	C1	0.64 M	0.68 M
11	NC	0	0
12	ANT	0L	0L
13	C0	0.63 M	0.67 M
14	Rx_Out	0L	0L
15	GND	0L	0L
16	LNA_IN	49.6 M	62.2 M
17	LNA_OUT	49.3 M	61.9 M
18	GND	0	0
19	V_{DD}	358 K	315 K
20	GND	0L	0L
21	GND	0	0
22	$V_{CC}3$	119.2 M	128.5 M
23	$V_{CC}2$	227 M	223.2 M
24	$V_{CC}1$	0.47 M	0.47 M

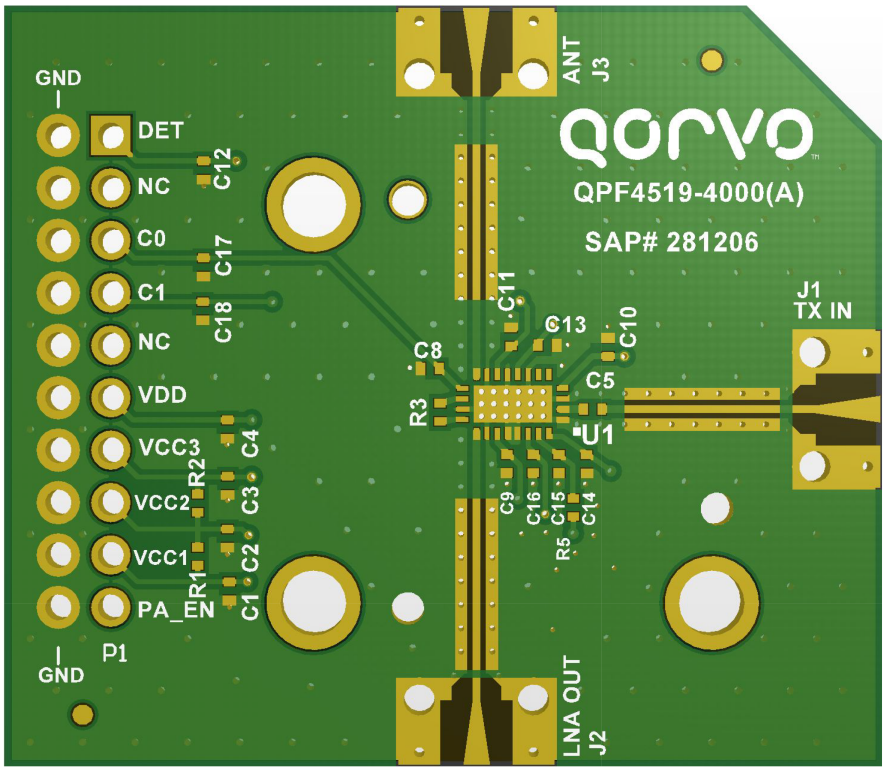
Step 4. Test Part in 50 Ω Environment on Qorvo EVB

An effective way to identify whether the problem is due to an FEM failure is to test the FEM on an Evaluation Board (EVB). This is a quick and easy way to identify whether the FEM functions fully to datasheet specifications, partially meets specifications or fails. The EVB is designed to test the FEM in a 50 Ω system to compare performance with datasheet specifications.

If an EVB is available, the FEM should be mounted on it and tested. The steps are:

a. Remove DUT from customer board and solder the part onto a known working EVB.
b. Test the part on the EVB according to the EVB test plan or your company's test conditions.
c. If the DUT meets the EVB specifications or your company's specifications, continue to step 5. If not, generate a test report that identifies the failing parameters.

Figure 7. Qorvo QPF4519 evaluation board.



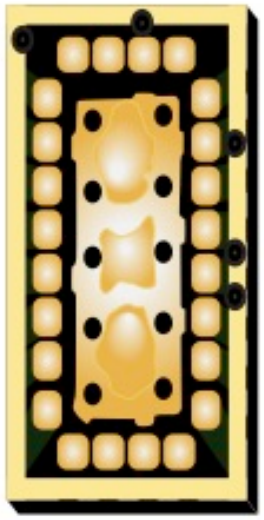
Step 5. Check Solder Coverage

Checking the FEM ground solder coverage will help to pin down the root causes. Qorvo's manufacturing notes recommend a minimum of 85% to 90% solder coverage on pads and complete coverage on ground pads for most of the Qorvo Wireless Connectivity parts. Poor solder coverage will degrade the FEM performance. The photo in Figure 8 illustrates poor solder coverage on a PCB ground pad.

To check the solder coverage:

a. Check solder coverage and voids on backside ground (GND slug).
b. Check solder coverage and voids on PCB ground pad.
c. Recover ground pad with complete solder coverage and reflow (repopulate) part.
d. Redo Step 2d in the troubleshooting process to see if the expected output power is achieved.
e. If Step 2d fails then continue to Step 6.

Figure 8. PCB ground pad with bad solder coverage.

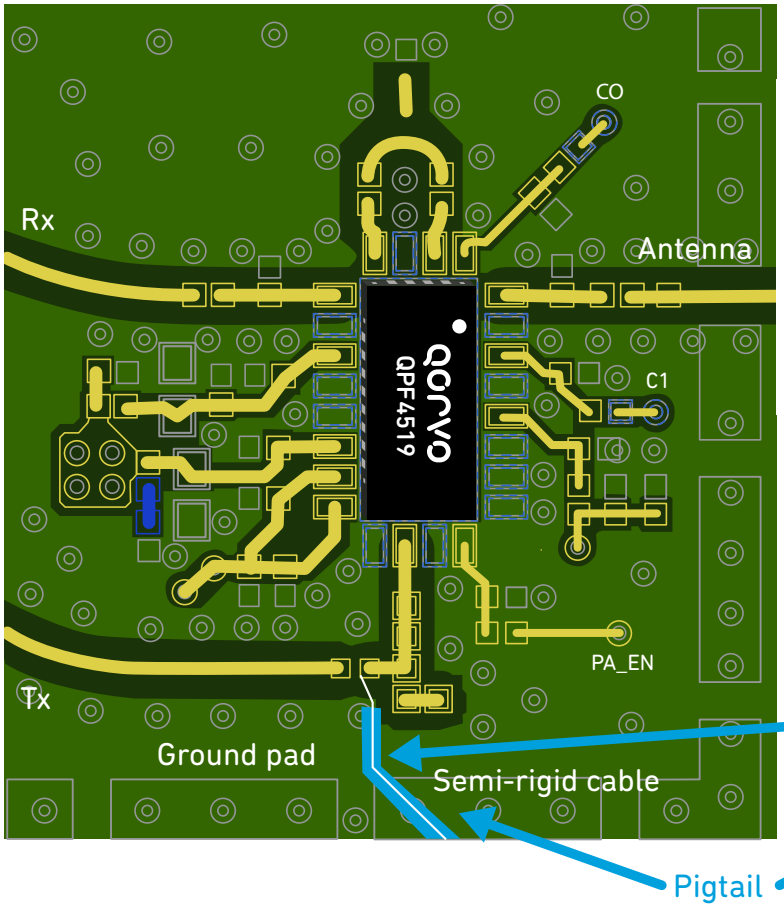


Step 6. On-Board 50 Ω Test

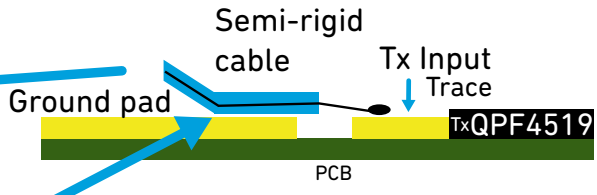
This step will further help determine if the problem lies within the FEM.

a. Place a pigtail at the transmit node of the FEM to verify that the FEM is performing correctly by using a known input signal from a signal generator and manually biasing the FEM.
b. Measure the antenna power output to determine if it aligns with the datasheet value. For example, for the QPF4519, the output should be 20 dBm with an input signal of ~-11 dBm at 5.21 GHz.
c. If the antenna output measures 20 dBm, we know the FEM is performing correctly. Note that you can also measure gain, linearity and Error Vector Magnitude (EVM) using this technique.
d. If the FEM fails the on-board 50 Ω test, create a test report.

Figure 9. Semi-rigid cable solder location.



a. tPlace a pigtail at the transmit node of the FEM to verify the FEM is performing correctly by using a known input signal from a signal generator and manually bias the FEM.
b. Then measure the antenna power output to determine if it aligns with the data sheet value of 20 dBm. For an input signal of ~ -11 dBm at 5.21 GHz for example.
c. If the output of the antenna measures 20 dBm then we know the FEM is performing properly. Note, you can also measure – gain, linearity and EVM using this technique.
d. If it fails, the on board 50Ω test then a test report is done.



System Debug – System Budget and Loads

If the FEM is still not performing properly on the system board after steps 1-6, it is possible that the problem is caused by other components on the board rather than the FEM.

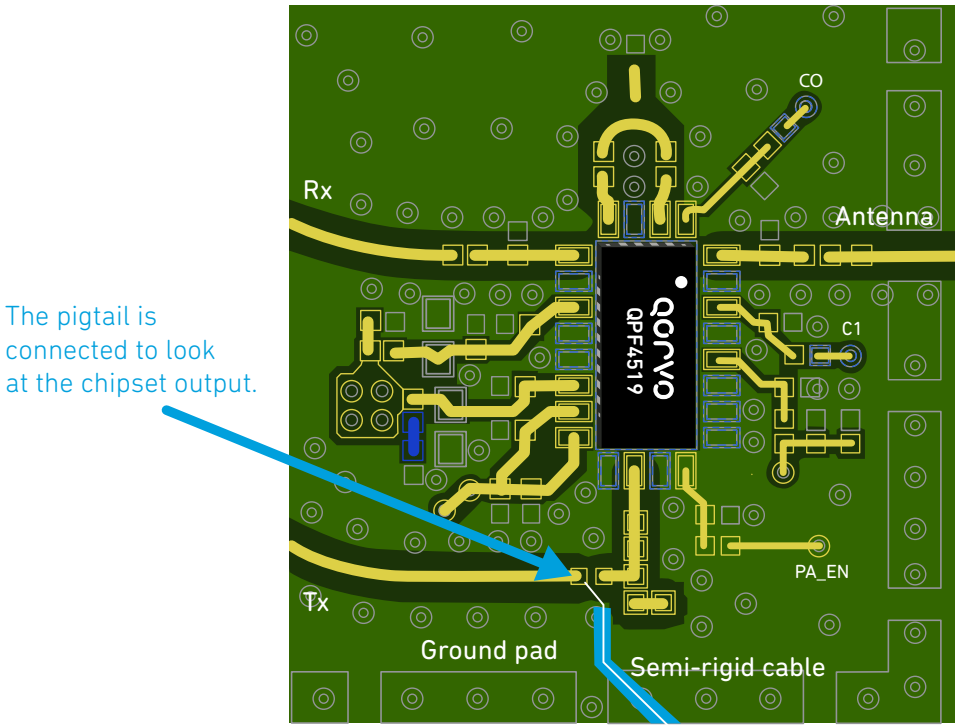
In this event, the suggested debug process is to measure the input power from the chipset (Step 7) and examine the post-FEM circuit (Step 8). Both steps will determine possible root causes related to FEM application circuitry, which major section (TXCVR or post-FEM components) should be investigated further, and whether further circuit optimization (tuning) is required.

Step 7. Measure Input Power to the FEM from the Transceiver (TXCVR)

This step will determine if the problem lies with the TXCVR drive signal. The chipset transceiver output to the FEM is measured to determine whether it meets the system requirement.

a. Remove FEM and solder pigtail at the FEM TX input, and measure input power to the FEM from the TXCVR as shown in Figure 10.
b. If possible, also record the load to the FEM from the TXCVR signal.

Figure 10. Semi-rigid cable solder location.



Step 8. Measure Post-FEM Circuit

At this point, you have basically ruled out the FEM as the cause of the issue.

To measure the post-FEM circuit:

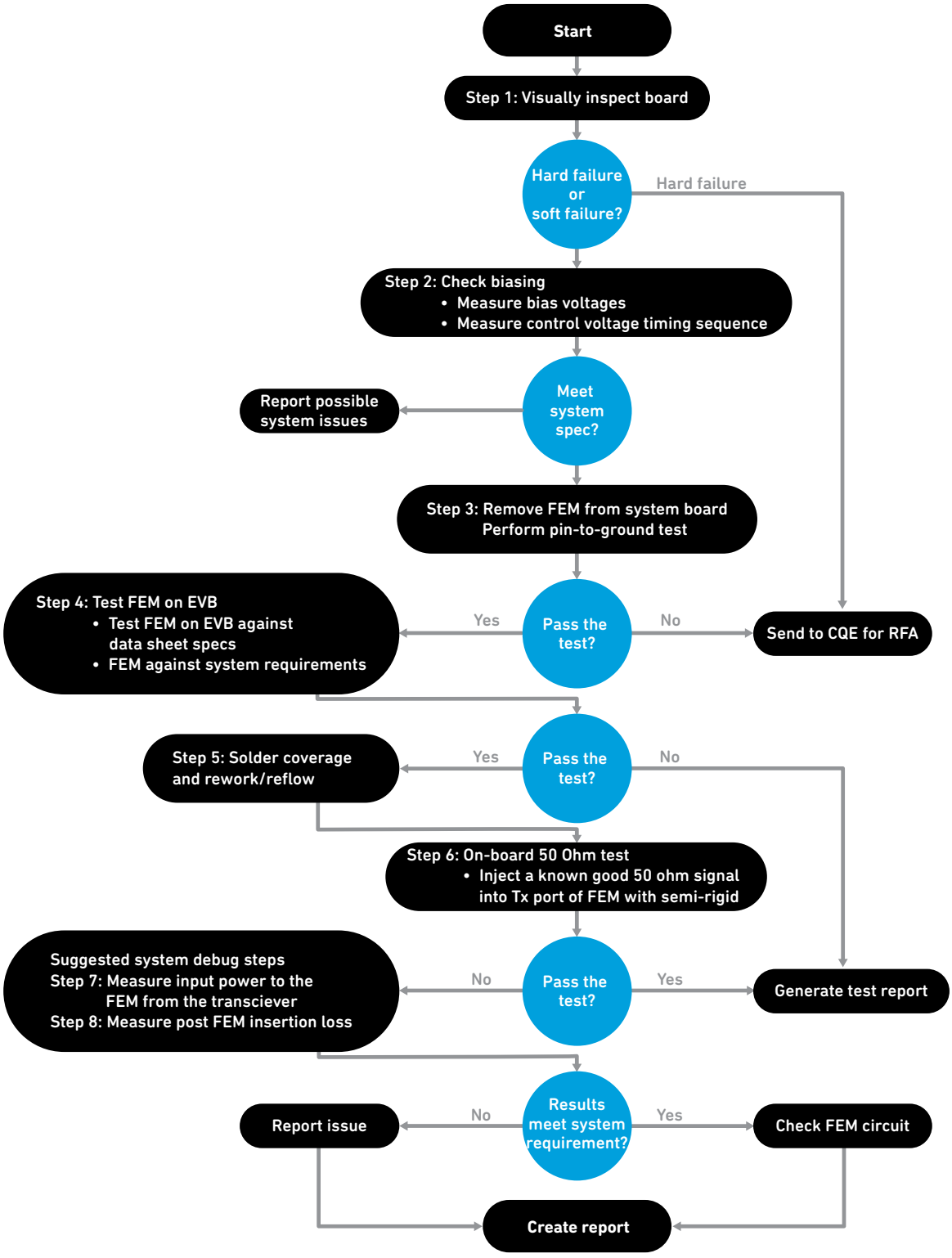
a. With the FEM removed from system board, solder a pigtail at the FEM antenna port pad. Do small signal test from the pigtail at the FEM antenna port to the system antenna port. Check if the insertion loss meets the system design specification.

System Budget Summary

Recording and reviewing the results of the tests on the pre-FEM and post-FEM circuits (steps 7 and 8) enables you to determine if they meet system specifications. If there is no issue with the pre- and post-FEM circuits then recheck the FEM circuit and generate a report.

Conclusion

Applications and engineering personnel should be able to quickly isolate suspected Wi-Fi FEM problems by following the steps described ion this white paper, which include checking the assembly and biasing the part. This should enable engineers to determine whether the FEM meets specifications or if it's damaged. Checking the performance of other areas such as the output power level from the TXCVR and the post-FEM network insertion loss will further help to determine where the root cause lies.


Start
Step 1: Visually inspect board
Hard failure or soft failure?
Hard failure
Step 2: Check biasing
• Measure bias voltages
• Measure control voltage timing sequence
Meet system spec?
Report possible system issues
Step 3: Remove FEM from system board
Perform pin-to-ground test
Step 4: Test FEM on EVB
• Test FEM on EVB against data sheet specs
• FEM against system requirements
Yes
Pass the test?
No
Send to CQE for RFA
Step 5: Solder coverage and rework/reflow
Yes
Pass the test?
No
Step 6: On-board 50 Ohm test
• Inject a known good 50 ohm signal into Tx port of FEM with semi-rigid
Suggested system debug steps
Step 7: Measure input power to the FEM from the transciever
Step 8: Measure post FEM insertion loss
No
Pass the test?
Yes
Generate test report
Report issue
No
Results meet system requirement?
Yes
Check FEM circuit
Create report