# Application Note PAC2xxxx Stacking BMS Devices

***Power Application Controller® Battery Management***

# 1 PAC2xxxx BMS Devices

The Qorvo® PAC2xxxx are a family of Intelligent Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs. They integrate a FLASH-programmable MCU, Power Management, Current/Voltage/Temperature Sense and drive circuits for charge/discharge FETs and protection fuses. It can communicate using UART, SPI I2C/SMBus serial interfaces. The devices provide access to multiple analog and digital peripherals required to safely manage today's high cell count battery packs. Additional information is available on Qorvo's web page Battery Management Devices - Qorvo.

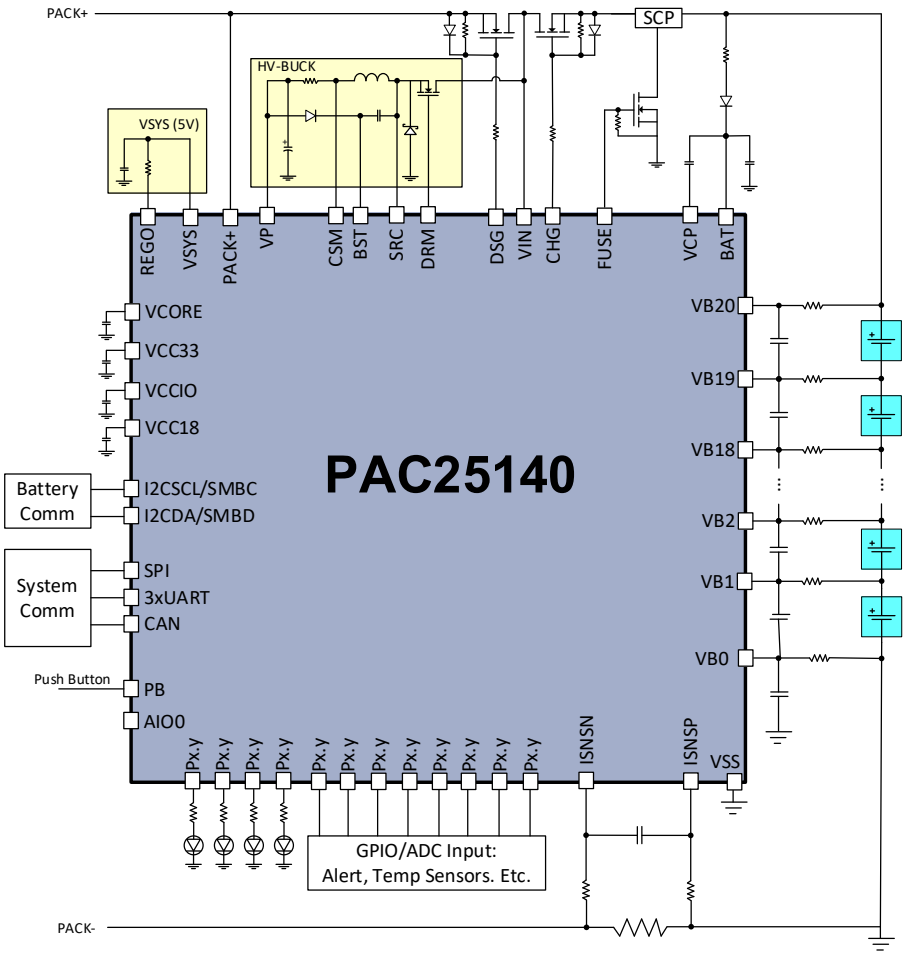


*Figure 1 Standard Application Diagram*

## 2 Introduction of Stacking Qorvo BMS Devices

A single PAC25140 IC BMS can monitor up to 20-series battery cells due to the fab process selection limiting the maximum voltage rating. In many large battery cell count battery applications (>20 cells in series), the system may require multiple integrated circuits (ICs) to cover the full stack of cells. By using multiple PAC2xxxx devices in a stack of modules, the system can monitor and balance the high number of cells in sets of 20 cells. For example, if the system requires 60 battery cells in series, this will require three IC's each supporting 20 cells which could provide the system 150V to 265V.
The difficulty of building a single IC device to cover 60 cells would be very expensive and require a complex fabrication process. By using three ICs to cover the whole battery pack, you can divide the voltage stack into 20 cell modules, as in figure 2.

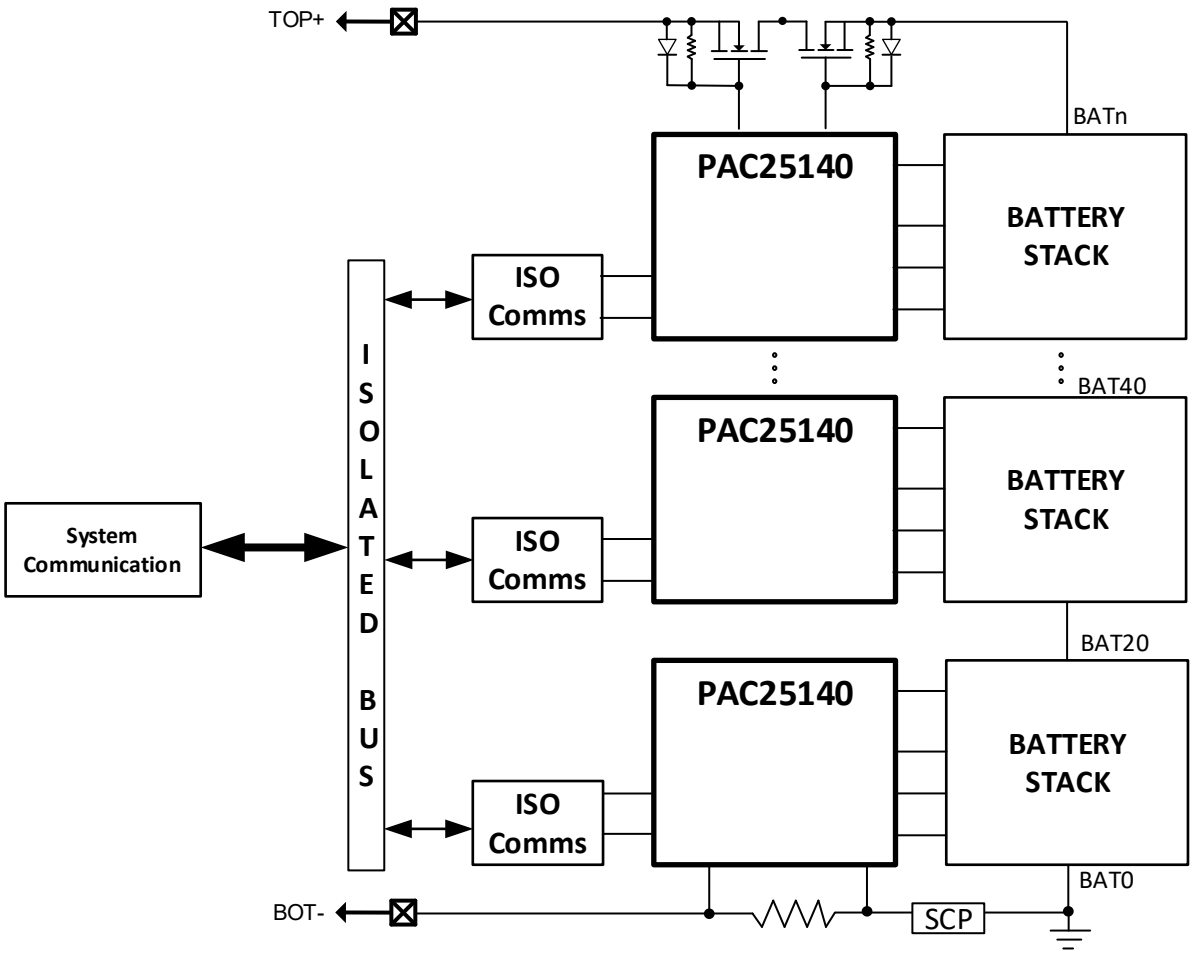


*Figure 2 **Example Diagram of Stacking BMS Devices***

## 2.1 Considerations When Stacking BMS Devices

To cover battery packs with higher than 20s cells, multiple BMS devices of PAC2x140 are required to monitor the stacked cells. The control master device typically sits on the bottom and shares the ground with the pack negative terminal, making system level communications easy. The rest of the stacked PAC2x140 devices are stacked and ground is the top of the last stack. This is why an isolation device, or a high-voltage level shifter is required for the communications between the master BMS IC and the rest of the stack.

Communication along the stack can be any isolated protocol. PAC25140 supports I2C, SPI, UART/RS-485, or CAN bus. The bottom master device can use isolation, or not, since it is on the same ground reference as the system depending on the noise and any ground shift the system could experience.

For safety reasons, the FET control will need to be a shared signal among all the stacked devices. Especially critical is the short circuit and over current detection and shut-off control from the master BMS on the bottom of the stack to the high-side FETs on the top of the stack. This needs to be as fast as possible.

## 2.2 Stacking BMS Devices Communication

When stacking you will need to consider how to maintain communication and control of the modules. The IC on the bottom is ground reference, so standard communication works. The next module is sitting on top of the 20 cells voltage, and therefore isolated communication that can float up to that higher voltage is needed. For the example application, isolated I2C was chosen, see figure 2. However, UART using RS-485, or CAN could be considered.

## 2.3 FET Control Issues with Stacking BMS devices

Stacking BMS devices requires a good review of the issues. One issue is which device controls protection FETs, and the control for these FETs is limited to the voltages of the stack the devices is monitoring. In particular, the discharge FET can be difficult to control as the BOT node or pack negative node can be several modules down and the Gate to Source voltage of the discharge protection FET will increase beyond the device absolute maximum rating.

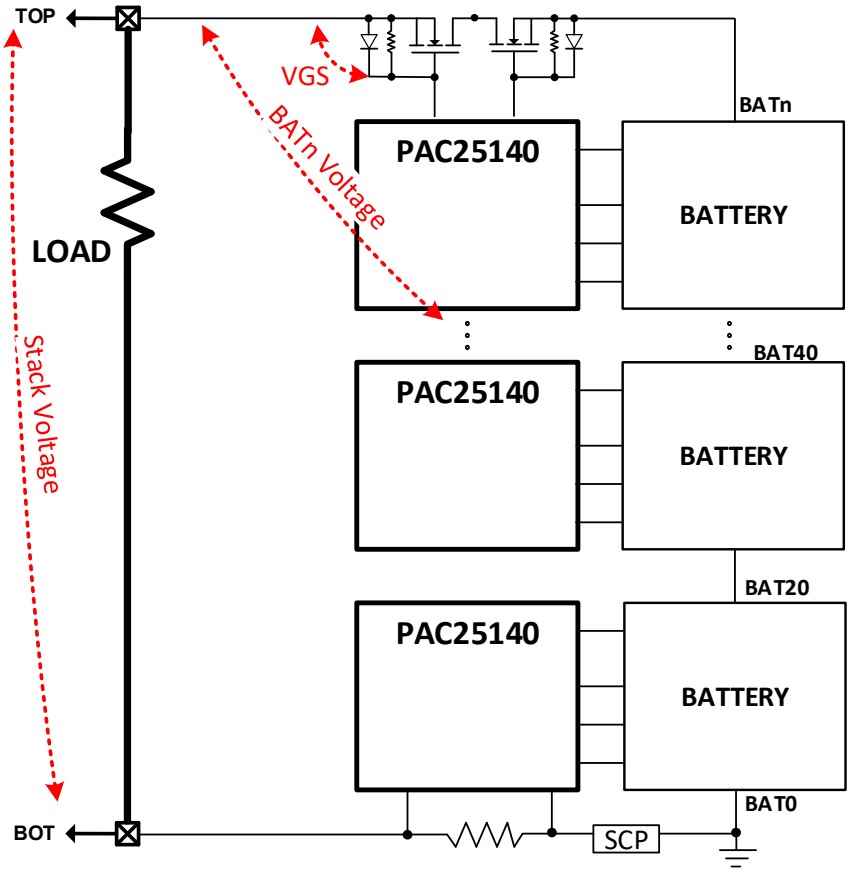


*Figure 3 **Example of BMS Discharge FET Issue***

## 2.4 Protection FET Control with Stacking BMS devices

Voltage protection devices must be added to prevent any absolute maximum voltage violation and IC damage. These devices should be rated to value of the full stack voltage peak expected – including transients. In figure 4, MP1,MP2, MN1 and MN2 should be rated to the full stack voltage plus any peak.

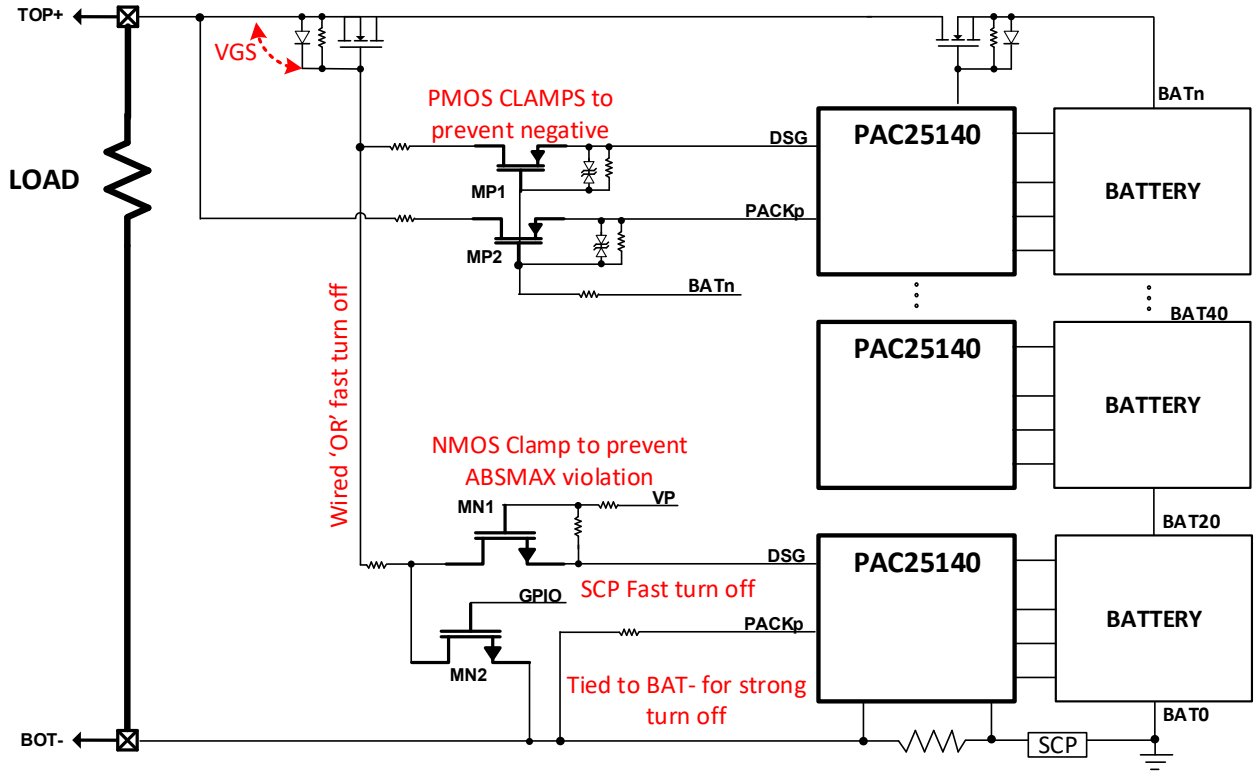


*Figure 4 **Example of BMS Protection FET Solution***

MP1 and MP2 are used to protect the top device gate drive DSG pin.
MN1 is used to protect the bottom device DSG pin.
MN2 is used to speed up the DSG FET turn off when a short or over current is detected.

# 3 Implementation of BMS Stacking

Starting with existing PAC25140 EVK schematic PAC25140EVK , one can modify the EVK circuity to support evaluation of a BMS stacking system.

## 3.1 Top BMS device

For the top BMS IC the charge Pump capacitor should be enlarged from 0.47uF to 10uF to improve the turn on strength. Protection FETs with appropriate rating should be added to limit the voltage, as in figure 4.

## 3.2 Bottom BMS device

For the master on the bottom to control the high-side FETs, configure bottom DSG output as a low side drive control, to pull off the high-side protection FETs, see figure 5 for markup of EVK schematic.

1. Remove PACK+ components, and tie PACK+ pin=GND
2. Charge Pump, remove the components, and tie VCP= VP, keep Charge Pump disabled.

This will allow the bottom DSG to react the same as normal short/over current fault protection. This takes around 350us. For additional speed, a parallel NMOS circuit is added and driven by a bottom GPIO, this takes around 30us. See figure 4 for FET configuration and figure 6 for waveform and timing examples.

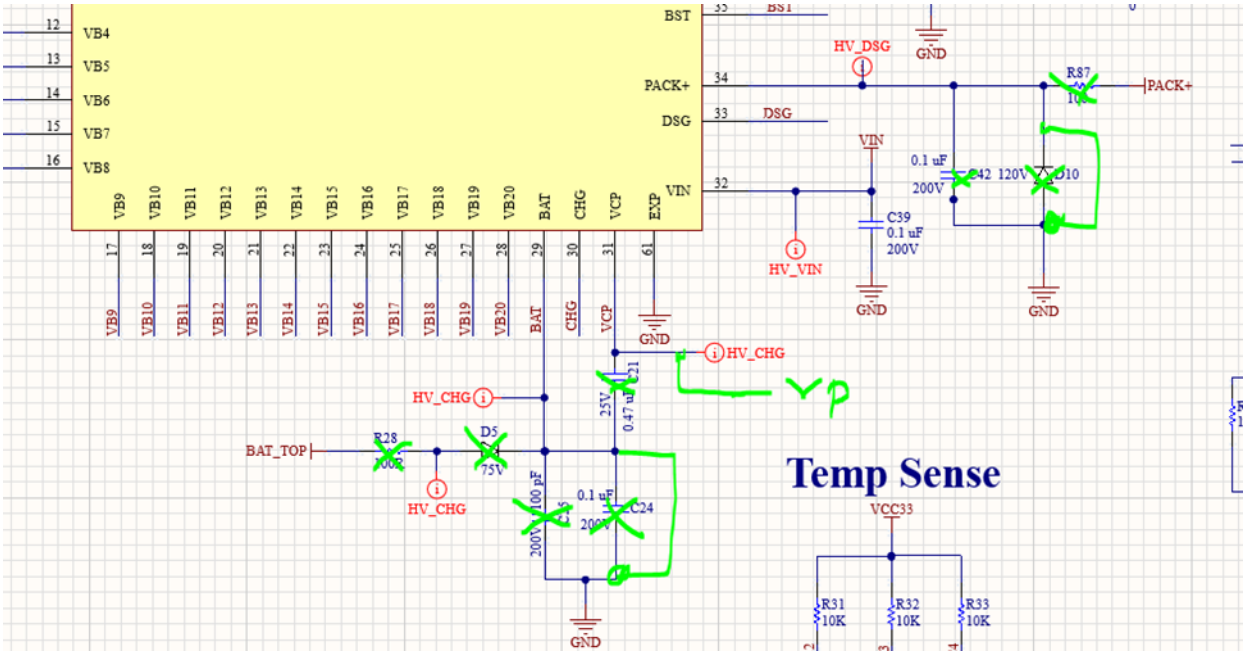


*Figure 5 **Example of PAC25140 EVK Modifications for Master IC on the bottom***

## 3.3 Middle BMS devices

For all middle BMS IC's, the charge pump can be disabled and tied off saving BOM and power since the protection FETs are not needed. See Figure 5.

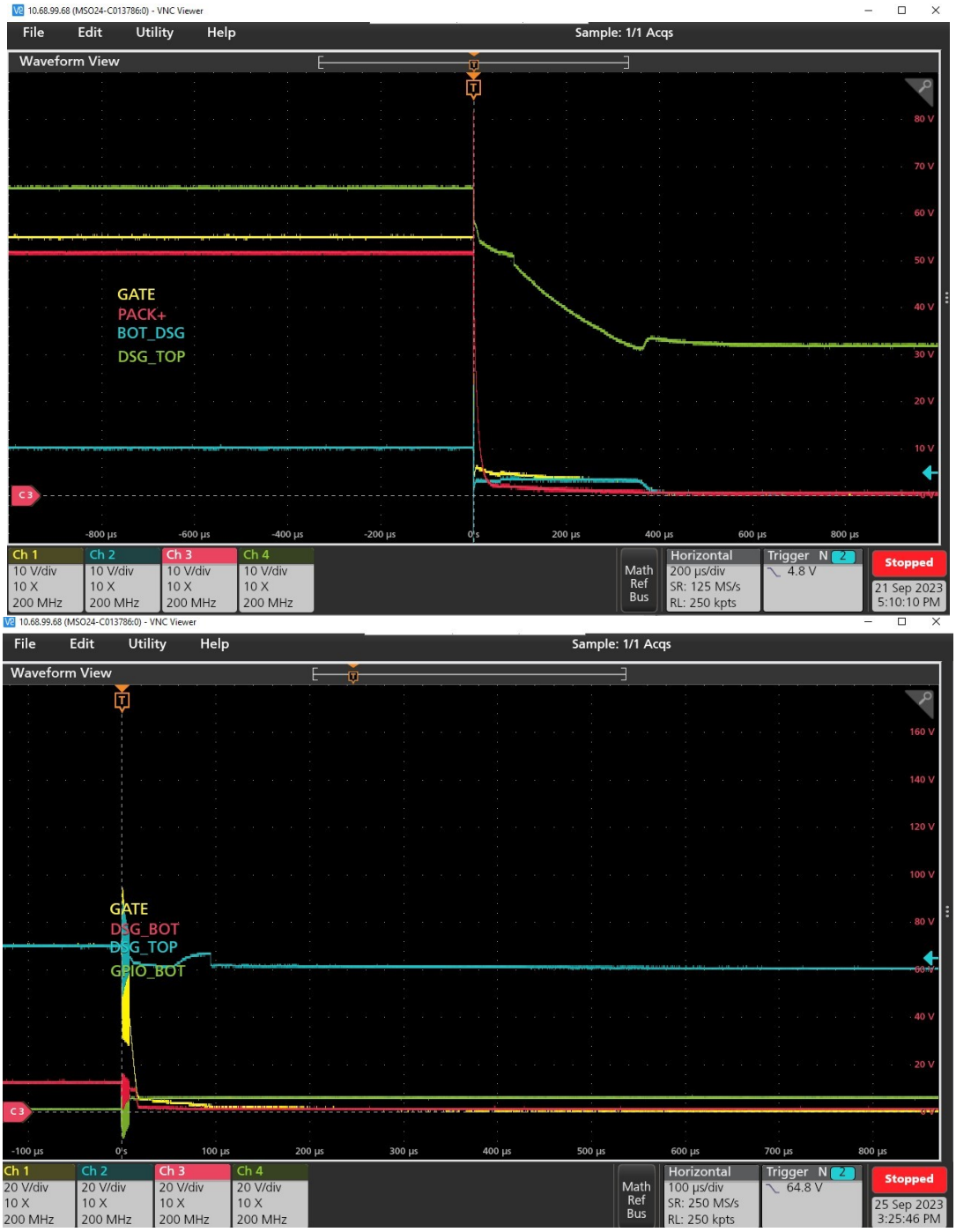


*Figure 6 **Example of turn off waveforms***

*Mater/Bottom turning off without and with GPIO in parallel*

## 3.4 Communication Across the Stack of BMS Devices

Turn on sequence is important to manage. The master/bottom DSG must be turned ON and GPIO control of quick pulldown must be turned off ahead of turning on the Top DSG. If the top DSG is turned-on as soon as bottom DSG pin is turned-on, the NMOS of master/bottom DSG will pull the top DSG and Charge Pump (HVCP) and the top HVCP will set a fault.
The master must control the system sequence and must have a delay to be sure bottom DSG ON reaction is complete to release top DSG driver.

In addition to the I2C isolation, a GPIO fault signal should be used to communicate a fault across all devices in the stack. It can be part of the I2C isolation or dedicated optical isolator.

## 3.5 Lab Setup of a Four Stack of BMS Devices

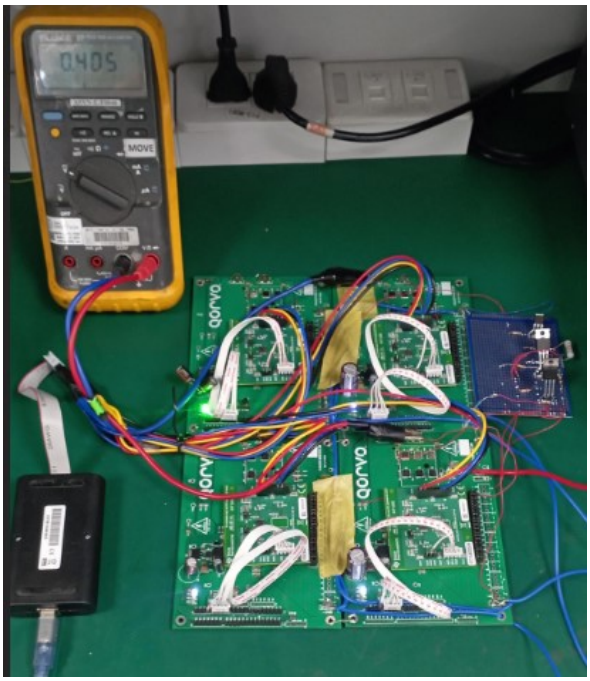

*Figure 7* ***Example concept testing in the lab***

Setup is using two boards of EVK25140 and two boards of EVK22140. Using 4 independent sources (30V) to supply simulated battery packs with resistor divider, communicate via isolated I2C bus.
All four boards work in I2C SLAVE mode and each has a unique address.

GUI is I2C master, GUI is a modified version of the standard EVK's, contact Qorvo for more information. GUI manages the system of all four boards via I2C interface and isolator board.

Firmware is a modification of the standard version on the website

Bottom BMS device measures current via R-shunt, current protection by hardware is in analog and firmware.
Protection FETs added on small PCB and wired into appropriate Top or Bottom EVKs

# 4 REVISION HISTORY

| Revision | DESCRIPTION |
|---|---|
| 1.0 | • Initial Release |
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# 5 LEGAL INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** www.qorvo.com
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