QPE6105A Lighting Reference Design

Reference Design Description

1 Introduction

This document provides information on the QPE6105A Lighting Reference Design.

The QPE6105A is part of a complete solution to deliver design files, application notes and software to enable fast time-to-market for lighting products such as smart LED bulbs.

QPE6105A is a small module that can be mounted on a circular carrier (host) PCB, both typically mounted in a E27 bulb socket. The module has pins on one side for angled (perpendicular) mounting on the carrier PCB.

The module is based on a 2-layer PCB hosting Qorvo's QPG6105 chip in a QFN32 package. The PCB design contains a printed antenna and an option to connect an external antenna to benefit from Qorvo's patented ConcurrentConnect™ Antenna Diversity.

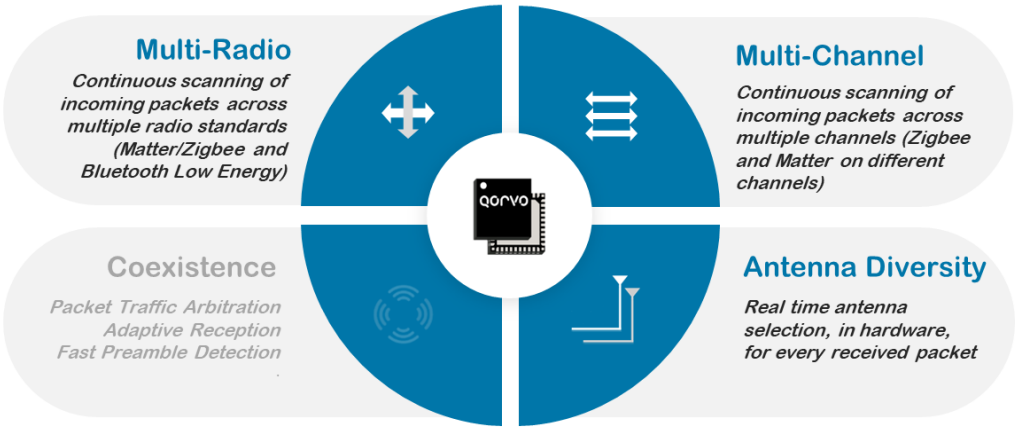
This document covers the following topics:

- Block diagram
- Connector Pinning
- Schematics
- PCB layout, component placement and PCB stack-up
- Bill of Material
- Design guidelines for the RF section
- Information on the interfaces for PWM, ADC, I²C, UART and SPI.

! The information in this document is for reference only. **Any change of the design may impact the performance of the RF system**. As such, it is advised to simulate the results with a suitable RF simulator and/or perform measurements on a prototype version.

Design files for this multi-layer PCB stack are available from Qorvo's website [2]. These can be adapted to other PCB stack-ups.

The **QPG6105** chip is a multi-standard Smart Home communications controller supporting Matter™, Zigbee, Thread, Bluetooth® Low Energy and Bluetooth® Mesh technologies, enabling greater interoperability and scalability. The following ConcurrentConnect™ technologies are supported in the QPG6105 chip. Note that ConcurrentConnect Coexistence is not supported.



The QPE6105A module's small size, 2-layer PCB design, optional antenna diversity and flexibility to integrate in a filament or LED light bulb delivers a versatile, cost-effective and proven solution for lighting applications.

Table of Contents

2 General Information

This chapter shows general information about the QPE6105A Module.
The block diagram is shown in Figure 1 below.

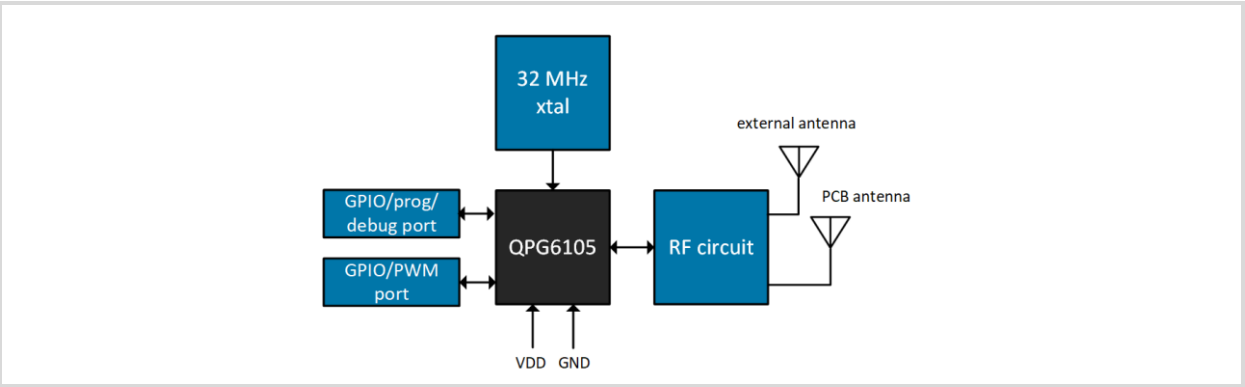


Figure 1: QPE6105A Module Block Diagram

The operating conditions for the QPE6105A are stated below.

Table 1: Operating Conditions

Parameter	Min	Max
Ambient Temperature Range	-40°C	125°C
Power Supply Voltage Range	1.8 V	3.6 V

2.1 QPE6105A Programming Interface

The QPE6105A supports SPI. See section 5.5 for more information.

2.2 Connector Pinning

Figure 2 below shows the pinning for the connectors on the PCB's top side and bottom side. The signals for the primary functions are available on the PCB top side. Signals for programming & debugging are made available on the bottom side. Please note that this configuration allows single sided mounting of a programmed module in a host application by only using the pins of the frontside.

The pitch of the pins is 1.5 mm to facilitate manual soldering of the module in production.

The signal names stated in Figure 2 are also stated in the circuit diagram (see: Figure 3).

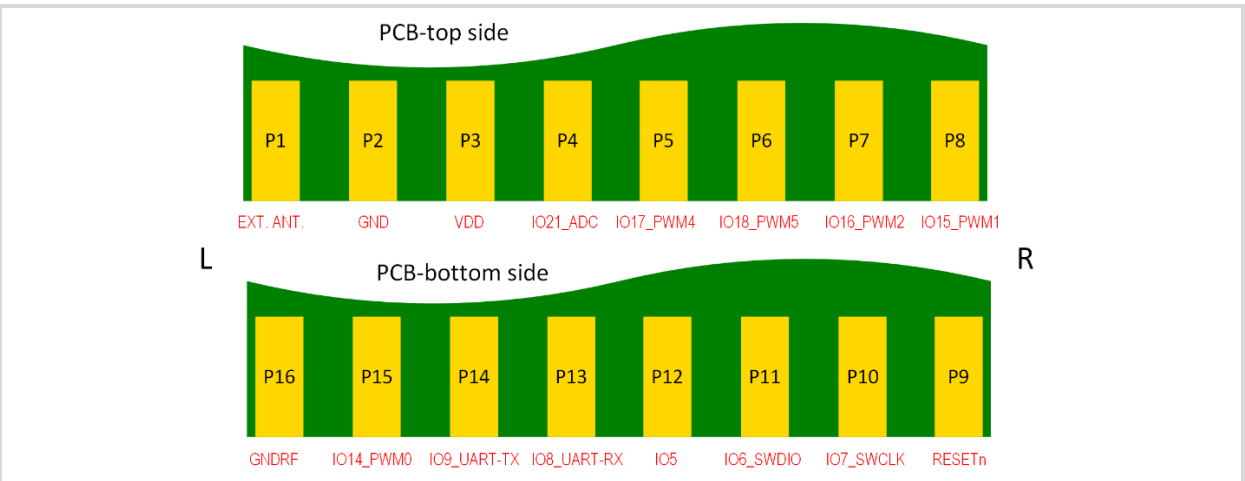


Figure 2: Connector Pinning

3 Reference Design

This chapter contains the schematics, Bill of Material, PCB layout, component placement and PCB stack-up of the QPE6105A Module reference design.

The QPE6105A includes various GPIO interfaces embedding PWM, ADC, GPIO, I²C, SPI, UART and the modules programming interface.

Please see [1] for more information on digital connectivity options.

3.1 Schematics

The overall schematic of the QPE6105A reference design (see Figure 3 below) shows the circuit diagram containing the QPG6105 with the RF passives, and the interfaces for programming and debugging. Note that the signal names are also shown in the PCB connector pinning of Figure 2.

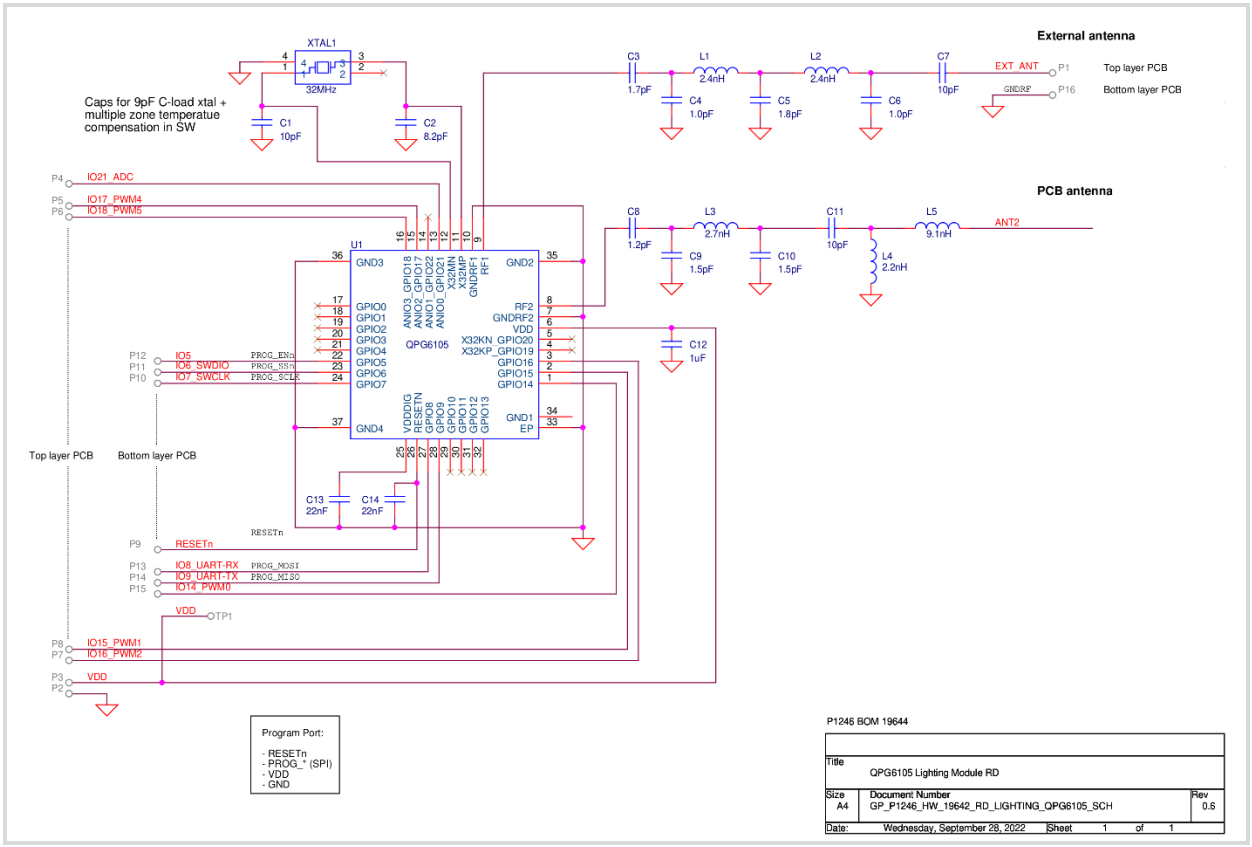


Figure 3: Circuit Diagram

Table 2: Module and Chip Pinning

Connector Pin# (**top** layer)	Signal (module)	QPG6105 Pin name	Connector Pin# (**bottom** layer)	QPG6105 Chip Pin#	Signal
P1	EXT. ANT.	-	P16	GNDRF1	GNDRF
P2	GND	GND	P15	GPIO14	IO14_PWM0
P3	VDD	VDD	P14	GPIO9	IO9_UART-TX
P4	IO21_ADC	ANIO0_GPIO21	P13	GPIO8	IO8_UART-RX
P5	IO17_PWM4	ANIO2_GPIO17	P12	GPIO5	IO5
P6	IO18_PWM5	ANIO3_GPIO18	P11	GPIO6	IO6_SWDIO
P7	IO16_PWM2	GPIO16	P10	GPIO7	IO7_SWCLK
P8	IO15_PWM1	GPIO15	P9	RESETn	RESETn

3.2 Bill of Material

This section provides the Bill of Material as used in this reference design.

! Most of the capacitors and inductors in the RF circuit are "critical items" that shall have the same part number as described in the BOM in this section. The RF performance may be influenced if type or brand of these components are changed. These components are identified by "RF purpose" in the column "Description". Note that some of these components need to be High-Q type.
The 32 MHz crystal used shall conform to its 32 MHz Crystal Procurement Specification [2].

Table 3: Bill of Material for QPG6105 Based Reference Design GP_P1246_BOM_19644 (rev 0.6)

Item Nr	Qty	Value	Part Reference	Tolerance	Type	Voltage (V)	Manufacturer	MPN	Description
1	1	10 pF	C1	±2%	COG/NP0	25	Murata	GJM0335C1E100GB01D	cap ceramic 0201 **RF** GJM **High-Q**
2	1	8.2 pF	C2	±0.05pF	COG/NP0	25	Murata	GJM0335C1E8R2WB01D	cap ceramic 0201 **RF** GJM **High-Q**
3	1	1.7 pF	C3	±0.1pF	COG/NP0	50	Murata	GRM0335C1H1R7BA01D	cap ceramic 0201 **RF** purpose
4	2	1.0 pF	C4 C6	±0.05pF	COG/NP0	50	Murata	GRM0335C1H1R0WA01D	cap ceramic 0201 **RF** purpose
5	1	1.8 pF	C5	±0.1pF	COG/NP0	50	Murata	GRM0335C1H1R8BA01D	cap ceramic 0201 **RF** purpose
6	2	10 pF	C7 C11	5%	COG/NP0	50	Murata	GRM1555C1H100JA01D	cap ceramic 0402 **RF** purpose
7	1	1.2 pF	C8	±0.1pF	COG/NP0	50	Murata	GRM0335C1H1R2BA01D	cap ceramic 0201 **RF** purpose
8	2	1.5 pF	C9 C10	±0.1pF	COG/NP0	50	Murata	GRM0335C1H1R5BA01D	cap ceramic 0201 **RF** purpose
9	1	1 µF	C12	10%	X5R	25	Murata	GRM155R61E105KA12	cap ceramic 0402 general purpose
10	2	22 nF	C13 C14	±20%	X5R	16	Murata	GRM033R61C223ME84D	cap ceramic 0201
11	2	2.4 nH	L1 L2	±0.1nH	inductor	0	Murata	LQP03TN2N4B02p	inductor 0201 **RF** purpose
12	1	2.7 nH	L3	±0.1nH	inductor	0	Murata	LQP03TN2N7B02p	inductor 0201 **RF** purpose
13	1	2.2 nH	L4	+/-0.2nH	inductor	0	Murata	LQW15AN2N2C10D	inductor 0402 **RF** purpose
14	1	9.1 nH	L5	+/-2%	inductor	0	Murata	LQW15AN9N1G00D	inductor 0402 **RF** purpose
15	1	QPG6105	U1	-	RF/PROC-IC	-	Qorvo	QPG6105	QPG6105
16	1	32 MHz	XTAL1	-	XTAL_SMD	0	Procurement Spec	GP_P007_PS_06543_32MHz__2016_Crystal_Procurement_Spec [2]	XTAL 32MHz SMD 2016 CL 9pF -40-125*C
17	1	PCB	0.50	-	PCB	-	PCB manuf.	GP_P1246_HW_19643_RD_LIGHTING_QPG6105_PCB [2]	
18	Ref	Schematic	0.60	-	Schematic	-	Qorvo	GP_P1246_HW_19642_RD_LIGHTING_QPG6105_SCH [2]	

3.3 PCB Layout

This section describes a reference layout for the QPE6105A based on a 2-layer FR4 PCB. The effective dimensions (excluding pin area) are 14.3 mm x 9 mm x 0.84 mm (LxWxH). Its full dimensions (including pin area) are 14.3 mm x 12 mm x 0.84 mm.

Figure 5 through 9 shows the assembly layer for the components, the two copper layers, the PCB's cross section (stack-up) and the PCB dimensions.

This layout can be adapted to the form factor of the customer's design. The recommendations described in chapter 4 should be followed carefully.

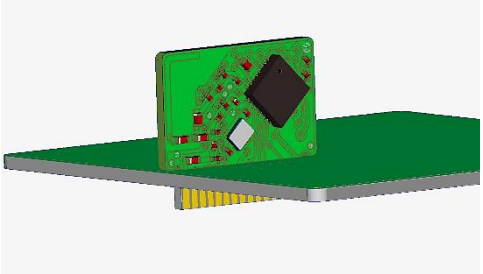


Figure 4: Module Placement in Host

The bottom layer, as shown in Figure 7, should provide a solid, uncut ground under the RF circuit.

The SPI communication lines should be routed carefully. See section 5.5 for more information on SPI.

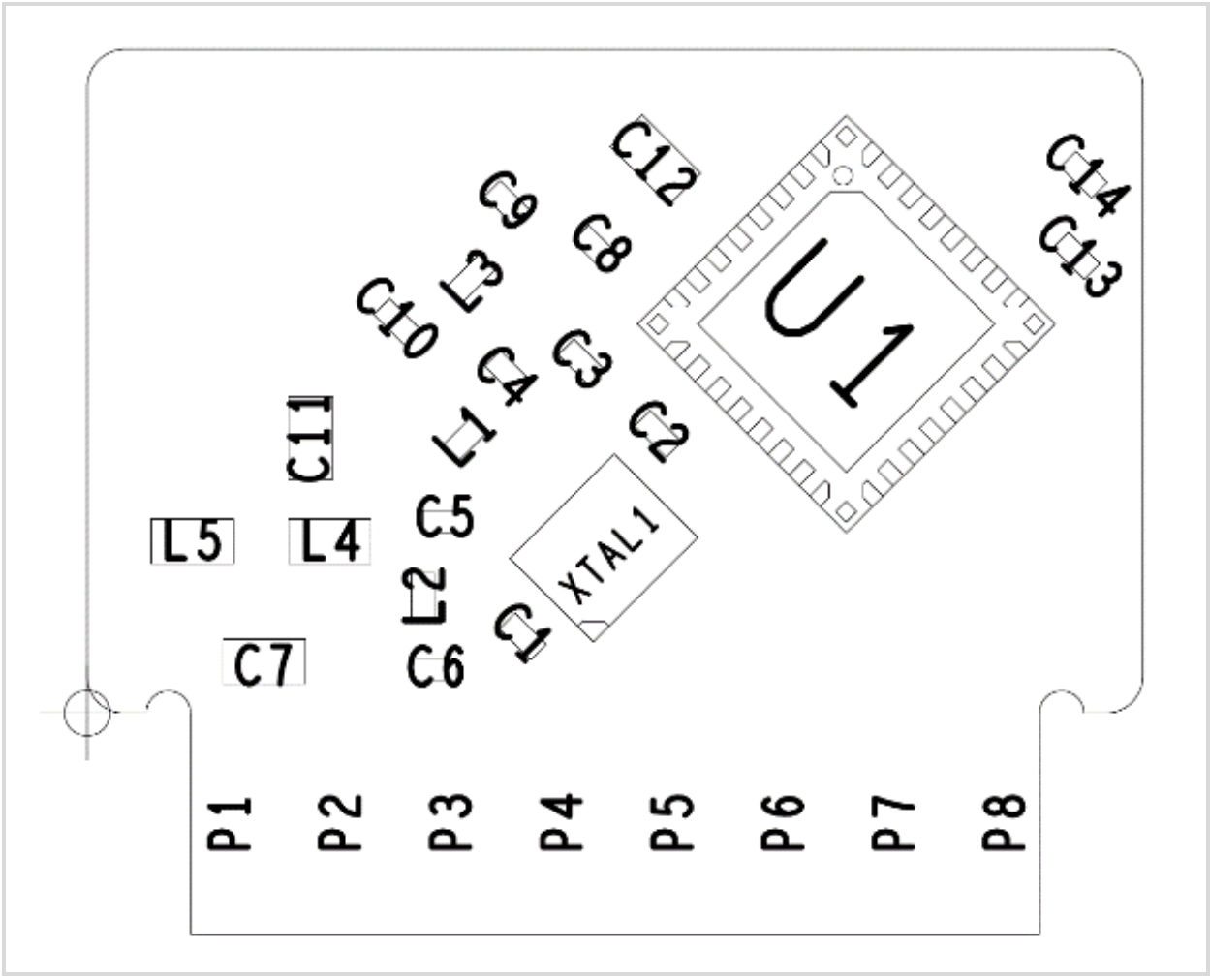


Figure 5: Assembly Top

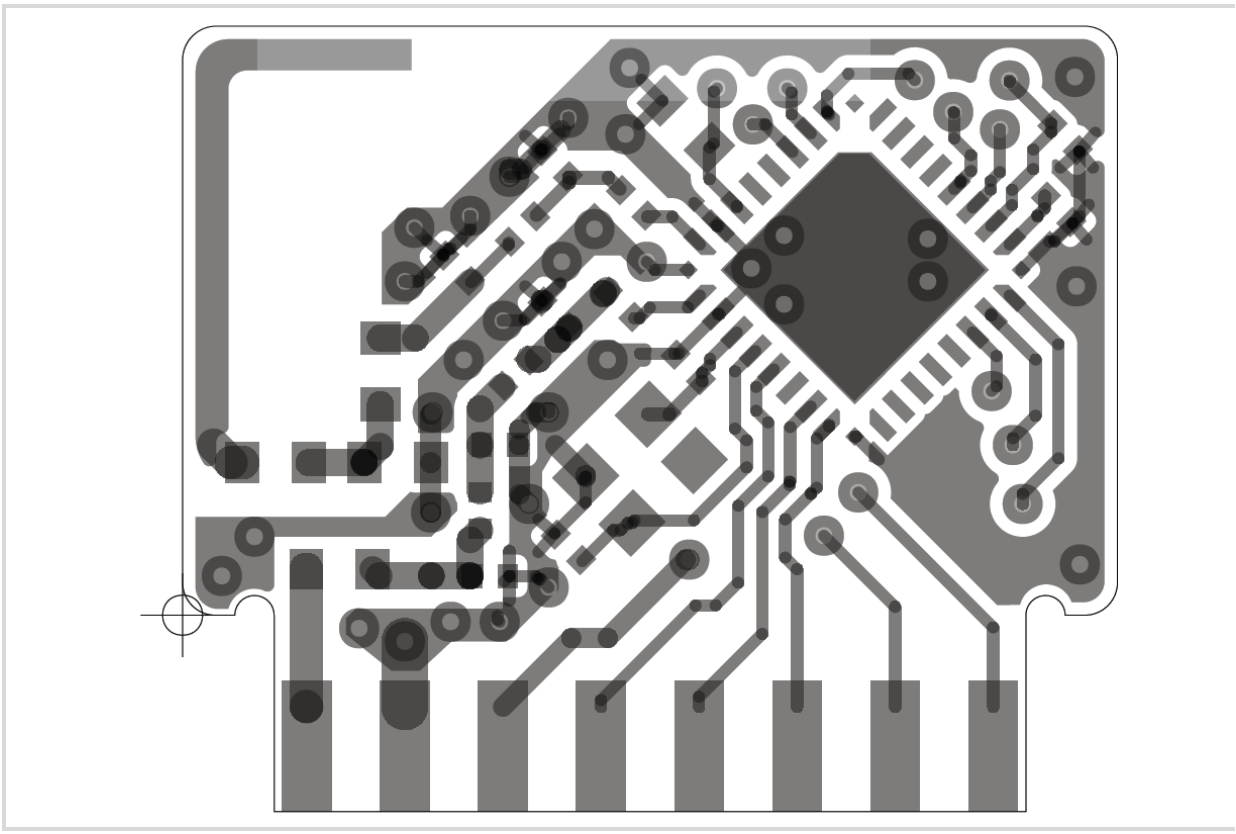


Figure 6: Copper Top Layer

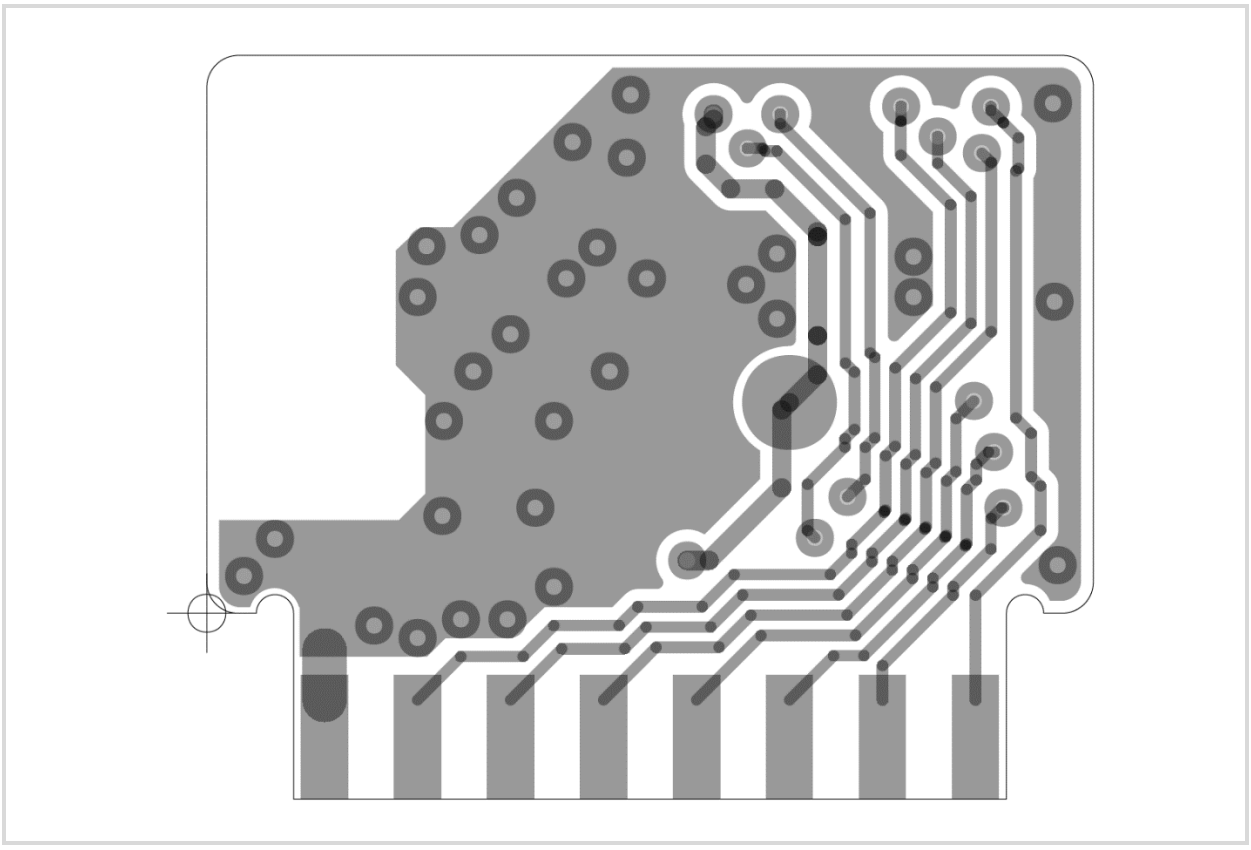


Figure 7: Copper Bottom Layer

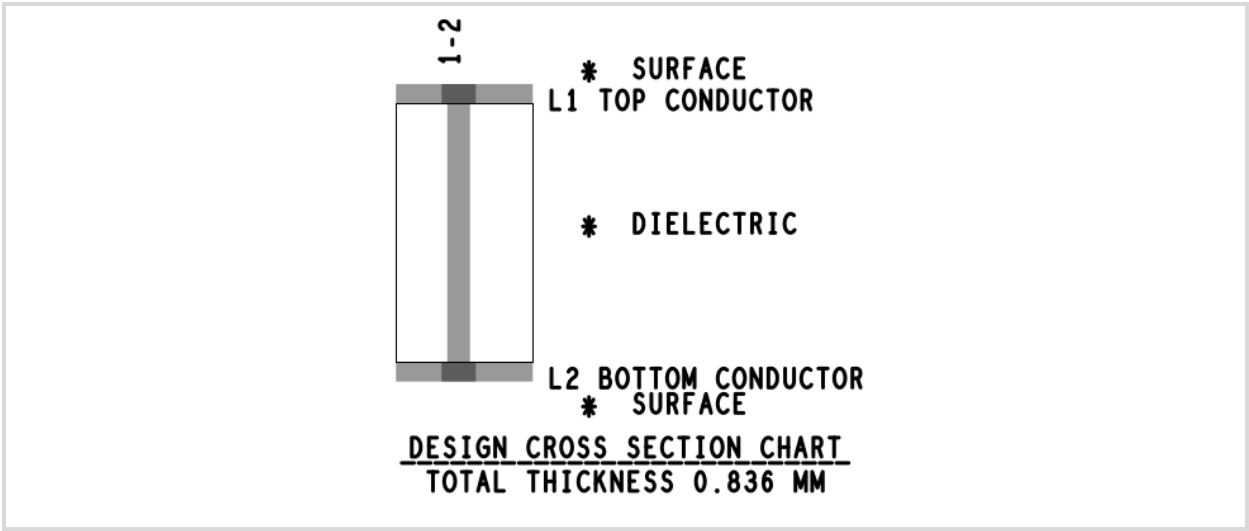


Figure 8: Cross-section

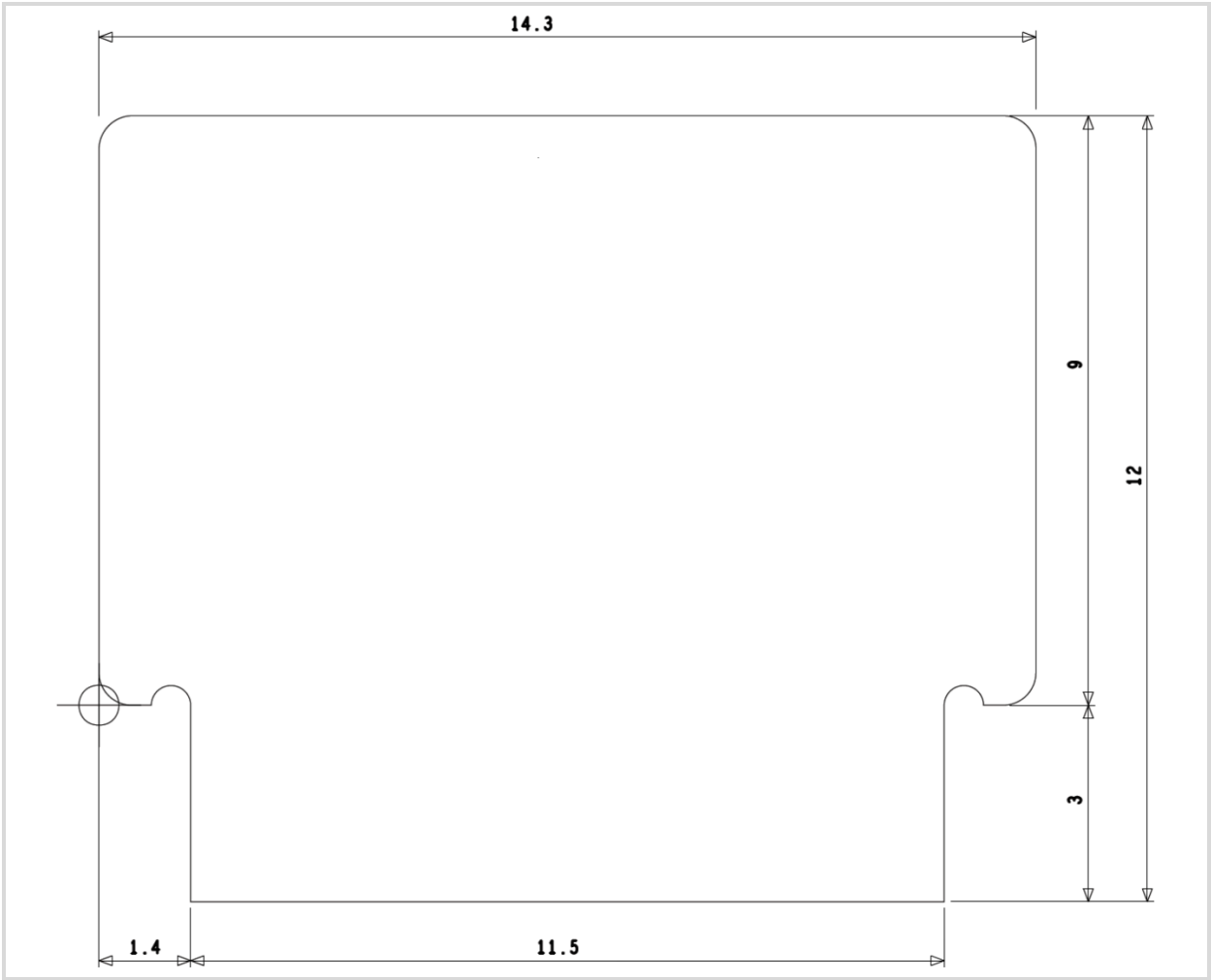


Figure 9: PCB Dimensions

4 RF Design Guidelines

This chapter provides detailed design guidelines for the general RF section, the 2.4 GHz low-pass filter circuits, the antenna matching circuits and the actual antennas.

4.1 RF Section

Figure 10 below shows the schematics of the RF section identifying the main purpose of the various sub-circuits. The upper region is intended for an external antenna, the lower region for the printed PCB antenna. So, C3 .. C7, L1 and L2 are not needed if only the PCB antenna is used. And C8 .. C11 and L3 .. L5 are not needed if only the external antenna is used.

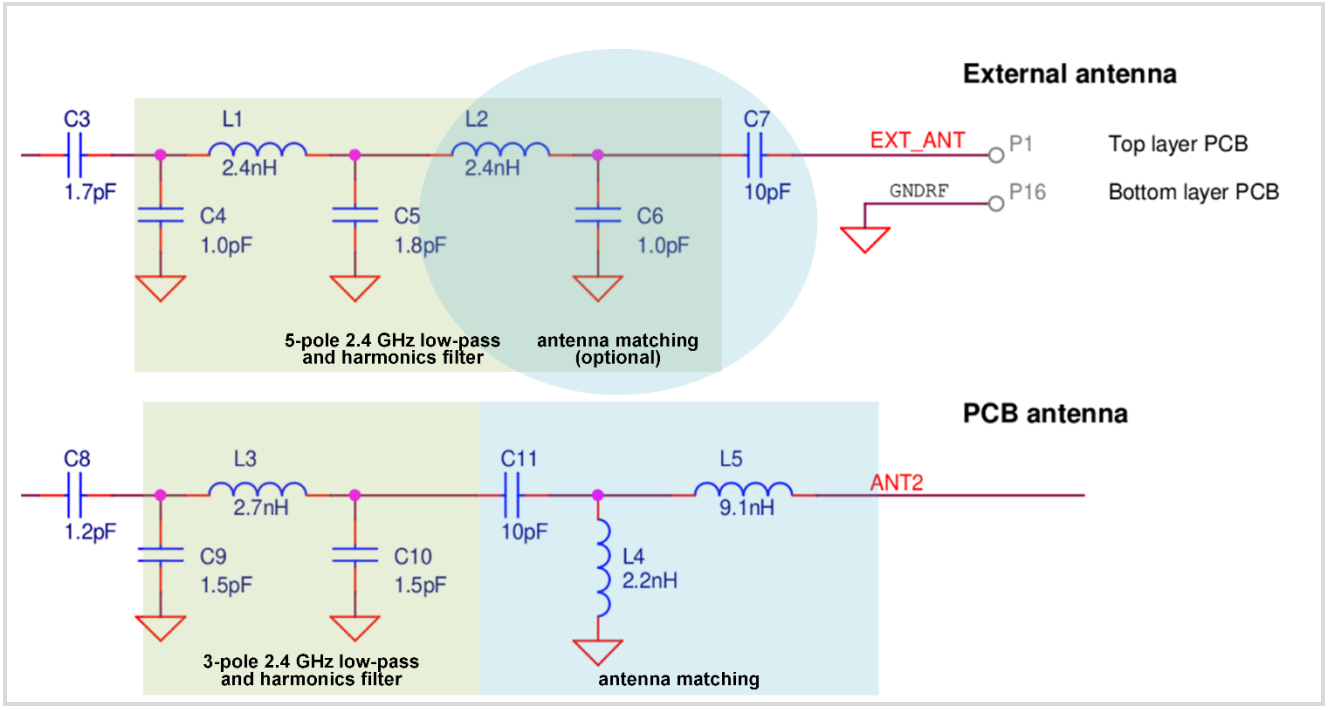


Figure 10: Schematics RF Section

The placement of the various RF circuits is very critical:

- follow the Qorvo reference design
- the 2.4 GHz low-pass filters must be placed close to the RF ports of the QPG6105 chip
- the antenna matching circuits must be close to the antennas.

The current schematic is using a 5-pole low-pass filter for the external antenna, the output impedance is 50 Ohm. In this configuration there are no component positions available for matching of the external antenna. If a matching network for an external antenna is needed, it is possible to use the same configuration as used for the PCB antennas, so a 3-pole low-pass filter making 3 component positions (L2, C6 and C7) available for matching of the external antenna.

Grounding is critical on the RF side of the QPG6105 chip:

- create a solid, uncut copper shape on the footprint of the QPG6105 chip exposed ground pad as done in this reference design.
- connect QPG6105 pin 7 (GNDRF2) and pin 10 (GNDRF1) directly to the exposed ground pad on the top layer of the PCB.
- connect the exposed ground pad with, at least, four vias to reference ground on the bottom layer.
- all power supply decoupling capacitors and the 32 MHz oscillator load capacitors (C1, C2) must have a low impedance ground return path to the exposed die pad of the chip.

4.2 RF Layout

The layout used in this reference design, as shown in detail in Figure 11, has proven to have good RF performance, low spurious emissions and is certifiable in the FCC, ETSI and ARIB (Japan) regulatory domains.

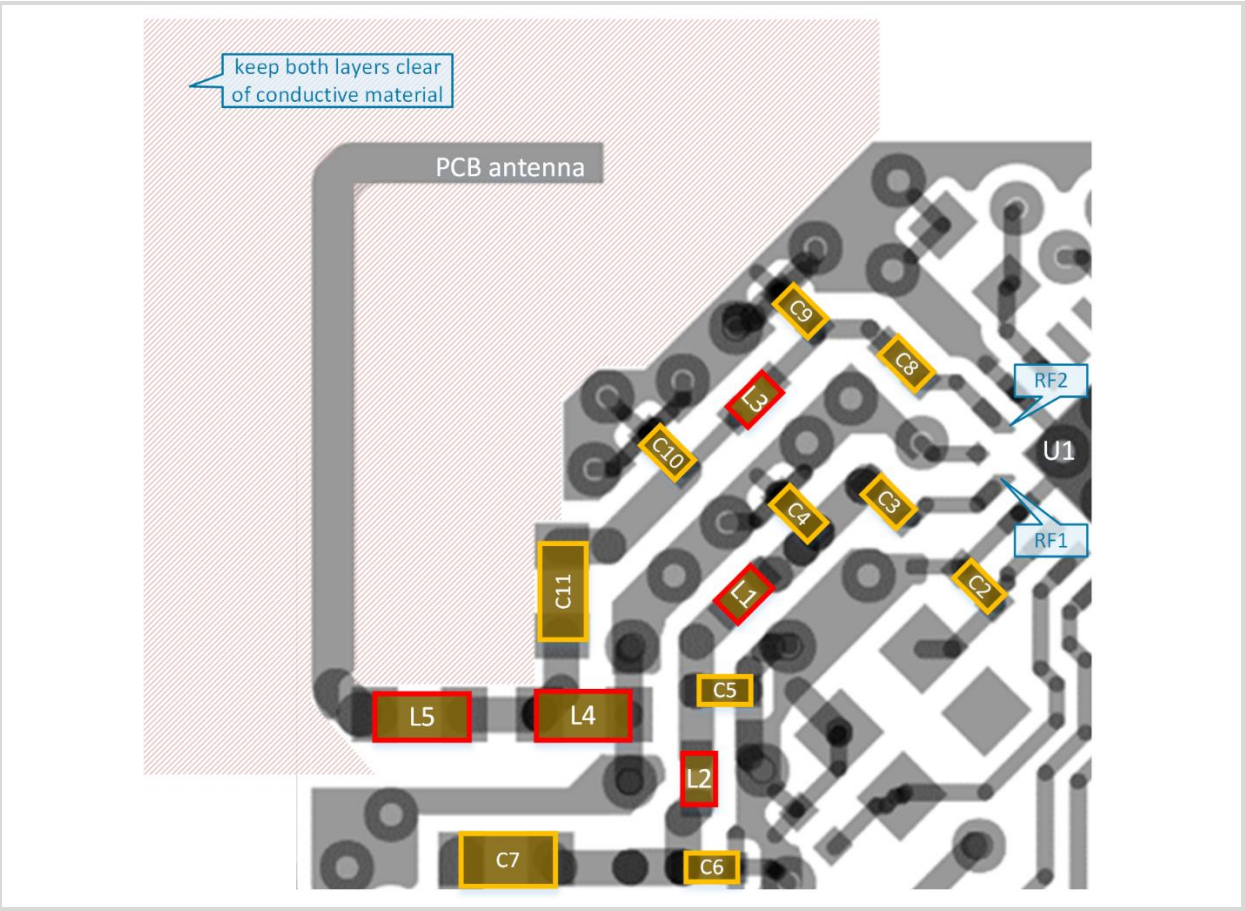


Figure 11: PCB Detail RF Section

The two 2.4 GHz low-pass filter circuits comprises **C4**, **L1**, **C5, L2, C6** for the external antenna, and **C9**, **L3**, **C10** for the PCB antenna. Place these components in the same **π** configuration as shown in Figure 11 above, so in the same arrangement and orientation. Both filters should be placed close to the QPG6105. The RF grounding must have low impedance up to the 4th harmonic (9800 MHz).

All traces from **C10** and **C6** onwards are 50 Ω traces. Trace dimensions will depend on PCB stack-up, please check with a trace impedance calculation tool.

It is important to have a solid ground connection from **C4**, **C5**, **C6**, **C9** and **C10** to the ground plane on the bottom layer and the exposed ground pad of the QPG6105 chip. It is recommended to use vias close to these capacitors per ground connection. Also, a solid uncut ground plane on the bottom layer under the low-pass filter is needed.

The characteristics of the components in the RF section are critical for the performance of the radio:

- use the recommended components (see: Bill of materials: Table 3)
- changing the distance between components or the components' orientation will change the performance of the filter, so use the recommended component placement
- any change in trace length or width in the filter circuits will influence the impedance matching and/or may cause harmonic spurious emissions. Note that the PCB traces between the low-pass filter and the antenna matching circuit are 50 Ω lines and may have any length.

4.3 Antenna Matching

The antenna matching circuit for the **PCB** antenna consists of C11, L4 and L5. The component values can change with the host PCB design or the direct environment of the antenna.

For the antenna matching circuit for the **external** antenna L2, C6 and C7 can be used. Note that these components, together with C4, L1, C5, can also function as a 5-pole LPF.

If there is a need for a change in the antenna matching of the external antenna, then L2, C6 and C7 must be adjusted. C4, L1 and C5 will then function as a 3-pole low-pass filter (LPF) using the same values as shown in the LPF for the PCB antenna. This is shown in the table below.

Table 4: External Antenna Matching Components

Component	Default Value for 5-pole LPF	Default Value for 3-pole LPF with Adjusted Antenna Matching
C4	1.0 pF	1.5 pF
L1	2.4 nH	2.7 nH
C5	1.8 pF	1.5 pF
L2	2.4 nH	to be adjusted
C6	1.0 pF	to be adjusted
C7	10 pF	to be adjusted

It is recommended to check the return loss of the antennas, and corresponding matching networks, with a network analyzer. The design goal is ≥ 10 dB return loss over at least 2400 - 2500 MHz. To prevent yield issues on antenna performance, it is recommended to aim to achieve the 10 dB return loss over a larger bandwidth which will make the design more robust.

When both the external and the PCB antennas are used, the antenna-to-antenna isolation between the two antennas should be ≥ 10 dB to effectively benefit from antenna diversity.

4.4 Antennas

This reference design can use the PCB antenna, an external antenna, or both. Note that for single antenna design the other (non-used) RF port should be left open, so, **not** connected to ground or VDD.

For an **external** antenna several options are available:

a) A simple wire acting as a monopole, consider ~27 mm length to form a ¼ wavelength monopole.
b) The LED string wire (when a LED filament bulb is used).
c) Injection into the mains via a passive coupler.
d) Adding an extra PCB antenna on the host PCB.

Note 1: When option b) or c) is used, the voltage rating of the capacitors in the RF circuit must be revised!
Note 2: Adding an external antenna can also be facilitated by using a small (uFL or MHF4) connector.

When both the PCB antenna and an external antenna are used, try to place the external antenna at an 90° angle relative to the PCB antenna or at maximum possible distance to provide good antenna isolation between both antennas. The design goal for the antenna-to-antenna isolation is ≥ 10 dB.

Qorvo recommends the use of two antennas to benefit from the antenna diversity advantages. Antenna diversity provides ≈ 9 dB more effective range and ≈ 9 dB extra robustness to interference and fading (1% outage). Certain applications can have space constraints to place the two antennas. In this case, consider using only one antenna.

5 Interfacing Guidelines

This chapter contains information on the module's interfaces for PWM, ADC, I²C, UART and SPI.

5.1 Pulse Width Modulation (PWM) Interface

The QPE6105A uses the integrated PWM engine of the QPG6105 chip to generate PWM signals. Five 16-bit PWM outputs are available that can be used to control LED (string) drivers, e.g., warm & cool white and RGB. See also Table 5 below. The modulation parameters can be configured in software.

Note that an 8-bit PWM mode is available for signals that need a higher PWM frequency.

Table 5: PWM Interface Overview

Signal	Connector Pin#	QPG6105 Chip Pin#	PCB pin location
IO14_PWM0	P15	1	bottom side
IO15_PWM1	P8	2	top side
IO16_PWM2	P7	3	top side
IO17_PWM4	P5	15	top side
IO18_PWM5	P6	16	top side

5.2 Analog-to-Digital Converter (ADC) Interface

The QPE6105A uses the integrated 10/12 bit ADC module of the QPG6105 chip to monitor an analog signal.

This signal can be an **external** analog signal (IO21_ADC) supplied via ANIO pin P4. The ADC can also be configured by software to monitor the power supply level and/or temperature **internally**; no external components are then required. In this case the power supply level and temperature are measured independent from the signal available at pin P4.

The ADC runs on 4 MHz clock speed. A total of 16 cycles (4 µs) are needed to obtain a conversion result.

Please refer to the QPG6105 Data Sheet [1]; sections "ADC Characteristics" and "Battery / Temperature Monitor Characteristics" for the ADC's accuracy, range and other data.

5.3 I²C Interface

The Inter-Integrated Circuit (I²C) Master interface is a synchronous, single-ended, serial communication specification that is supported in the QPE6105A. This interface can be used for interfacing with additional peripheral I²C devices or for current control of LED drivers (instead of using the PWM interface).

For this purpose, the signals shown in Table 6 below shall be made available for these use cases. See also Figure 2 (Connector Pinning) and Figure 3 (Circuit Diagram).

Table 6: Signals for I²C

Signal	Connector Pin#		QPG6105 Chip Pin#	Notes
SDA	P5		15	serial data line
SCL	P6		16	serial clock line

For more details on I²C of the QPE6105A, please refer to [1] section "I²C Master".

5.4 UART Interface

The Universal Synchronous Receiver-Transmitter (UART) interface is an asynchronous serial communication interface specification that is supported in the QPE6105A.

This interface can be used for interfacing with additional peripheral devices, for terminal logging during (software) development, for RF validation and RF certification testing.
For this purpose, the signals shown in Table 7 below shall be made available for these use cases. See also Figure 2 (Connector Pinning) and Figure 3 (Circuit Diagram).

Table 7: Signals for UART Interfacing

Signal	Connector Pin#	QPG6105 Chip Pin#	Notes
UART-TX	P14	28	serial data line
UART-RX	P13	27	serial clock line

For more details on UART interfacing of the QPE6105A, please refer to [1] section “UARTs”.

5.5 SPI Interface

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface specification that is supported in the QPE6105A. The primary programming interface for programming the Flash memory in the QPG6105 chip is its SPI Slave interface. For this purpose, the signals shown in Table 8 are available on the module’s IO pins. See also Figure 2 (Connector Pinning) and Figure 3 (Circuit Diagram).

Table 8: Signals for SPI Programming

Signal	Connector Pin#	QPG6105 Chip Pin#	Notes
PROG_ENn	P12	22	low (stable) enables programming mode at startup/reset
SSPI_SSN	P11	23	Slave select signal
SSPI_SCLK	P10	24	clock provided by the programmer
SSPI_MOSI	P13	26	data from programmer to device
SSPI_MISO	P14	28	data from device to programmer

For more details on SPI of the QPE6105A, please refer to [1] section “SPI Programming Interface”.

6 Decoupling Recommendations

The module's design contains a VDD decoupling capacitor (C12). The VDDDIG power supply output of the QPG6105 chip (pin 25) is decoupled to ground with C13. The RESETn line has a 22 nF decoupling capacitor (C14) that satisfies external POR trigger conditions for a VDD rise time[1] up to 500 µs. Please refer to [1] for details on the POR circuit of the QPG6105. For larger VDD rise times, Figure 12 provides an overview of recommended capacitances. Segger drag & drop programming is not currently supported for RESETn capacitances larger than 220 nF.

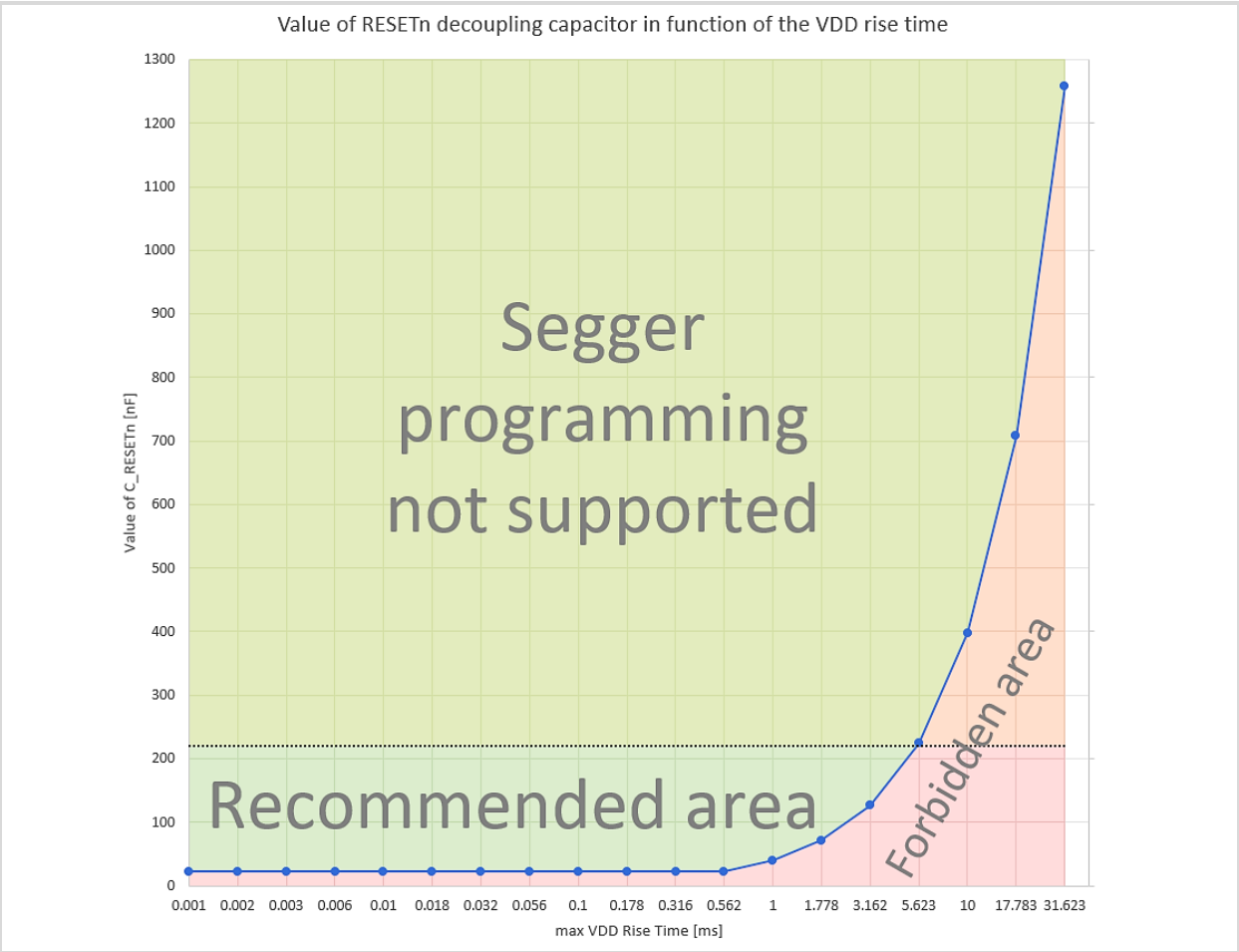


Figure 12: Capacitance of RESETn Decoupling Capacitor vs max. VDD Rise Time

6.1 Decoupling Capacitors Layout Recommendations

- place the VDD decoupling capacitor (C12) as close as possible to VDD (pin 6) of the QPG6105 chip
- connect the ground of C12 directly to the QPG6105 ground using pin 7 (GNDRF2)
- place the VDDDIG decoupling capacitor (C13) as close as possible to VDDDIG (pin 25) of the QPG6105 chip
- connect the ground of the VDDDIG decoupling capacitor (C13) directly to the QPG6105 ground corner (pin 37).

[1] The time required for VDD (of 3.3 V) to go from 330 mV to 2.97 V (i.e., from 10% to 90% of VDD).

References

[1] Qorvo **QPG6105 Data Sheet**; Qorvo document GP_P008_DS_17366, available at QPG6105 webpage: https://www.qorvo.com/products/p/QPG6105

[2] Qorvo **QPE6105A Lighting Reference Design Package**; Qorvo document GP_P1246_HW_19781, available at https://www.qorvo.com/products/p/QPG6105#documents

Abbreviations

ARIB	Association of Radio Industries and Businesses (Japan)
BOM	Bill Of Materials
ETSI	European Telecommunication Standardization Institute (EU)
FCC	Federal Communications Commission (USA)
FR4	Flame Retardant grade 4 (fiberglass reinforced epoxy laminates)
GND	Ground
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
I/O	Input/Output
LED	Light Emitting Diode
MCU	Micro Controller Unit
PCB	Printed Circuit Board
POR	Power On Reset
RF	Radio Frequency
RX	Receive(r)
SPI	Serial Peripheral Interface
TX	Transmit(ter)
UART	Universal Asynchronous Receiver and Transmitter
VDD	Voltage Drain Drain (positive voltage supply)

Important Notice

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Document History

Version	Date	Section	Changes
1.0	Dec 20, 2022		Initial version.
1.1	Dec 21, 2022	3.2	Update of High-Q type description.
1.2	Feb 6, 2023	6	Segger drag & drop programming text updated.
		all	New file name issued.
1.3	Mar 17, 2023	all	Bad references corrected. Minor format updates.
1.4	Apr 14, 2023	1	Updated ConcurrentConnect image.
1.5	Apr 17, 2023	1	Updated ConcurrentConnect information.
1.6	May 2, 2023	2.1, 5.3, 5.4, 5.5	Revised text avoiding “program port”.
1.7	May 11, 2023	all	Released public version.
		2.1	Removed text about UART software support.
		5.3	Revised text w.r.t. “programming”.
		5.4	Reference to data sheet section updated. Added reference to Fig. 3 and Fig. 4.
		References	References updated for web pages.
		last page	Page size corrected.