APPLICATION NOTE

SiC E1B Modules Technical Overview

Scope

Qorvo has pioneered the introduction of SiC JFET based cascodes (SiC FET) with gate drive compatibility to Si MOSFETs, IGBTs, and SiC MOSFETs, based on the 5V threshold voltage and wide gate operating range of +/-25V. These devices are inherently very fast switching, with excellent body diode characteristics.

Qorvo has combined the advantageous SiC JFET based power device with an industry standard power module package, E1B, to further enhance power density, efficiency, cost-effectiveness, and ease of use for industrial power systems.

This application note introduces Qorvo's latest E1B power module packages with two topology configurations (half-bridge and full bridge). To fully exploit the fast-switching capability of SiC devices, critical design guidelines must be followed to ensure success. This application note covers the static and dynamic performance of Qorvo SiC E1B modules and practical design tips to implement the fast-switching capability of Qorvo's SiC E1B module successfully and reliably.

IMPORTANT: Snubbers are strongly recommended for SiC E1B modules due to their intrinsic fast-switching speed. Also, snubber greatly reduces turn-off switching loss making SiC E1B modules extremely attractive in ZVS (zero voltage turn-on) soft-switching applications such as phase-shifted full-bridge (PSFB), LLC, etc.

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

This application note also provides resource links to simulation models, assembly guidelines, thermal characteristics, reliability, and qualification documents.

Resource and reference

[1] SiC E1B Modules Technical Overview

[2] SiC E1B Modules Mounting Guideline

[3] SiC FET & Module User Guide

[4] SiC E1B Modules DPT EVB User Guide

[5] Qorvo SiC Module Link: SiC Modules - Qorvo

[6] Web based loss calculator for part selection: https://www.qorvo.com/design-hub/design-tools/interactive/fet-jet-calculator

[7] Qorvo SiC power solution central hub: https://www.qorvo.com/innovation/power-solutions/sic-power

[8] More design tips: https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips

[9] Origins of SiC FETs and Their Evolution Towards the Perfect Switch

Contents

Product introduction

SiC power semiconductors have great potential to improve power density, efficiency, and cost-effectiveness for overall system design compared to Si. The core advantages of SiC are high voltage blocking capability, low conduction loss, low switching loss, and high thermal conductivity. These advantages combine to provide significant improvements in efficiency and power density.

First, system power density is increased because SiC allows high switching frequency (low switching loss) which enables smaller passive components (capacitors, inductors, transformers, and EMI filters, etc.).

In the meantime, increasing power density also means increased heat concentration. Qorvo's SiC FET technology provides excellent efficiency (low conduction loss and low switching loss) and thermal performance (low thermal resistance from junction to case) to greatly ease thermal management.

Thanks to the aforementioned advantages, Qorvo's SiC E1B module provides improved efficiency and performance in industrial applications such as renewable energy systems, industrial power supplies, energy storage systems, and EV charging stations, etc. **Figure 1** shows a typical application in solar system.

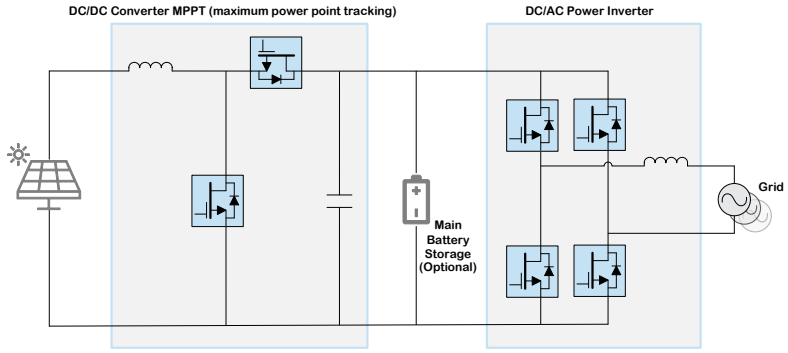
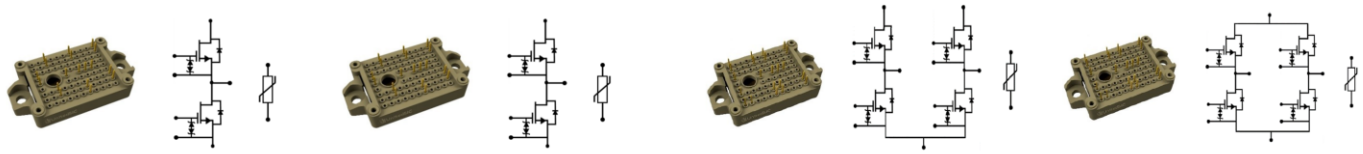


Figure 1. Qorvo SiC E1B module in solar systems (half-bridge for a boost converter, full-bridge for a single phase inverter).

Qorvo SiC E1B module

Qorvo delivers low on-resistance (R_{DSON}) in an industry standard (pin compatible) E1B power module package as shown in **Figure 2**. Qorvo's E1B power module provides two topology options: half-bridge (HB) configuration and full-bridge (FB) configuration. Both HB and FB are the backbone of many popular power conversion topologies.

UHB50SC12E1BC3N **UHB100SC12E1BC3N** **UFB15C12E1BC3N** **UFB25SC12E1BC3N**



1200V HALF-BRIDGE Cascode FET Power Modules			
Part #	RDS(on) Typ 25C	Max Continuous Drain Current	Max Continuous Drain Current
UHB50SC12E1BC3N	19mohm	50A (Tc = 50C)	69A (Tc = 25C)
UHB100SC12E1BC3N	9.4mohm	100A (Tc < 85C)	100A (Tc = 25C)

1200V HALF-BRIDGE Cascode FET Power Modules			
Part #	RDS(on) Typ 25C	Max Continuous Drain Current	Max Continuous Drain Current
UFB15C12E1BC3N	70mohm	15A (Tc = 105C)	24A (Tc = 25C)
UFB25SC12E1BC3N	35mohm	25A (Tc = 90C)	36A (Tc = 25C)

Figure 2. Qorvo 1200V SiC E1B half-bridge and full-bridge module RDS(on) and current rating.

Qorvo's 4 E1B modules shown in **Figure 2** are all 1200V rated. The half-bridge module has two R_{DSON} classes.
UHB50SC12E1BC3N has typical R_{DSON} of 19mOhm at 25C junction temperature and 69A rated current at 25C case temperature.
UHB100SC12E1BC3N has typical R_{DSON} of 9.4mOhm at 25C junction temperature and 100A rated current at 25C case temperature.
The full-bridge module has two R_{DSON} classes.
UFB15C12E1BC3N has typical R_{DSON} of 70mOhm at 25C junction temperature and 24A rated current at 25C case temperature.
UFB25SC12E1BC3N has typical R_{DSON} of 35mOhm at 25C junction temperature and 36A rated current at 25C case temperature.

Qorvo SiC E1B module features and benefits

Table 1 summarizes features and benefits of Qorvo SiC E1B module.

Static characteristics assessment in this section includes R_{DSON}, body diode VF, gate charge Qg, output capacitance Coss, Rthjc (thermal resistance from junction to case). Dynamic characteristics include switching loss for hard-switching and soft-switching applications. The 1200V 100A rated half-bridge module (UHB100SC12E1BC3N) is used as an example to assess static characteristics and dynamic characteristics.

QORVO FEATURES	QORVO BENEFITS
Low R_{DSON}	Low conduction loss
Low body diode VF	Low conduction loss (3rd quadrant, dead time)
Low Qg	Low Gate drive loss
Low Coss	Low switching loss and low V_{DS} transition time
Low Rthjc	Low Tj and better lifetime
Extremely low turn-off loss	Ideal for ZVS application (no turn-on loss)
2X power cycling vs SiC MOSFET	Longer lifetime

Table 1. Qorvo SiC E1B module features and benefits.

Static characteristics

Qorvo's advanced SiC die technology enables superior electrical and thermal performance in the market as shown in **Table 2**. The two parts are comparable in R_{DSON} at 125C with same voltage and current rating.

SPECS	QORVO	SiC MOSFET VENDOR A
Part number	UHB100SC12E1BC3N	X
ID	100 A	100 A
VDS (max)	1200 V	1200 V
V_{TH}	5 V	2.5 V
R_{DSON} (25C)	9.4 mΩ	10.5 mΩ
R_{DSON} (125C)	15 mΩ	14.1 mΩ
Body diode VF (100A, 25C)	1.63 V	5.1 V
Body diode VF (100A, 150C)	2.1 V	4.7 V
Qg (VGS -5V to 15V; VDS 800V)	170 nC	324 nC
Eoss (VDS 800V)	154 uJ	147 uJ
Rth,jh	0.4 °C/W (lab test)	0.428 °C/W

Table 2. Qorvo E1B module (1200V, 100A, half-bridge) key parameters v.s. a SiC MOSFET pin compatible part (Vendor A, X).

Qorvo SiC E1B module has higher V_{TH} to provide better immunity to gate false triggering. Qorvo has much lower body diode VF to provide lower loss during normal 3rd quadrant conduction and dead time conduction loss. Qorvo has much lower Gate charge to reduce Gate drive loss for high switching frequency applications. Qorvo has much lower thermal resistance to enable lower junction temperature and longer lifetime.

Low R_{DSON}: Qorvo E1B modules are based on SiC JFET technology to enable much lower R_{DSON} per unit area (R_{dsA}). A cascode structure (SiC FET) is used to enable normally-off operation as shown in **Figure 3**. For typical planar SiC MOSFET the channel resistance makes a significant part (>40% for 1200V device) of total R_{DSON} of the device. That channel resistance of a planar SiC MOSFET is replaced by a low voltage Si MOSFET (<10% of total R_{DSON} for 750V device) in Qorvo SiC FET structure. For more technical details, please refer to this white paper: Origins of SiC FETs and Their Evolution Towards the Perfect Switch.

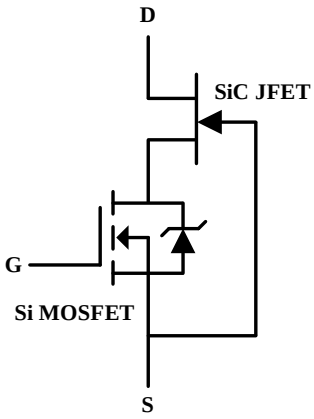


Figure 3. Qorvo SiC FET cascode structure combining benefits of Si and SiC.

Low body diode VF: SiC MOSFET body diode has much higher VF than Si MOSFET due to its higher bandgap since knee voltage of PN diode scales with the energy bandgap. Qorvo SiC FET technology uses cascode structure to combine the benefits of Si and SiC. In a cascode structure the body diode VF has two components, Si MOSFET V_{SD} and SiC JFET V_{SD}. The Si MOSFET V_{SD} is about 0.7V. Once Si MOSFET is conducting, its V_{SD} bias SiC JFET gate positively and SiC JFET (normally-on) channel turns on. In other words, synchronous rectification is automatically enabled for a cascode structure in 3rd quadrant operation.

Low Qg: The Gate charge of Qorvo SiC FET is determined by the low voltage Si MOSFET as shown in **Figure 4**. The low voltage Si MOSFET is designed with low Qg with a 5V typical threshold voltage (V_{TH}). Furthermore, Qorvo SiC FET can fully turn on at 10V gate bias as shown by the left chart in **Figure 4**. At 10V gate bias, Qg is further reduced to 128nC compared to 170nC at 15V gate bias.

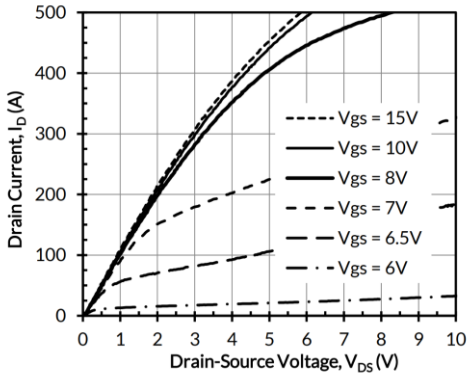


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

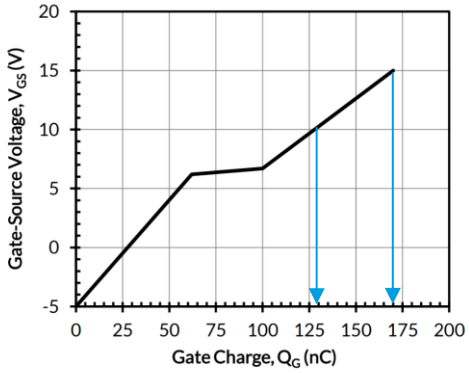


Figure 8. Typical gate charge at V_{DS} = 800V and I_D = 100A

Figure 4. Qorvo SiC E1B module (UHB100SC12E1BC3N) datasheet I-V curve (left) and gate charge curve (right).

Low Coss: Qorvo SiC E1B module has very low R_{dsA} (on-resistance per unit area) to enable smaller chip size for a given R_{DSON}. Therefore, low Coss(er) (energy related device output capacitance) and low Coss(tr) (time and charge related device output capacitance) is achieved to provide fast VDS transition and low switching loss.

Low Rthjc: Qorvo SiC E1B module applies silver sinter die-attach to provide 6 times better thermal conductivity of the interface comparing to most solder materials, resulting an equivalent or even lower junction-to-case thermal resistance with a smaller die size. Low Rthjc helps to keep junction temperature rise low and reliability high.

Dynamic characteristics

Dynamic characteristic benchmark in this section focuses on switching loss performance for both hard-switching and soft-switching conditions to demonstrate two key points:

- Qorvo SiC E1B modules provide low switching loss. Especially, the extremely low turn-off switching loss is very attractive to ZVS (zero-voltage-turn-on) high-switching-frequency applications such as phase-shifted full-bridge (PSFB), LLC, etc.
- Using snubber correctly can greatly reduce switching loss while providing waveform control, especially for ZVS applications.

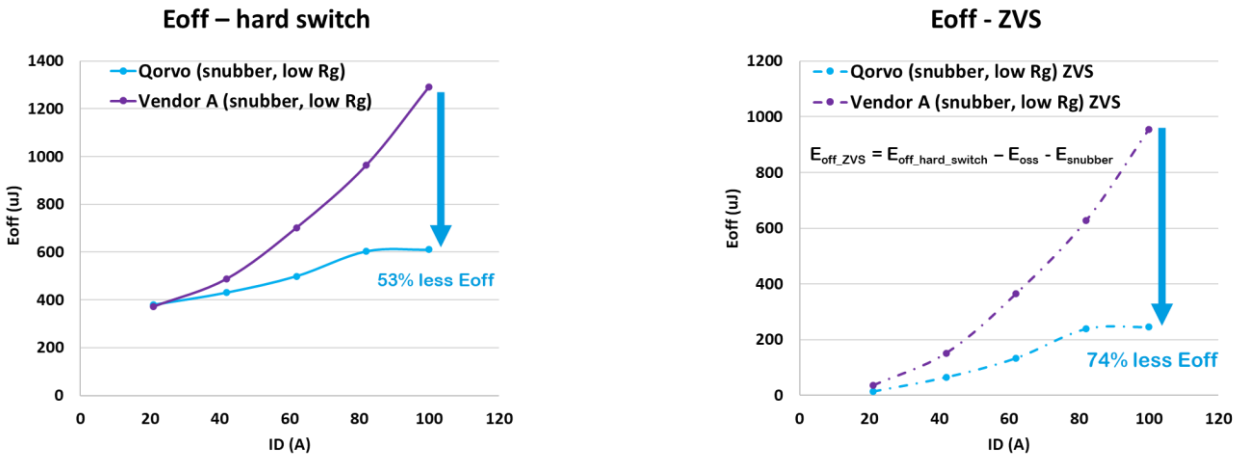


Figure 5. Qorvo SiC E1B module (UHB100SC12E1BC3N) switching loss benchmark with SiC MOSFET with recommended snubber.

Snubber configuration

A typical RC snubber configuration in a half-bridge is shown in **Figure 6** for hard-switching and ZVS soft-switching applications.

Bus snubber consists of decoupling capacitor (Cd) and resistor (Rd) between the fast-switching half-bridge and DC LINK bulk capacitor. Cd should be placed as close as possible to the half-bridge to minimize power loop stray inductance. This enables faster di/dt (current slew rate) while containing VDS overshoot spikes. It is a much more efficient way than simply increasing Rg (gate resistor) to contain VDS overshoot spikes. Cd is typically 0.1 uF. Rd is typically 1 Ω to 4.7 Ω. Actual number depends on PCB design.

Device snubber consists of capacitor (Cs) and resistor (Rs) across device drain-to-source terminals. Cs is typically 2-3 times the device Coss(er) (energy equivalent output capacitance). Rs is typically 1 Ω to 4.7 Ω. Cs helps to control voltage slew rate (dv/dt) and VDS overshoot spikes. Rs helps to damp the VDS ringing.
For hard-switching the device snubber resistor Rs is placed near device drain-to-source to provide best damping effects. **Please note that snubber resistor power loss is much less (about 6X lower) than CV^2.** Detailed explanation is available in application note Switching Fast SiC FETs with a Snubber and in webinar Minimizing EMI and switching loss for fast SiC FETs.
For ZVS soft-switching the device snubber has no resistor Rs in series to avoid Rs energy loss during ZVS turn-on in each soft-switching cycle. Instead, the damping effect is realized by bus snubber resistor Rd shown in **Figure 6 (b)** which is also series connected in the power loop. Wide PCB traces or planes are recommended for snubber RC terminals for better heat dissipation.

Double pulse test (DPT) schematic: Load inductor (L) represents an inductive load. The DC LINK capacitor has high capacitance to hold DC bus voltage while providing energy to the load inductor L. Cd is the power loop decoupling capacitor, usually a ceramic capacitor. It is located very close to the half-bridge to minimize power loop stray inductance during switching transients. CT is a current transformer for current measurement. CT measures the sum of device current and snubber current.

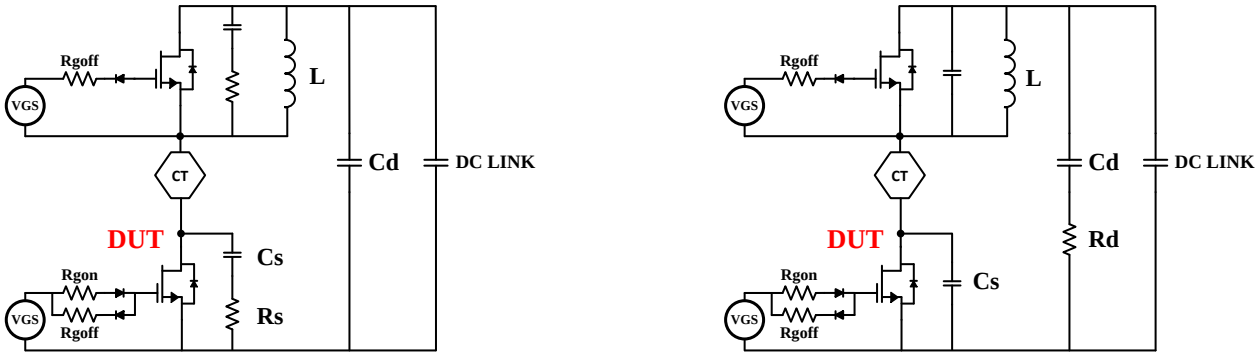


Figure 6. DPT schematic with RC snubbers on both switches for (a) hard-switching and (b) ZVS soft-switching.

Snubber greatly reduce turn-off switching loss

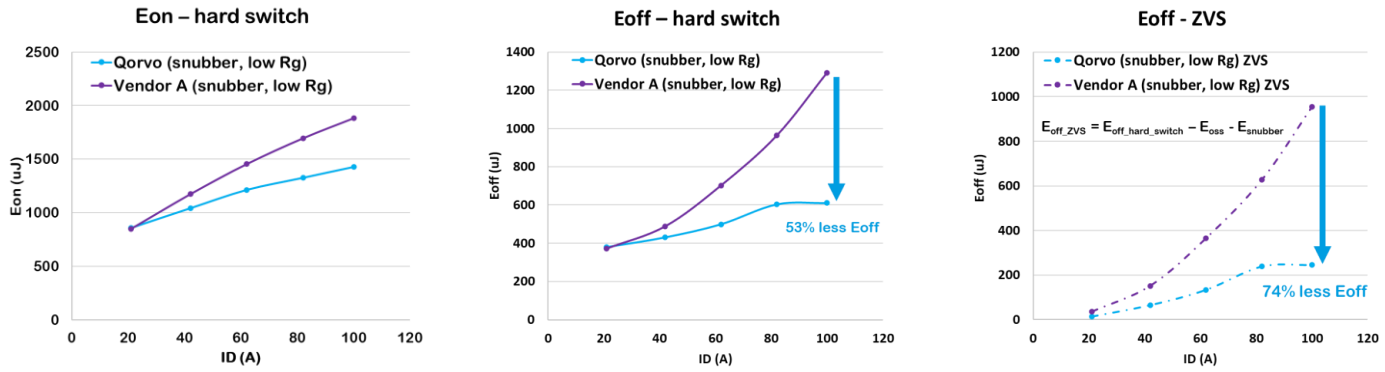
Table 2 in previous section shows static parameter benchmark between a Qorvo SiC E1B 1200V 100A half-bridge module UHB100SC12E1BC3N and a SiC MOSFET (part X also 1200V 100A rated) from vendor A in same package (same pinout). **Table 3** shows the dynamic test conditions on a double pulse test (DPT) EVB.

SPECS	QORVO	SiC MOSFET VENDOR A	SiC MOSFET VENDOR A
Part number	UHB100SC12E1BC3N	X	X
Device snubber	2x330 pF	No snubber	2x330 pF
Rgon (external)	15 Ω	2.2 Ω	2.2 Ω
Rgoff (external)	4.7 Ω	5 Ω	2.2 Ω
Bus decoupling snubber	0.2 uF, 2.35 Ω		
Bus voltage	800 V		
Load current	20 A to 100 A		
Gate bias	15 V to -5 V		

Table 3. Dynamic test conditions: Qorvo E1B module (1200V, 100A, half-bridge) v.s. a SiC MOSFET pin compatible part (Vendor A).

The two benchmark parts are tested at room temperature with 800 V bus and current stepping from 20 A to 100 A. Bus decoupling capacitor is used to minimize power loop stray inductance. More details are available in the snubber configuration section. Two 330 pF snubber capacitors are used for each switch position of the Qorvo E1B half-bridge module. SiC MOSFET benchmark part X is tested under two conditions to demonstrate that **snubber effectiveness is universal for all fast-switching devices and that using snubber provides much better trade-off between switching loss and waveform control than a simple Rg control method**.

Figure 7 compares switching losses based on **Table 3**. All loss measurement includes both device switching losses and device snubber losses. A pure capacitive device snubber is used as shown in **Figure 7 (c)** to avoid snubber resistor loss in ZVS.



(a) Turn-on loss (hard-switching) (b) Turn-off loss (hard-switching) (c) Turn-off loss (ZVS soft-switching)

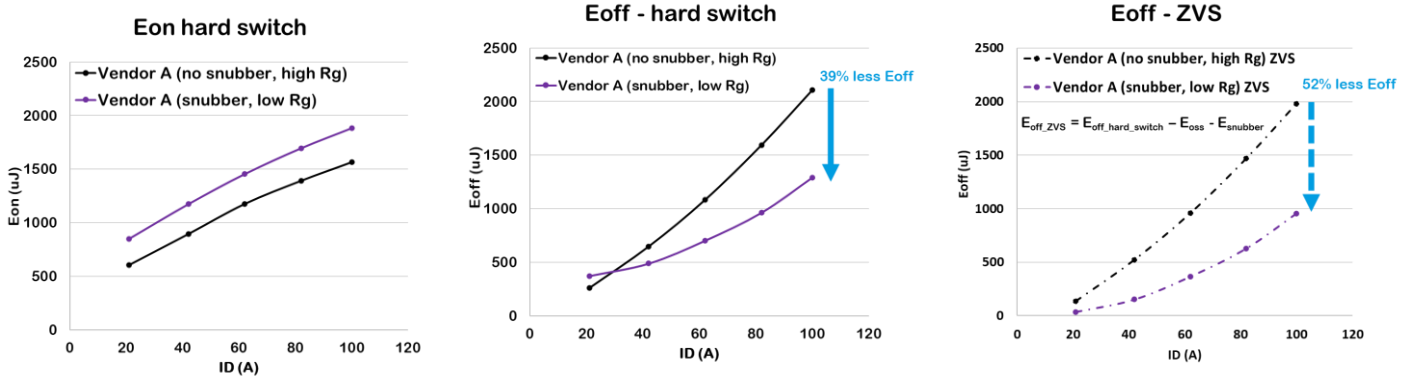
Figure 7. Qorvo SiC E1B module (UHB100SC12E1BC3N) switching loss benchmark with SiC MOSFET with recommended snubber.

Figure 7 (a) shows hard-switched turn-on loss comparison. The blue curve is Qorvo SiC E1B (UHB100SC12E1BC3N) with snubber. The purple curve is SiC MOSFET (part X) from vendor A with snubber. Qorvo SiC E1B has 24% lower hard turn-on loss with recommended snubber conditions in **Table 3**. The hard-switched turn-on loss does scale with device snubber capacitance. Therefore, proper selection of device snubber capacitance value is important to avoid unnecessary increase in hard-turn-on loss.

Figure 7 (b) shows hard-switched turn-off loss comparison. Blue curve is Qorvo SiC E1B (UHB100SC12E1BC3N) with snubber and using low Rgoff. The purple curve is SiC MOSFET (part X) from vendor A with snubber and using low Rgoff. Comparing purple and blue curves at 100 A shows **53% turn-off loss reduction by choosing Qorvo SiC E1B module** (UHB100SC12E1BC3N).

Figure 7 (c) shows **Qorvo SiC E1B module is extremely efficient in ZVS soft-switching applications**. This chart is derived from **Figure 7 (b)** by subtracting device output capacitance energy (Eoss) and device snubber capacitor energy (Esnub) since these energies are ZVS turn- recycled during next on event to load and should not be considered as energy losses. The blue curve is Qorvo SiC E1B (UHB100SC12E1BC3N) with snubber using low Rgoff. The purple curve is SiC MOSFET from vendor A with snubber using low Rgoff. Comparing purple and blue curves at 100 A shows **74% turn-off loss reduction by choosing Qorvo SiC E1B module** (UHB100SC12E1BC3N).

Figure 8 compares snubber effects on switching losses for SiC MOSFET (vendor A) based on **Table 3**.



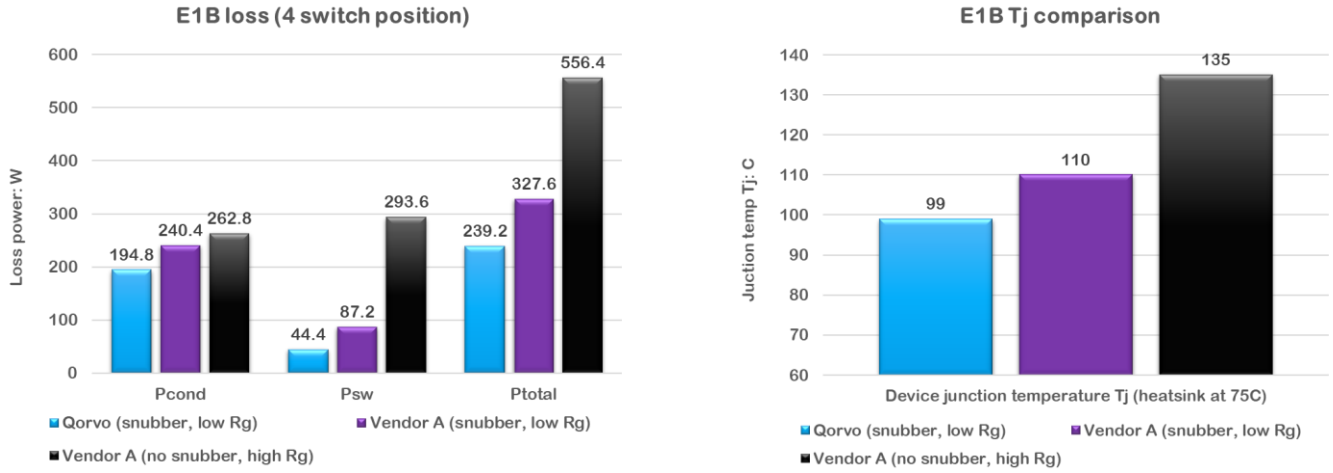
(a) Turn-on loss (hard-switching) (b) Turn-off loss (hard-switching) (c) Turn-off loss (ZVS soft-switching)

Figure 8. Snubber effects on switching losses for SiC MOSFET (vendor A).

Figure 8 (a) shows hard-switched turn-on loss comparison. The black curve is SiC MOSFET (part X) from vendor A without snubber. The purple curve is SiC MOSFET with snubber. The hard-switched turn-on loss does scale with device snubber capacitance. Therefore, proper selection of device snubber capacitance value is important to avoid unnecessary increase in hard-turn-on loss.

Figure 8 (b) shows hard-switched turn-off loss comparison. The purple curve is SiC MOSFET (part X) from vendor A with snubber using low Rgoff. The black curve is SiC MOSFET (part X) from vendor A without snubber using high Rgoff to control VDS overshoot. Comparing black and purple curves at 100 A shows **39% turn-off loss reduction by using snubber for a SiC MOSFET module**. In **Figure 8 (b)** **choosing Qorvo SiC E1B module (UHB100SC12E1BC3N) provides another 53% turn-off loss reduction**.

Figure 8 (c) compares snubber effects on turn-off loss for ZVS soft-switching applications. This chart is derived from **Figure 8 (b)** by subtracting device output capacitance energy (Eoss) and device snubber capacitor energy (Esnub) because this energy is recycled during next ZVS turn-on event to load and should not be considered as energy loss. The black curve is SiC MOSFET from vendor A without snubber using high Rgoff to control VDS overshoot. The purple curve is SiC MOSFET from vendor A with snubber using low Rgoff. Comparing black to purple curves at 100 A shows **52% turn-off loss reduction by using snubber for a SiC MOSFET module**. In **Figure 8 (c)** **choosing Qorvo SiC E1B module (UHB100SC12E1BC3N) provides another 74% turn-off loss reduction**.



(a) (b)

Figure 9. Loss analysis for a 50kW PSFB: (a) Loss distribution and (b) device junction temperature.

Figure 9 shows the loss analysis simulation results of a 50kW phase-shifted full-bridge using benchmark data collected from **Figure 7** and **Figure 8**. The simulation assumes 50kW rated power, 800V input bus voltage, 400V output voltage, 150kHz switching frequency, 150ns deadtime, heatsink temperature fixed at 75C. The blue bar represents Qorvo SiC E1B module (UHB100SC12E1BC3N) using snubber with low Rg. The purple bar represents Vendor A SiC MOSFET module using snubber with low Rg. The black bar represents Vendor A SiC MOSFET module using only high Rg without device snubber.

Using high Rg alone to control VDS turn-off spike is very inefficient. The turn-off loss of using SiC MOSFET with high Rg is 6.6X higher than Qorvo solution. When pure capacitive device snubber is used for the same SiC MOSFET module, its turn-off loss is reduced from 293W to 87W! Accordingly, its junction temperature is reduced from 135C to 110C. At same condition (snubber with low Rg), using Qorvo solution can further reduce junction temperature to 99C.

To sum up, snubbers are strongly recommended for ZVS soft-switching applications like PSFB and LLC to significantly improve efficiency and lifetime (lower Tj). Qorvo's SiC E1B modules when properly used with snubber can further reduce turn-off switching loss to enable exceptional performance in ZVS soft-switching applications.

Snubber explanation

Figure 10 shows the turn-off waveforms at 100 A with the 3 different conditions in **Table 3**. Please note the current waveform includes both device current and device snubber current as shown in **Figure 6 (b)**. Therefore, the integration of IDS and VDS in **Figure 10**

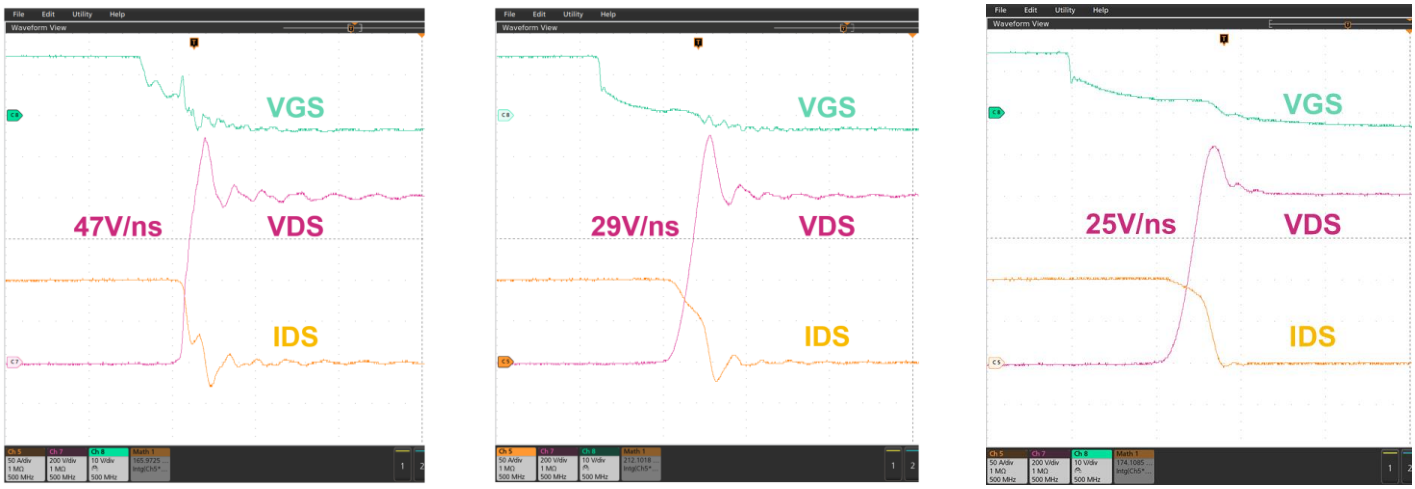
represents hard-switch turn-off loss. For soft-switch turn-off loss (ZVS turn-on) the device Eoss and snubber Esnub should be subtracted from the hard-switch turn-off loss measured in **Figure 10**.

Turn-off current waveforms explain why using snubber with fast-switching device achieves best (lowest) turn-off loss.

In **Figure 6 (b)**, when low side DUT (device under test) turns off, the same dv/dt exists for both high side and low side device because bus voltage is maintained a constant 800 V by DC LINK and decoupling capacitor. Therefore, displacement current exists for device output capacitance (Coss) and device snubber capacitance (Cs) based on:

$$C \cdot \frac{dV}{dt} = I$$

In other words, during DUT turn-off dv/dt transition, the high side Coss and Cs extract displacement current from inductive load (L) to discharge themselves, thus reducing IDS for the DUT to have less VDS and IDS overlap (turn-off loss). This effect is clearly shown in **Figure 10 (a, b, c)**. Based on the above capacitor equation, faster device turn-off dv/dt and higher equivalent device output capacitance (Coss + Cs) means more current extracted from load, thus less voltage and current overlap for DUT, hence lower turn-off loss.



(a) Qorvo SiC with snubber (b) SiC MOSFET with snubber (c) SiC MOSFET NO snubber (high Rg)

Figure 10. 100 A turn-off waveforms. CH5 is IDS (50 A/div). CH7 is VDS (200 V/div). CH8 is VGS (10 V/div). Time is 100 ns/div.

Power cycling

Reliability of power modules and lifetime assessment are key to improving system reliability and lifetime, especially for emerging wide-band-gap (WBG) semiconductors (SiC, GaN, etc.). The main failure modes of power module are related to thermo-mechanical fatigue. Power cycling tests are accelerated tests to switch device under test (DUT) on and off frequently so the device junction temperature can cycle in a controlled method. It applies thermo-mechanical stress to test the reliability of module packaging (wire bond, die attach, etc.). In the meantime, it also applies electrical stress to semiconductor die and packaging components (wire bond, lead, etc.) to better simulate the temperature gradients of actual applications than a passive temperature cycling test.

Figure 11 demonstrates why **Qorvo SiC E1B stack-cascode modules have 2X power cycling compared to normal SiC MOSFET modules**. **Figure 11 (a)** shows that in a stack cascode structure the Si MOSFET sits on top of SiC JFET. This allows power source wire bond to be attached on the Si MOSFET. Since Si is less rigid than SiC the thermo-mechanical stress of wire bond interface during power cycling is much reduced thus extending power cycling lifetime by 2X. Additionally, Qorvo applies silver sinter die-attach to both layers, from Si MOSFET to SiC JFET and from SiC JFET to DBC, to further improve reliability comparing to solder die-attach (widely used in today's SiC discretes and modules). The advantage of Si power cycling performance over SiC has been previously reported. [Reference Paper]: *F. Hoffmann, N. Kaminski and S. Schmitt, "Comparison of the Power Cycling Performance of Silicon and Silicon Carbide Power Devices in a Baseplate Less Module Package at Different Temperature Swings," 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Nagoya, Japan, 2021, pp. 175-178, doi: 10.23919/ISPSD50666.2021.9452242.*

Figure 10 (b) shows power cycling benchmarks from lab measurements. The horizontal axis is the device junction temperature rise, ΔT_j, used during power cycling. The vertical axis is the number of power cycles till failure. Devices under test are Qorvo SiC E1B 1200V 50A half-bridge module, UHB50SC12E1BC3N, and a Vendor A 1200V 16mΩ SiC MOSFET half-bridge module in same E1B package. At 100C junction temperature rise, Qorvo SiC E1B module (blue dots) has more than 2X better cycles compared to SiC MOSFET module in same package. Qorvo specifies stack cascode structure in part number with "SC". Three Qorvo SiC E1B modules implement stack cascode structure, UFB25SC12E1BC3N (1200V, 25A, 35mΩ, full-bridge), UHB50SC12E1BC3N (1200V, 50A, 19mΩ, half-bridge), UHB100SC12E1BC3N (1200V, 100A, 9.3mΩ, half-bridge).

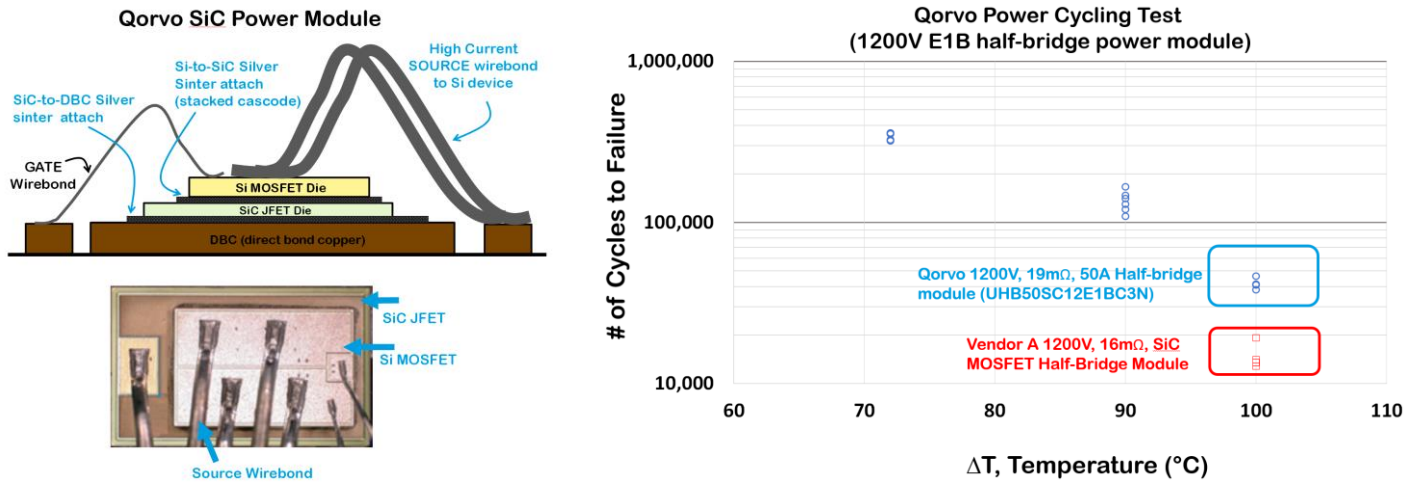


Figure 10. Qorvo SiC E1B power cycling: (a) stack-die structure with power wire bond to Si die and (b) power cycle vs SiC MOSFET.

Summary

Qorvo SiC E1B half-bridge and full-bridge modules offer excellent static (R_{DSON}, Coss, Rthjc, etc.) and dynamic performance (Eon, Eoff) to achieve superior efficiency and power density for high power applications. The stack cascode E1B modules also provide Si level power cycling performance (reliability and lifetime) which is more than 2X better than SiC MOSFET. The extremely low turn-off loss of Qorvo SiC E1B modules with snubber is especially attractive to soft-switch (ZVS turn-on) applications such as PSFB, LLC, etc.

DPT EVB available

Qorvo provides two double pulse test (DPT) EVB options to support customer evaluation of the half-bridge E1B module and full-bridge E1B module. The EVBs are available through Qorvo sales channel. **Figure 11** shows an example of full-bridge E1B module DPT EVB. For more information, please refer to this E1B EVB application note SiC E1B Modules DPT EVB User Guide.

Figure 11. Full-bridge E1B module DPT EVB 3D view. Top view (left) and bottom view (right).

Contact Information

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