APPLICATION NOTE

SiC E1B Modules DPT EVB User Guide

Scope

Qorvo has combined the advantageous SiC JFET based power device with an industry standard power module package, E1B, to further enhance power density, efficiency, cost-effectiveness, and ease of use for industrial power systems. For more details on Qorvo SiC E1B module benefits please refer to SiC E1B Modules Technical Overview.

This application note introduces Qorvo's latest E1B power module DPT EVB (half-bridge and full bridge). To fully exploit the fast-switching capability of SiC devices, critical design guidelines must be followed to ensure success. This application note shares PCB design and waveforms of Qorvo SiC E1B modules and practical design tips to implement the fast-switching E1B module successfully and reliably.

IMPORTANT: Snubbers are strongly recommended for SiC E1B modules due to their intrinsic fast-switching speed. Also, snubber greatly reduces turn-off switching loss making SiC E1B modules extremely attractive in ZVS (zero voltage turn-on) soft-switching applications such as phase-shifted full-bridge (PSFB), LLC, etc.

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

This application note also provides resource links to simulation models, assembly guidelines, thermal characteristics, reliability, and qualification documents.

Resource and reference

[1] SiC E1B Modules Technical Overview

[2] SiC E1B Modules Mounting Guideline

[3] SiC FET & Module User Guide

[4] SiC E1B Modules DPT EVB User Guide

[5] Qorvo SiC Module Link: SiC Modules - Qorvo

[6] Web based loss calculator for part selection: https://www.qorvo.com/design-hub/design-tools/interactive/fet-jet-calculator

[7] Qorvo SiC power solution central hub: https://www.qorvo.com/innovation/power-solutions/sic-power

[8] More design tips: https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips

[9] Origins of SiC FETs and Their Evolution Towards the Perfect Switch

Contents

Introduction to double pulse test

The Double Pulse Tester provides flexibility in dynamic characterization (switching loss, speed, delay, etc.) of the device under test (DUT) under varying voltage and current conditions. A double pulse tester (DPT) uses a half bridge structure with an inductive load. A simplified schematic is shown in **Figure 1**. The low side device of a half-bridge is the device under test (DUT) with ON/OFF gate signals. The high side switch is a freewheeling device with OFF gate signal. Inductive load L is connected between phase node (mid-point between high side and low side device) and positive DC bus. CT measures the sum of device current and snubber current.

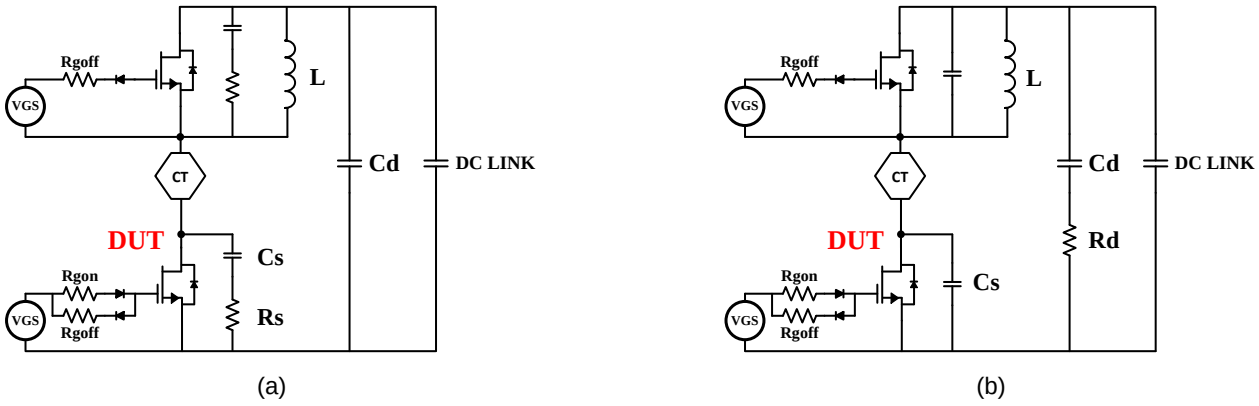


Figure 1. DPT schematic with RC snubbers on both switches for (a) hard-switching and (b) ZVS soft-switching.

Figure 2 illustrates typical DPT waveforms and operation. During the DUT first gate-ON pulse, constant bus voltage applies across the load inductor L through DUT which results in a linear increase of inductor current. By adjusting the DUT first gate pulse ON time the inductor current level, which is the same as the DUT first turn-off current, can be controlled. When the DUT is turned off at specified current level, inductor current will freewheel through the high side device until DUT is turned ON again. Measurements of VGS, VDS, IDS at the “turn-off” and “turn-on” transient reveal device switching speed (dv/dt, di/dt slew rate), gate delay, switching loss, and reverse recovery (high side device) performance.

By selecting the appropriate inductor value, the two V_{GS} pulses should have short duration relative to the period of a test to avoid self-heating of device junction temperature (Tj) from conduction loss. To test at junction temperatures higher than room temperature an electrically insulated heater can be placed on the DUT to set its junction temperature.

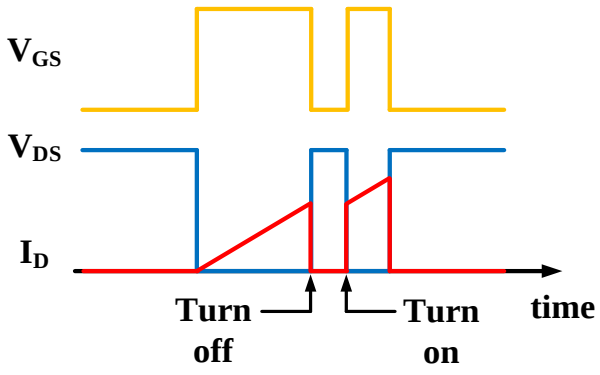


Figure 2. DPT typical waveforms of VGS, VDS, IDS for the low side DUT.

Snubber configuration

A typical RC snubber configuration in a half-bridge is shown in **Figure 1** for hard-switching and ZVS soft-switching applications.

Bus snubber consists of decoupling capacitor (Cd) and resistor (Rd) between the fast-switching half-bridge and DC LINK bulk capacitor. When the device under test (DUT) is turning on/off, the bypass capacitor Cd provides transient energy path to commutate the high side (HS) and low side (LS) devices. This is the transient power loop. Cd should be placed as close as possible to the half-bridge to minimize power loop stray inductance. This enables faster di/dt (current slew rate) while containing VDS overshoot spikes. It is a much more efficient way than simply increasing Rg (gate resistor) to contain VDS overshoot spikes. Cd is typically 0.1 uF. Rd is typically 1 Ω to 4.7 Ω. Actual number depends on PCB design.

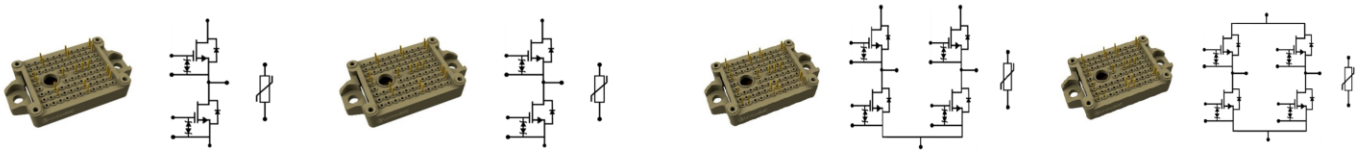
Device snubber consists of capacitor (Cs) and resistor (Rs) across device drain-to-source terminals. Cs is typically 2-3 times the device Coss(er) (energy equivalent output capacitance). Rs is typically 1 Ω to 4.7 Ω. Cs helps to control voltage slew rate (dv/dt) and VDS overshoot spikes. Rs helps to damp the VDS ringing.
For hard-switching the device snubber resistor Rs is placed near device drain-to-source to provide best damping effects. **Please note that snubber resistor power loss is much less (about 6X lower) than CV^2.** Detailed explanation is available in application note Switching Fast SiC FETs with a Snubber and in webinar Minimizing EMI and switching loss for fast SiC FETs.
For ZVS soft-switching the device snubber has no resistor Rs in series to avoid Rs energy loss during ZVS turn-on in each soft-switching cycle. Instead, the damping effect is realized by bus snubber resistor Rd shown in **Figure 5 (b)** which is also series connected in the power loop. Wide PCB traces or planes are recommended for snubber RC terminals for better heat dissipation.

Double pulse test (DPT) schematic: Load inductor (L) represents inductive load. The DC LINK capacitor has high capacitance to hold DC bus voltage while providing energy to the load inductor L. Cd is the power loop decoupling capacitor, usually a ceramic capacitor. It is located very close to the half-bridge to minimize power loop stray inductance during switching transients. CT is a current transformer for current measurement. CT measures the sum of device current and snubber current.

Qorvo SiC E1B module

Qorvo delivers low on-resistance (R_{DSON} at room temperature) in an industry standard (pin compatible) E1B power module package as shown in **Figure 3**. Qorvo's E1B power module provides two topology options: half-bridge (HB) configuration and full-bridge (FB) configuration. Both HB and FB are the backbone of many popular power conversion topologies.

UHB50SC12E1BC3N **UHB100SC12E1BC3N** **UFB15C12E1BC3N** **UFB25SC12E1BC3N**



1200V HALF-BRIDGE Cascode FET Power Modules			
Part #	RDS(on) Typ 25C	Max Continuous Drain Current	Max Continuous Drain Current
UHB50SC12E1BC3N	19mohm	50A (Tc = 50C)	69A (Tc = 25C)
UHB100SC12E1BC3N	9.4mohm	100A (Tc < 85C)	100A (Tc = 25C)

1200V HALF-BRIDGE Cascode FET Power Modules			
Part #	RDS(on) Typ 25C	Max Continuous Drain Current	Max Continuous Drain Current
UFB15C12E1BC3N	70mohm	15A (Tc = 105C)	24A (Tc = 25C)
UFB25SC12E1BC3N	35mohm	25A (Tc = 90C)	36A (Tc = 25C)

Figure 3. Qorvo 1200V SiC E1B half-bridge and full-bridge module RDS(on) and current rating.

Qorvo's 4 E1B modules shown in **Figure 3** are all 1200V rated. The half-bridge module has two R_{DSON} classes.

UHB50SC12E1BC3N has typical R_{DSON} of 19mOhm at 25C junction temperature and 69A rated current at 25C case temperature.

UHB100SC12E1BC3N has typical R_{DSON} of 9.4mOhm at 25C junction temperature and 100A rated current at 25C case temperature.

The full-bridge module has two R_{DSON} classes.

UFB15C12E1BC3N has typical R_{DSON} of 70mOhm at 25C junction temperature and 24A rated current at 25C case temperature.

UFB25SC12E1BC3N has typical R_{DSON} of 35mOhm at 25C junction temperature and 36A rated current at 25C case temperature.

Half-bridge E1B DPT EVB

Absolute Maximum Rating: The Qorvo SiC E1B half-bridge module Double Pulse Tester (DPT) EVB is limited to a maximum of **1000 V** (drain to source peak voltage). Maximum load current is limited by the rating of device under test and load inductor.

EVB introduction

Figure 4 shows the half-bridge DPT evaluation board with top side and bottom side views.
Low-power signals and 12 V auxiliary power supply are separated from the high-voltage terminals.
To avoid high dv/dt induced turn-on for fast SiC devices an isolated gate driver and isolated power supplies are used to suppress high dv/dt induced common mode noise in the gate signal path. Both high side and low side has its own gate driver.
The DC link decoupling snubber resistor Rd is optional when device snubber Rs is used for hard-switching applications.
The DC link decoupling snubber resistor Rd is recommended when device snubber Rs is NOT used for ZVS soft-switching applications. It provides measurement of low side DUT drain current for switching turn-on loss (Eon), switching turn-off loss (Eoff) and measurement of high side freewheeling device current for reverse recovery (Qrr).
Due to the fast-switching capability of SiC devices, the transient power loop PCB layout is designed to minimize the parasitic inductances and capacitances.

(a) (b)

Figure 4. Half-bridge E1B module DPT EVB 3D view. (a) top view and (b) bottom view.

Isolated gate driver and gate drive voltage: Isolated gate drivers with CMTI (common mode noise immunity) above 100V/ns is recommended to tolerate fast dv/dt slew rate of SiC FET to fully exploit the fast-switching capability of SiC to increase power density and improve efficiency. An isolated gate driver (ADUM4136BRWZ) with Desat protection is used in the EVB.
The gate drive voltage range from positive VDD to negative VEE is designed to be flexible in this EVB.
Figure 5 shows the gate drive schematic for the low side switch. The maximum gate drive voltage range is 20V, limited by U5. D3 and D4 are Zener diodes to define the desired VDD and VEE. For example, as shown in **Figure 5**, turn-on voltage VDD is 15V, turn-off voltage VEE is -3.3V. The remaining voltage of the total 20V drops on R4. JP3 and JP4 are jumpers that provide option to use 0V turn-off or negative VEE turn-off. For 0V turn-off, both JP3 and JP4 are populated with 0Ω resistor. For negative VEE turn-off, only JP4 is populated with 0Ω resistor. JP3 is left unpopulated. The EVB uses negative VEE turn-off by default.

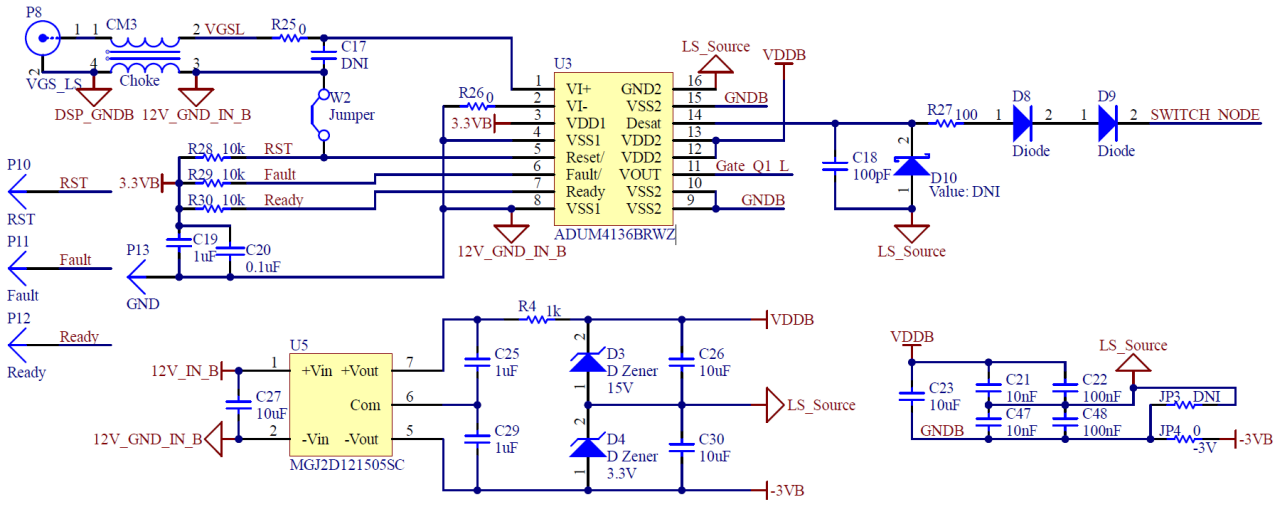


Figure 5. Half-bridge E1B module DPT EVB gate drive schematic for low side device.

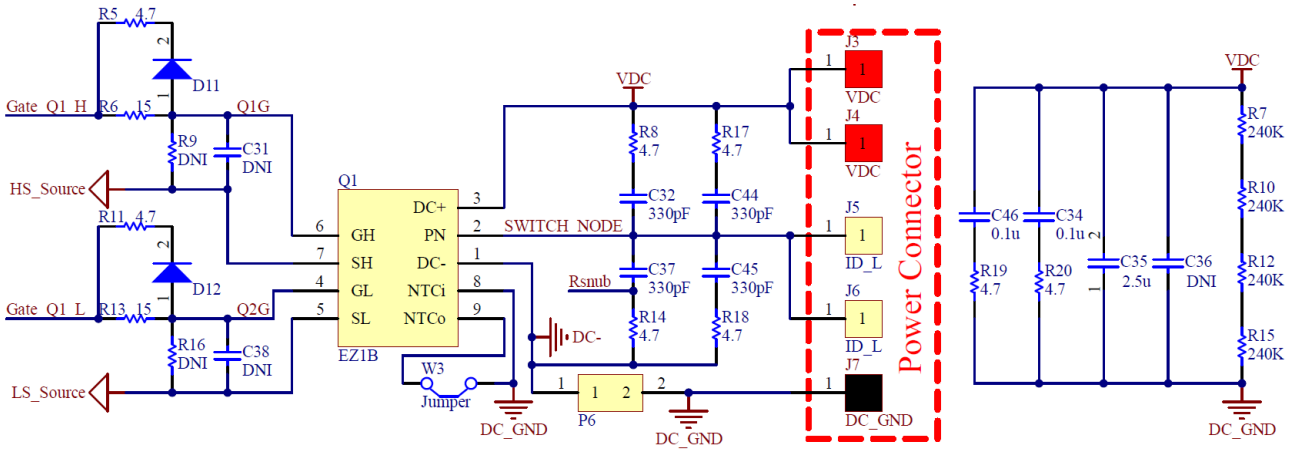


Figure 6. Half-bridge E1B module DPT EVB power loop and gate resistor network.

Input gate signal: In **Figure 5** the input gate signal should provide a 3.3 V logic signal via the BNC connector. The unswitched switch position must have its gate signal input BNC connector shorted. The first pulse width sets the load current for the test. Inductor current and first gate pulse width follow this equation:

$$L \cdot \frac{di}{dt} = V$$

L is inductor inductance. V is the bus voltage. “di” is the desired turn-off current. “dt” is the first gate pulse width.

For example, to achieve 20 A load current at 800 V DC bus voltage with a 200 uH inductor, the first pulse width should be 5 µs. The second pulse width should be less than 1 µs to avoid excess increment of inductor current. Low pass RC filter is recommended for gate driver input signal to further reduce chance of false turn-on by common mode noise generated from SiC fast dv/dt. R25 (0 Ω) and C17 (330 pF) filter low side gate input while R2 (0 Ω) and C6 (330 pF) form the low pass filter for high side gate input.

Gate resistors: In **Figure 6** R13 is turn-on gate resistor (Rgon) for low side switch. R11 is turn-off gate resistor (Rgoff) for low side switch. D12 is a steering diode to allow different Rgon and Rgoff values to help flexible design of turn-on and turn-off speed. For high side switch, R6 is the Rgon, R5 is the Rgoff, and D11 is the steering diode. R9 and R16 are pull down gate resistors with resistance around 10kΩ. C38 (1 nF) and C31 (1 nF) are gate-to-source filter capacitors to further smooth gate waveforms.

Snubbers: In **Figure 6** both device snubber and bus snubber positions are reserved. For detailed function explanation please refer to the snubber configuration section above. R8, C32, R17, C44 are device snubbers for high side switch. R14, C37, R18, C45 are device snubbers for low side switch. R19, C46, R20, C34 are bus snubbers for the half-bridge.

Please follow Qorvo SiC FET User Guide to select appropriate values for Rgon, Rgoff, and snubber capacitor.

Measurement

All measurements (VGS, VDS, IDS) are on the low side device. The oscilloscope used for test results in this document is Tektronix MSO58B. VGS voltage is measured with Tektronix TPP1000 1 GHz voltage probe. VDS is measured with Pomona 6498 400 MHz voltage probe. DUT drain current is measured at the source using a 1:10 turn ratio transformer followed by a Pearson 2877 200 MHz Current transformer. The compact 10:1 transformer is constructed with a ferrite toroid (TC9.5/4.8/3.2-3E27) core as shown in **Figure 7**.

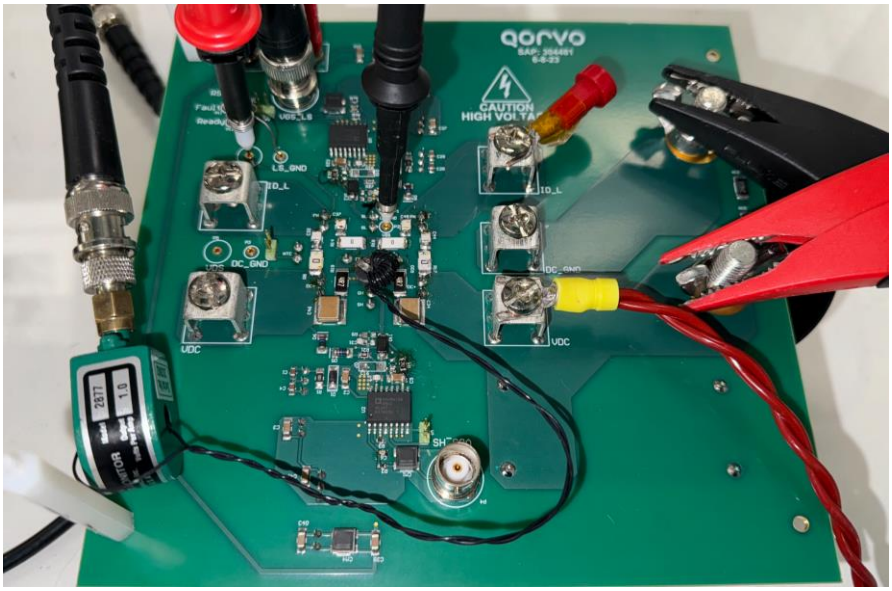


Figure 7. Half-bridge E1B module DPT EVB measurement setup.

Voltage measurement: Passive probes are used for voltage measurement due to their higher bandwidth and smaller ground loop compared to conventional differential probes. The black probe measures VGS. The red probe measures VDS. Since the ground of both VGS and VDS probe is connected to scope ground, common mode choke is recommended for both VGS and VDS cables to avoid common mode noise coupling into oscilloscope during switching transients. Please make sure probes and probe tips are mechanically secure to avoid accidentally shorting high voltage during testing.

Current measurement: current measurement is inserted in jumper P6 shown in **Figure 6** for the low side switch. DUT current is measured at the source using a 1:10 turn ratio transformer followed by a Pearson 2877 Current transformer. The compact 1:10 transformer is constructed with a ferrite toroid (Ferroxcube TC9.5/4.8/3.2-3E27) core as shown in **Figure 7**. The Pearson 2877 transformer is connected to oscilloscope through a BNC cable with 1MΩ termination. The Pearson transformer 2877 (1 V/A) has 200 MHz bandwidth. When used with the 1:10 transformer, the two-stage current transformer has an equivalent gain of 100 mV/A.

***WARNING**: The current measurement toroid and its secondary windings should all be considered at the DC bus high voltage level because the 1:10 transformer does not provide safety isolation.*
***WARNING**: The inductor is operated at High Voltage. Therefore, additional safeguards including placing the inductor and its leads with 1 kV isolation from the test bench and other user accessible areas are required.*

Test setup and results

Test procedure

DANGER: The Double Pulse Tester operates with high voltage which is not touch safe and can cause injury or death. Proper precautions must be followed in its use including:

1. Always properly turn on the gate signal generator and 12 V auxiliary power supplies before applying the High Voltage DC to the power loop.
2. The proper polarity of the high voltage DC must be observed.
3. The High Voltage DC must be disabled before the low voltage supplies.
4. After disabling the high voltage supply wait enough time for the DC bus main capacitor to discharge to 0 V before handling.

To perform a test, the external signal and supplies should be connected to the DPT in an unpowered state. Before any test starts all test probes and the inductor should also be safely and securely connected.

With all connections secured, the signals and supplies should be applied in the following order for safe measurement:

1. Enable the 12 V auxiliary power supply. This powers gate drive circuitry.
2. Enable the gate signal generator.
3. The unswitched switch position must have its gate signal input BNC connector shorted.
4. Test that the VGS pulse width generated by signal generator is correct by measuring VGS signal on the oscilloscope.
5. Test that the VGS voltage range is correct by measuring VGS signal on the oscilloscope.
6. Enable the high voltage DC.

Warning: Some components on board are polarized. Ensure the correct voltage polarity of each connector before plugging into the EVB to avoid damaging components.

After performing a test, the power supplies must be disabled in the reverse order:

1. Disable the High Voltage DC and wait until DC bus voltage drops to 0 V.
2. Disable the 12 V auxiliary power supply.
3. Disable the gate signal generator.

Test conditions and results

SPECS	QORVO	SIC MOSFET VENDOR A	SIC MOSFET VENDOR A
Part number	UHB100SC12E1BC3N	X	X
Device snubber	2x330 pF	No snubber	2x330 pF
Rgon (external)	15 Ω	2.2 Ω	2.2 Ω
Rgoff (external)	4.7 Ω	5 Ω	2.2 Ω
Bus decoupling snubber	0.2 uF, 2.35 Ω		
Bus voltage	800 V		
Load current	20 A to 100 A		
Gate bias	15 V to -5 V		

Table 1. Dynamic test conditions: Qorvo E1B module (1200V, 100A, half-bridge) v.s. a SiC MOSFET pin compatible part (Vendor A).

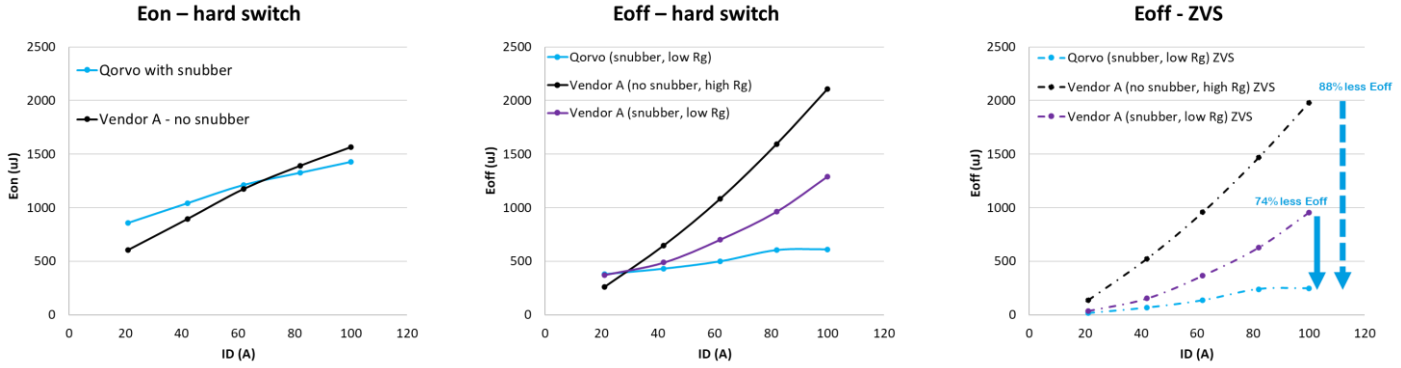
Table 1 shows the dynamic test conditions on a double pulse test (DPT) EVB. Qorvo's advanced SiC die technology enables superior electrical and thermal performance in the market as shown in **Table 2**. The two parts are matched by R_{DSON} at 125C with same voltage and current rating.

SPECS	QORVO	SiC MOSFET VENDOR A
Part number	UHB100SC12E1BC3N	X
ID	100 A	100 A
VDS (max)	1200 V	1200 V
V_{TH}	5 V	2.5 V
R_{DSON} (25C)	9.4 mΩ	10.5 mΩ
R_{DSON} (125C)	15 mΩ	14.1 mΩ
Body diode VF (100A, 25C)	1.63 V	5.1 V
Body diode VF (100A, 150C)	2.1 V	4.7 V
Qg (VGS -5V to 15V; VDS 800V)	170 nC	324 nC
Eoss (VDS 800V)	154 uJ	147 uJ
Rthjc (typ)	0.23 °C/W	0.428 °C/W

Table 2. Qorvo E1B module (1200V, 100A, half-bridge) key parameters v.s. a SiC MOSFET pin compatible part (Vendor A, X).

The two benchmark parts are tested at room temperature with 800 V bus and current stepping from 20 A to 100 A. Bus decoupling capacitor is used to minimize power loop stray inductance. More details are available in the snubber configuration section. Two 330 pF snubber capacitors are used for each switch position of the Qorvo E1B half-bridge module. SiC MOSFET benchmark part X is tested under two conditions to demonstrate that **snubber effectiveness is universal for all fast-switching devices and that using snubber provides much better trade-off between switching loss and waveform control than a simple Rg control method**.

Figure 7 compares switching losses based on **Table 1**. All loss measurement includes both device switching losses and device snubber losses. A pure capacitive device snubber is used as shown in **Figure 7 (c)** to avoid snubber resistor loss in ZVS.



(a) Turn-on loss (hard-switching) (b) Turn-off loss (hard-switching) (c) Turn-off loss (ZVS soft-switching)

Figure 6. Qorvo SiC E1B module (UHB100SC12E1BC3N) switching loss benchmark with SiC MOSFET.

Figure 7 (a) shows hard-switched turn-on loss comparison. Blue curve is Qorvo SiC E1B (UHB100SC12E1BC3N) with snubber. Black curve is SiC MOSFET (part X) from vendor A without snubber. The two curves are close to each other suggesting using snubber does not increase turn-on loss significantly. The hard-switched turn-on loss does scale with device snubber capacitance. Therefore, proper selection of device snubber capacitance value is important to avoid unnecessary increase in hard-turn-on loss.

Figure 7 (b) shows hard-switched turn-off loss comparison. Blue curve is Qorvo SiC E1B (UHB100SC12E1BC3N) with snubber and using low Rgoff. Black curve is SiC MOSFET (part X) from vendor A without snubber and using high Rgoff to control VDS overshoot. The purple curve is SiC MOSFET (part X) from vendor A with snubber and using low Rgoff. Comparing black to purple curves at 100 A shows **40% turn-off loss reduction by using snubber for a SiC MOSFET module**. Comparing purple to blue curves at 100 A shows **another 53% turn-off loss reduction by choosing Qorvo SiC E1B module** (UHB100SC12E1BC3N).

Figure 7 (c) shows Qorvo SiC E1B module is extremely efficient in ZVS soft-switching applications. This chart is derived from **Figure 7 (b)** by subtracting device output capacitance energy (Eoss) and device snubber capacitor energy (Esnub) because this energy is recycled during next ZVS turn-on event to load and should not be considered as energy loss. Blue curve is Qorvo SiC E1B (UHB100SC12E1BC3N) with snubber and using low Rgoff. Black curve is SiC MOSFET from vendor A without snubber and using high Rgoff to control VDS overshoot. The purple curve is SiC MOSFET from vendor A with snubber and using low Rgoff. Comparing black to purple curves at 100 A shows **52% turn-off loss reduction by using snubber for a SiC MOSFET module**. Comparing purple to blue curves at 100 A shows **another 74% turn-off loss reduction by choosing Qorvo SiC E1B module** (UHB100SC12E1BC3N).

Figure 8 shows switching waveforms of Qorvo SiC E1B module (UHB100SC12E1BC3N) at conditions shown in **Table 1**. VGS is 10 V/div, IDS is 50 A/div, VDS is 200 V/div.

(a) (b)

Figure 8. Half-bridge E1B module DPT EVB switching waveforms at 800 V, 100 A (UHB100SC12E1BC3N). (a) turn-on and (b) turn-off.

Schematic of half-bridge E1B module

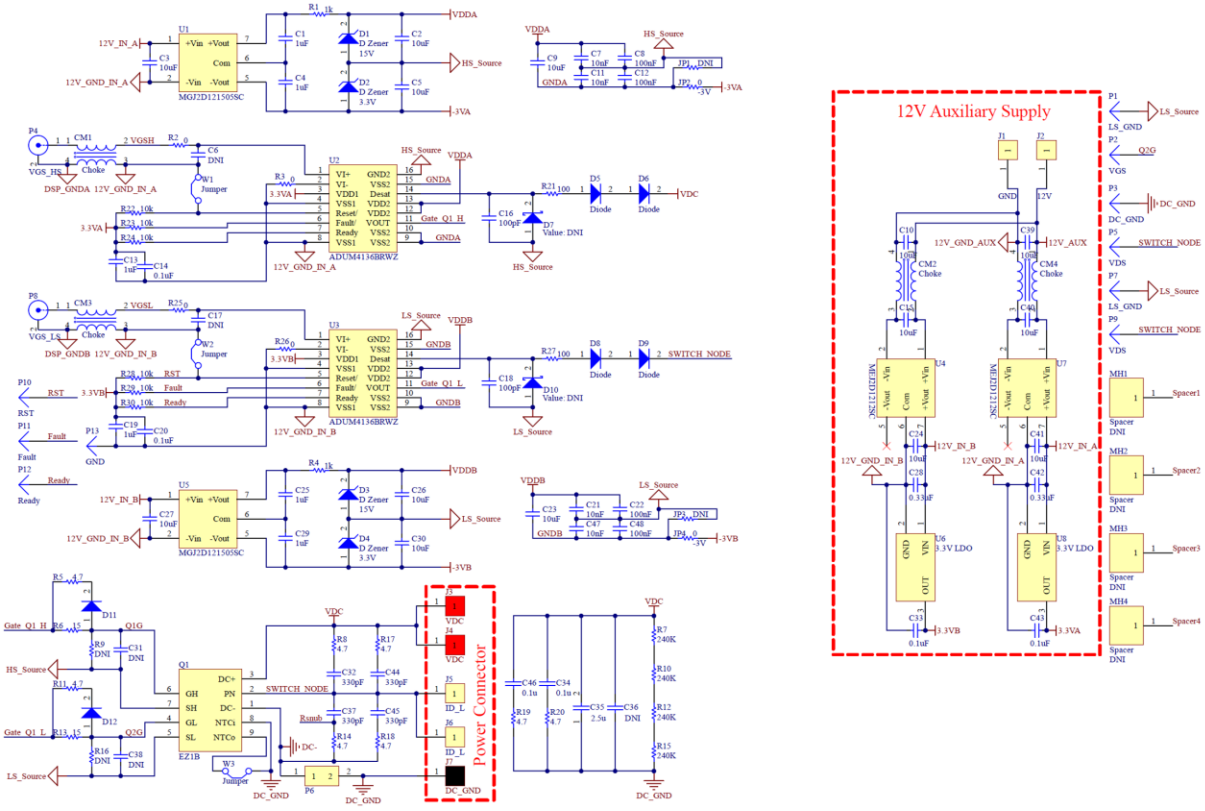
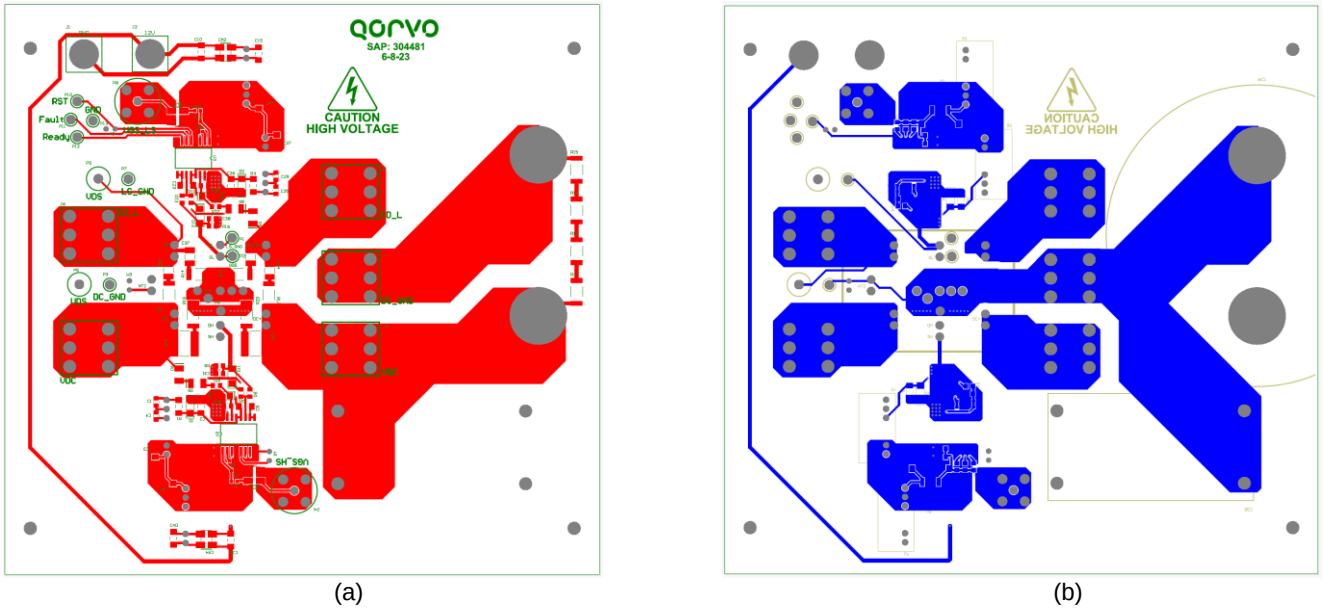


Figure 9. Half-bridge E1B module DPT EVB schematic.



(a) (b)

Figure 10. Half-bridge E1B module DPT EVB PCB print. (a) top layer and (b) bottom layer.

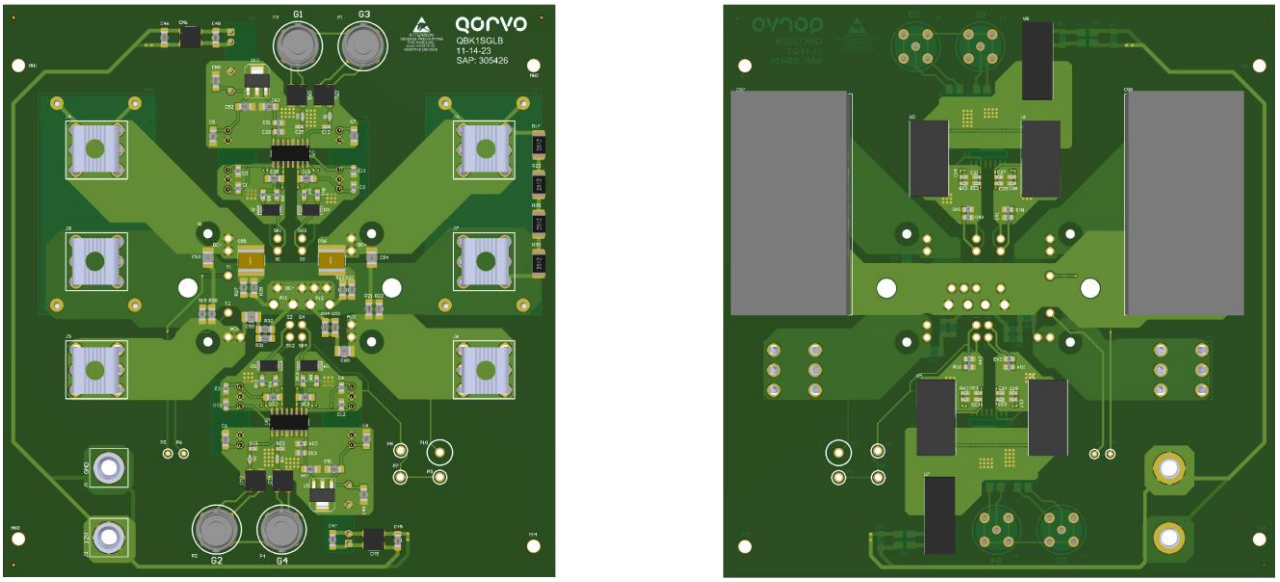
Full-bridge E1B DPT EVB

Absolute Maximum Rating: The Qorvo SiC E1B full-bridge module Double Pulse Tester (DPT) EVB is limited to a maximum of **1000 V** (drain to source peak voltage). Maximum load current is limited by the rating of device under test and load inductor.

EVB introduction

Figure 11 shows the full-bridge DPT evaluation board with top side and bottom side views.

Low-power signals and 12 V auxiliary power supply are separated from the high-voltage terminals.
To avoid high dv/dt induced turn-on for fast SiC devices an isolated gate driver and isolated power supplies are used to suppress high dv/dt induced common mode noise in the gate signal path. Both high side and low side has its own gate driver.
The DC link decoupling snubber resistor Rd is optional when device snubber Rs is used for hard-switching applications.
The DC link decoupling snubber resistor Rd is recommended when device snubber Rs is NOT used for ZVS soft-switching applications. It provides measurement of low side DUT drain current for switching turn-on loss (Eon), switching turn-off loss (Eoff) and measurement of high side freewheeling device current for reverse recovery (Qrr).
Due to the fast-switching capability of SiC devices, the transient power loop PCB layout is designed to minimize the parasitic inductances and capacitances.



(a) (b)

Figure 11. Full-bridge E1B module DPT EVB 3D view. (a) top view and (b) bottom view.

The same test procedure must be followed for safety operation as described in half-bridge EVB section.

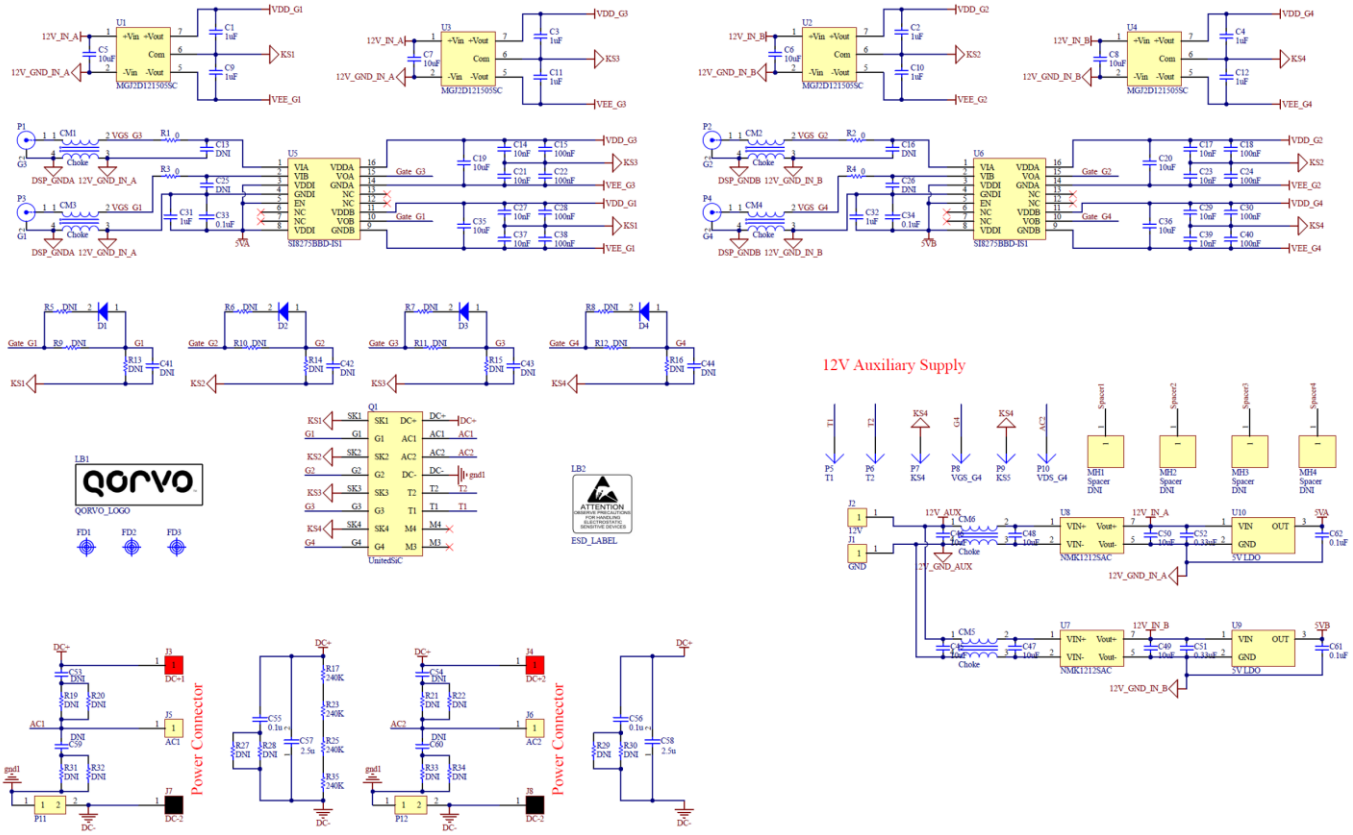
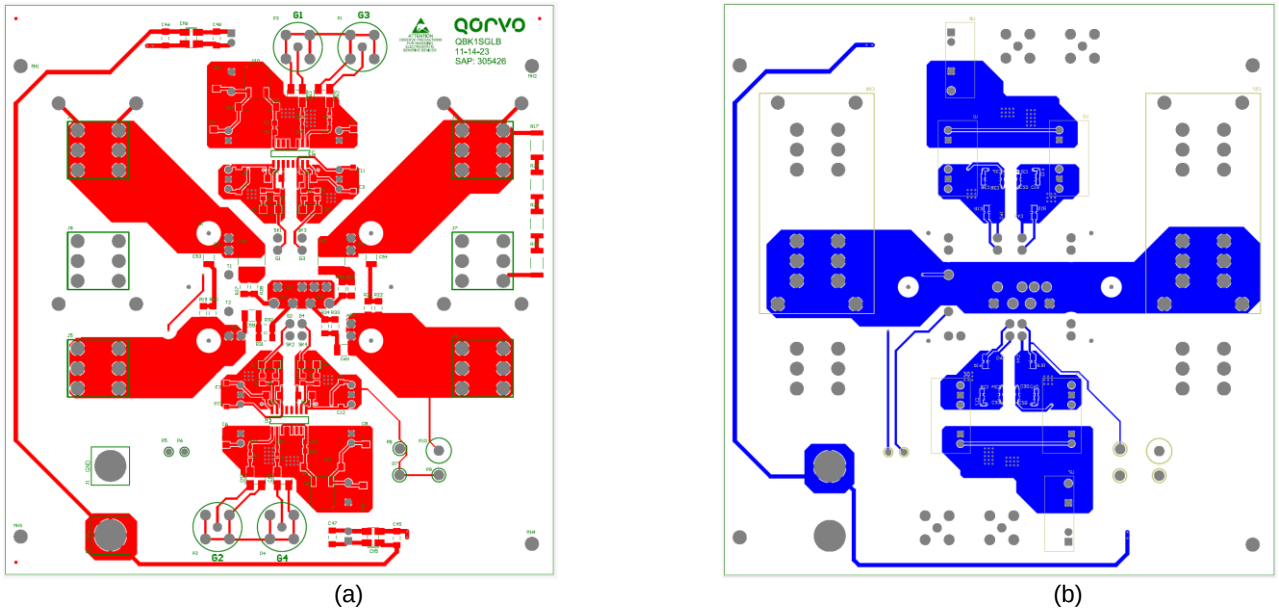


Figure 12. Full-bridge E1B module DPT EVB schematic.



(a) (b)

Figure 13. Full-bridge E1B module DPT EVB PCB print. (a) top layer and (b) bottom layer.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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