QM57508

Quad-Band GSM, Linear EDGE Transmit Module with Sixteen Dedicated High Linearity TRX Switch Ports

44 Pin 5.5 X 5.5 X 0.69 mm leadless SMT Package

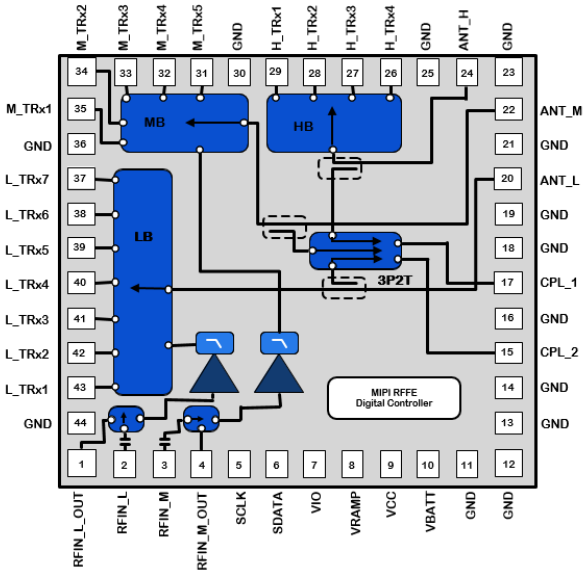
Product Overview

The QM57508 is a Transmit / Receive Module containing LB and MB 2G Power Amplifiers, 16 Tx / Rx Switch Ports, 3 Antenna and 2 Coupled Output Ports. The amplifiers supports GSM and EDGE Class 12 covering GSM850/GSM900 and DCS1800/PCS1900 bands. The MB 2G portion also supports Band 34 / 39 TD-SCDMA and TDD LTE capability.

The 16 Tx / Rx switch ports provides Low Insertion Loss / High Isolation paths to support 2G GSM/EDGE, 3G UMTS and 4G LTE Bands. The low band section has 7 TRX ports, the mid band section has 5 TRX ports and the high band section has 4 TRX ports. Each switch has a corresponding antenna output (LB_MB_HB). There is also a 3P2T switch, which supplies any antenna port to either coupled port. (CPL_1 / CPL_2)

A MIPI RFFE controller operates all functions including selection of PA Band / Mode / Bias and Switch Configurations.

Functional Block Diagram



Top View

Key Features

- Highly Functional, Small Footprint, Low Profile Module
- Seven LB High Linearity TRx ports.
- Five MB High Linearity TRx ports.
- Four HB High Linearity TRx ports.
- Low RF Switch Port Loss
- Three LB, MB, HB Antenna ports
- Two Antenna Coupler ports
- Two DC Blocked RF Input ports
- RF Input Bypass option
- MIPI RFFE Digital Control
- Supports Vramp or Pin Control

Applications

- WEDGE Handsets and Connected Devices
- GSM and Linear EDGE Transmit
- GSM and Linear EDGE Uplink Plus Multiband 3G and 4G
- Band 34 / 39 TD - SCDMA
- Band 34 / 39 TDD - LTE

Ordering Information

Part Number	Description
QM57508PCK	Evaluation Board Sample Kit
QM57508SB	Sample bag with 5 pieces
QM57508TR7	7" Reel with 750 pieces
QM57508TR13-5K	13" Reel with 5000 pieces
QM57508DK	Design Kit, QM57508PCK + RD2000 Communication Board

Absolute Maximum Ratings

Parameter	Ratings	Units
Supply Voltage (VCC, VBATT)	-1.2 to 6.0	V
Control Voltage (VRAMP)	-0.3 to 3.0	V
Digital control signals, SCLK, SDATA, VIO	2.0	V
RF Input Power for 2G PA	10	dBm
RF Input Power for all TRX Ports	31	dBm
Transmit Duty Cycle, Period = 4.6ms	50	%
Output Load VSWR	20:1	Note
Operating Temperature Range	-30 to +85	°C
Storage Temperature Range	-55 to +150	°C

Note: Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Operating Ambient Temperature (T_A)	-30	25	85	°C	
Supply Voltage, VCC	3.0	3.5	4.6	V	Normal operating range
Supply Voltage, VBATT	3.0	3.5	4.6	V	Normal operating range
Supply Leakage Current			10	µA	
VRAMP Voltage		0.16		V	GSM transmit; minimum RF output power
	0.25		1.65	V	GSM transmit; maximum RF output power
	1.25		1.65	V	EDGE transmit
VRAMP Capacitance			10	pF	DC to 200kHz
VRAMP Current			10	µA	
Supply Voltage, VIO	1.65	1.8	2.0	V	MIPI RFFE Supply Voltage
MIPI RFFE logic low (SCLK, SDATA)	0		0.3*VIO	V	
MIPI RFFE logic high (SCLK, SDATA)	0.7*VIO		VIO	V	
VIO Rise Time			450	µs	Required for device reset
Control Current (MIPI Digital Inputs)			50	µA	
Turn-on Time			20	µs	Refer to Timing Diagram
Switching Speed		2	5	µs	Port to Port
RF Port Impedance		50		Ω	Pins 2, 3 and all RF ports listed in Pin Description Table

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Power vs Modulation Table

Power vs Modulation Table				GSM / EDGE	TD-SCDMA	LTE			
						Modulation: QPSK		Modulation: 16QAM	
Band	Port	Freq (Start)	Freq (Stop)	Pout	TDS	5 MHz / 8 RB 10 MHz / 12 RB 20 MHz / 18 RB	5 MHz / 25 RB 10 MHz / 50 RB 20 MHz / 100 RB	5 MHz / 8 RB 10 MHz / 12 RB 20 MHz / 18 RB	5 MHz / 25 RB 10 MHz / 50 RB 20 MHz / 100 RB
GSM 850	ANT_L	824	849	34.5	NA	NA			
GSM 900	ANT_L	880	915	34.5	NA	NA			
GSM DCS	ANT_M	1710	1785	32.5	NA	NA			
GSM PCS	ANT_M	1850	1910	32.5	NA	NA			
EDGE 850	ANT_L	824	849	28.5	NA	NA			
EDGE 900	ANT_L	880	915	28.5	NA	NA			
EDGE DCS	ANT_M	1710	1785	28.5	NA	NA			
EDGE PCS	ANT_M	1850	1910	28.5	NA	NA			
34	ANT_M	2010	2025	NA	27.0	26.0	25.0	24.0	23.0
39	ANT_M	1880	1920	NA	27.0	26.0	25.0	24.0	23.0

Electrical Specifications: GSM Low Band_Vramp Power Control

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.5V, Pout = 34.5 dBm, T_A=+25°C, GMSK Modulation, Duty Cycle = 25%, Period = 4.6ms.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	GSM800 Band	824		849	MHz
	GSM900 Band	880		915	MHz
Input VSWR	5dBm ≤ P_{OUT} ≤ 34.5 dBm		1.5	2.5	X:1
RF Input Power (P_{IN})		-1	3	6	dBm
RF Output Power (P_{OUT}) Maximum	Vbatt =3.5V; P_{IN}=6dBm; T_A=+25°C, Vramp = 1.65V	34.5	35.25		dBm
Supply Current	Pout = 34.5 dBm, Frequency = 824-849MHz		2175		mA
	Pout = 34.5 dBm, Frequency = 880-915MHz		2160		mA
Efficiency (PAE)	Pout = 34.5 dBm, Frequency = 824-849MHz		35.2		%
	Pout = 34.5 dBm, Frequency = 880-915MHz		36.0		%
Harmonic Peak, 2fo	Pout = 34.5 dBm		-45	-36	dBm
Harmonic Peak, 3fo			-49	-36	dBm
Harmonic Peak, 4fo to 12.75GHz			-54	-36	dBm
Forward Isolation, PA off	P_{IN}=6dBm; VRAMP=0.16V		-67	-45	dBm
Noise Power 736MHz to 757MHz	VRAMP adjusted for P_{OUT}=34.5 dBm; RBW=100kHz		-90	-82	dBm/100KHz
Noise Power 757MHz to 763MHz			-90	-76	dBm/100KHz
Noise Power 869MHz to 894MHz			-88	-82	dBm/100KHz
Noise Power 925MHz to 935MHz			-88	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-89	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-115	-74	dBm/100KHz
Noise Power 1930MHz to 1990MHz			-115	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	5dBm ≤ P_{OUT} ≤ 34.5 dBm; RBW=1 Hz		-164	-146	dBm/Hz
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles VRAMP adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; P_{IN}=-1dBm to 6dBm, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 20:1	VSWR=20:1; all phase angles VRAMP adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; P_{IN}=-1dBm to 6dBm, T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: GSM Low Band_Pin Power Control

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Vramp = NA, Pout = 34.5 dBm, T_A=+25°C, GMSK Modulation, Duty Cycle = 25%, Period = 4.6ms.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	GSM800 Band	824		849	MHz
	GSM900 Band	880		915	MHz
Input VSWR	5dBm ≤ P_{OUT} ≤ 34.5 dBm		1.5	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		34.5	35.25		dBm
Gain	HPM, Pout = 34.5 dBm		37.3		dB
	LPM, Pout = 13 dBm		27.3		dB
Supply Current	HPM, Pout = 34.5 dBm		2070		mA
Efficiency (PAE)	HPM, Pout = 34.5 dBm		39		%
Harmonic Peak, 2fo	f=824 – 849, HPM, Pout = 34.5 dBm		-42	-33	dBm
	f=880 – 915, HPM, Pout = 34.5 dBm		-48	-36	dBm
Harmonic Peak, 3fo	HPM, Pout = 34.5 dBm		-45	-36	dBm
Harmonic Peak, 4fo to 12.75GHz			-56	-36	dBm
Forward Isolation, PA off	P_{IN}=6dBm		-78	-45	dBm
Noise Power 736MHz to 757MHz	Pin adjusted for P_{OUT}=34.5 dBm; RBW=100kHz		-82.5	-81	dBm/100KHz
Noise Power 757MHz to 763MHz			-82.8	-76	dBm/100KHz
Noise Power 869MHz to 894MHz			-82.0	-79	dBm/100KHz
Noise Power 925MHz to 935MHz			-82.0	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-82.6	-79	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-115	-74	dBm/100KHz
Noise Power 1930MHz to 1990MHz			-114	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	5dBm ≤ P_{OUT} ≤ 34.5 dBm; RBW=1 Hz		-164	-146	dBm/Hz
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 20:1	VSWR=20:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: EDGE Low Band

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Pout = 28.5 dBm, T_A=+25°C, 8PSK Modulation.

Vramp Control

Vramp adjusted for Pout. Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Pin Control

Pin adjusted for Pout, Vramp Disabled, Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	GSM800 Band	824		849	MHz
	GSM900 Band	880		915	MHz
Input VSWR			1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		28.5			dBm
Gain	HPM, Pout = 28.5 dBm		29.5		dB
	LPM, Pout = 13 dBm		28		dB
Supply Current	HPM, Pout = 28.5 dBm		1110		mA
Efficiency (PAE)	HPM, Pout = 28.5 dBm		17.5		%
Modulation Spectrum 200kHz offset	P_{OUT}=28.5dBm		-33	-30	dBc
Modulation Spectrum 400kHz offset			-61	-57	dBc
Modulation Spectrum 600kHz offset			-73	-63	dBc
EVM RMS	P_{OUT}=28.5dBm		3.5	4.5	%
Noise Power 736MHz to 757MHz	5dBm ≤ P_{OUT} ≤ 28.5dBm; RBW=100kHz		-86.5	-82	dBm/100KHz
Noise Power 757MHz to 763MHz			-86.4	-76	dBm/100KHz
Noise Power 869MHz to 894MHz			-85.7	-82	dBm/100KHz
Noise Power 925MHz to 935MHz			-86.0	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-86.0	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-115	-74	dBm/100KHz
Noise Power 1930MHz to 1990MHz			-115	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	5dBm ≤ P_{OUT} ≤ 28.5dBm; RBW=1 Hz		-164	-146	dBm/Hz
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles. Pin Adjusted for Prated into 50 Ω Load, Vcc=3.1V to 4.8V, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 20:1	VSWR=20:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: GSM Mid Band_Vramp Control

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.5V, Pout = 32.5 dBm, T_A=+25°C, GMSK Modulation, Duty Cycle=25%,Period=4.6ms.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	DCS1800 Band	1710		1785	MHz
	PCS1900 Band	1850		1910	MHz
Input VSWR	5dBm ≤ P_{OUT} ≤ 32.5 dBm		1.5	2.5	X:1
RF Input Power (P_{IN})		-1	3	6	dBm
RF Output Power (P_{OUT}) Maximum	Vbatt =3.5V; P_{IN}=3dBm; T_A=+25°C,	32.5	33.5		dBm
Supply Current	1710-1910 MHz, Pout = 32.5 dBm		1475		mA
Efficiency (PAE)	1710-1910 MHz, Pout = 32.5 dBm		32.75		%
Harmonic Peak, 2fo	Pout = 32.5 dBm		-39	-33	dBm
Harmonic Peak, 3fo			-51	-36	dBm
Harmonic Peak, 4fo to 12.75GHz			-45	-36	dBm
Forward Isolation, PA off	PA OFF, P_{IN}=6dBm; VRAMP=0.16V		-52	-37	dBm
Noise Power 736MHz to 757MHz	VRAMP adjusted for Pout = 32.5 dBm, RBW=100KHz		-108	-82	dBm/ 100KHz
Noise Power 757MHz to 763MHz			-104	-76	dBm/100KHz
Noise Power 869MHz to 894MHz			-100	-82	dBm/100KHz
Noise Power 925MHz to 935MHz			-99	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-98	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-88	-74	dBm/100KHz
Noise Power 1930MHz to 1990MHz			-90	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	5dBm ≤ P_{OUT} ≤ 32.5dBm; RBW=1 Hz		-154	-146	dBm/Hz
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles VRAMP adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; P_{IN}=-1dBm to 6dBm, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 20:1	VSWR=20:1; all phase angles VRAMP adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; P_{IN}=-1dBm to 6dBm, T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: GSM Mid Band_Pin Control

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Vramp = NA, Pout = 32.5 dBm, T_A=+25°C, GMSK Modulation, Duty Cycle=25%,Period=4.6ms.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	DCS1800 Band	1710		1785	MHz
	PCS1900 Band	1850		1910	MHz
Input VSWR	5dBm ≤ P_{OUT} ≤ 32.5 dBm		1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		32.5	33		dBm
Gain DCS 1800 Band	HPM, Pout = 32.5 dBm		39		dB
	LPM, Pout = 13 dBm		31		dB
Gain PCS 1900 Band	HPM, Pout = 32.5 dBm		37		dB
	LPM, Pout = 13 dBm		30		dB
Supply Current	1710-1910 MHz, Pout = 32.5 dBm		1425		mA
Efficiency (PAE)	HPM, Pout = 32.5 dBm		34		%
Harmonic Peak, 2fo	HPM, Pout = 32.5 dBm		-41	-33	dBm
Harmonic Peak, 3fo	HPM, Pout = 32.5 dBm		-52	-36	dBm
Harmonic Peak, 4fo to 12.75GHz	HPM, Pout = 32.5 dBm		-51	-36	dBm
Forward Isolation, PA off	P_{IN}=6dBm		-76	-37	dBm
Noise Power 736MHz to 757MHz	VRAMP adjusted for Pout = 32.5 dBm, RBW=100KHz		-105	-82	dBm/ 100KHz
Noise Power 757MHz to 763MHz			-105	-76	dBm/100KHz
Noise Power 869MHz to 894MHz			-99	-82	dBm/100KHz
Noise Power 925MHz to 935MHz			-96	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-96	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-80	-74	dBm/100KHz
Noise Power 1930MHz to 1990MHz			-83	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	5dBm ≤ P_{OUT} ≤ 32.5dBm; RBW=1 Hz		-148	-146	dBm/Hz
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 20:1	VSWR=20:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: EDGE Mid Band

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Pout = 28.5 dBm, T_A=+25°C, 8PSK Modulation.

Vramp Control

Vramp adjusted for Pout. Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Pin Control

Pin adjusted for Pout, Vramp Disabled, Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	DCS1800 Band	1710		1785	MHz
	PCS1900 Band	1850		1910	MHz
Input VSWR			1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		28.5			dBm
Gain DCS 1800 Band	HPM, Pout = 28.5 dBm		32		dB
	LPM, Pout = 13 dBm		30.5		dB
Gain PCS 1900 Band	HPM, Pout = 28.5 dBm		30.5		dB
	LPM, Pout = 13 dBm		28.5		dB
Supply Current	HPM, Pout = 28.5 dBm		1065		mA
Efficiency (PAE)	HPM, Pout = 28.5 dBm		18		%
Modulation Spectrum 200kHz offset	P_{OUT}=28.5dBm		-35.5	-30	dBc
Modulation Spectrum 400kHz offset			-63	-57	dBc
Modulation Spectrum 600kHz offset			-75	-63	dBc
EVM RMS	P_{OUT}=28.5dBm		2.5	4.5	%
Noise Power 736MHz to 757MHz	5dBm ≤ P_{OUT} ≤ 28.5dBm; RBW=100kHz		-99	-82	dBm/ 100KHz
Noise Power 757MHz to 763MHz			-99	-76	dBm/100KHz
Noise Power 869MHz to 894MHz			-98	-82	dBm/100KHz
Noise Power 925MHz to 935MHz			-96	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-96	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-83	-74	dBm/100KHz
Noise Power 1930MHz to 1990MHz			-85	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	5dBm ≤ P_{OUT} ≤ 28.5dBm; RBW=1 Hz		-148	-146	dBm/Hz
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Load, Vcc=3.1V to 4.8V, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 20:1	VSWR=20:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: TD-SCDMA Band 34

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Pout = 27.0 dBm, T_A=+25°C, TD-SCDMA Modulation.

Vramp Control

Vramp adjusted for Pout. Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Pin Control

Pin adjusted for Pout, Vramp Disabled, Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	Band 34	2010		2025	MHz
Input VSWR			1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		27			dBm
Gain	HPM, Pout = 27 dBm		27.5		dB
	LPM, Pout = -5 dBm		21		dB
Supply Current	HPM, Pout = 27 dBm		760		mA
	LPM, Pout = -5 dBm		75		mA
Efficiency (PAE)	HPM, Pout = 27 dBm		18.5		%
TDS ACLR1 (±1.6MHz)	HPM, Pout = 27 dBm		-42.0	-37	dBc
	LPM, Pout = -5 dBm		-47.5	-37	dBc
TDS ACLR2 (±3.2MHz)	HPM, Pout = 27 dBm		-64.0	-48	dBc
	LPM, Pout = -5 dBm		-50.0	-48	dBc
Noise Power 925MHz to 935MHz	Pout = 27 dBm, RBW=100 kHz		-95	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-95	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-80	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	Pout = 27 dBm, RBW=1 Hz		-147	-146	dBm/Hz
Harmonic Peak, 2fo	HPM, Pout = 27 dBm		-65	-36	dBm
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: TDD - LTE Band 34

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Pout = 26.0 dBm, T_A=+25°C, TDD - LTE Modulation: QPSK, 10MHz,12RB, MPR=0.

Vramp Control

Vramp adjusted for Pout. Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Pin Control

Pin adjusted for Pout, Vramp Disabled, Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	Band 34	2010		2025	MHz
Input VSWR			1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		26.0			dBm
Gain	HPM, Pout = 26 dBm		28.7		dB
	LPM, Pout = -5 dBm		19.5		dB
Supply Current	HPM, Pout = 26 dBm		685		mA
	LPM, Pout = -5 dBm		77		mA
Efficiency (PAE)	HPM, Pout = 26 dBm		16.5		%
ACLR1 – E-UTRA	HPM, Pout = 26 dBm		-40.0	-35	dBc
	LPM, Pout = -5 dBm		-39.0	-35	dBc
ACLR1 – UTRA	HPM, Pout = 26 dBm		-42.5	-38	dBc
	LPM, Pout = -5 dBm		-46.0	-38	dBc
ACLR2 – UTRA	HPM, Pout = 26 dBm		-52.5	-41	dBc
	LPM, Pout = -5 dBm		-50.0	-41	dBc
EVM RMS	HPM, Pout = 26 dBm		1.4	3.0	%
GPS Band Noise Power 1574MHz to 1576MHz	Pout = 25 dBm, 20MHz Full Resource Block (FRB) MPR 1 dB RBW=1Hz		-138	-130	dBm/Hz
GLONASS Band Noise Power 1597MHz to 1605MHz			-137	-130	dBm/Hz
Harmonic Peak, 2fo	HPM, Pout = 26 dBm		-55	-36	dBm
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: TD-SCDMA Band 39

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Pout = 27.0 dBm, T_A=+25°C, TD-SCDMA Modulation.

Vramp Control

Vramp adjusted for Pout. Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Pin Control

Pin adjusted for Pout, Vramp Disabled, Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	Band 39	1880		1920	MHz
Input VSWR			1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		27			dBm
Gain	HPM, Pout = 27 dBm		29		dB
	LPM, Pout = -5 dBm		20.5		dB
Supply Current	HPM, Pout = 27 dBm		765		mA
	LPM, Pout = -5 dBm		74		mA
Efficiency (PAE)	HPM, Pout = 27 dBm		19		%
TDS ACLR1 (±1.6MHz)	HPM, Pout = 27 dBm		-43	-37	dBc
	LPM, Pout = -5 dBm		-47	-37	dBc
TDS ACLR2 (±3.2MHz)	HPM, Pout = 27 dBm		-64	-48	dBc
	LPM, Pout = -5 dBm		-50	-48	dBc
Noise Power 925MHz to 935MHz	Pout = 27 dBm, RBW=100kHz		-97.5	-70	dBm/100KHz
Noise Power 935MHz to 960MHz			-98.0	-82	dBm/100KHz
Noise Power 1805MHz to 1880MHz			-85.0	-74	dBm/100KHz
Noise Power 2400MHz to 2500MHz	Pout = 27 dBm; RBW=1 Hz		-148	-146	dBm/Hz
Harmonic Peak, 2fo	HPM, Pout = 27 dBm		-52.5	-36	dBm
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: TDD - LTE Band 39

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.6V, Pout = 26.0 dBm, T_A=+25°C, TDD - LTE Modulation: QPSK, 10MHz,12RB, MPR=0.

Vramp Control

Vramp adjusted for Pout. Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Pin Control

Pin adjusted for Pout, Vramp Disabled, Bias set through MIPI Programming.
Refer to Mode Table for detailed operating conditions and programming.

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency	Band 39	1880		1920	MHz
Input VSWR			1.7	2.5	X:1
RF Input Power (P_{IN})				6	dBm
RF Linear Output Power (P_{OUT})		26.0			dBm
Gain	HPM, Pout = 26 dBm		28.7		dB
	LPM, Pout = -5 dBm		22		dB
Supply Current	HPM, Pout = 26 dBm		675		mA
	LPM, Pout = -5 dBm		80		mA
Efficiency (PAE)	HPM, Pout = 26 dBm		17		%
ACLR1 – E-UTRA	HPM, Pout = 26 dBm		-41.8	-35	dBc
	LPM, Pout = -5 dBm		-40.0	-35	dBc
ACLR1 – UTRA	HPM, Pout = 26 dBm		-41.5	-38	dBc
	LPM, Pout = -5 dBm		-45.8	-38	dBc
ACLR2 – UTRA	HPM, Pout = 26 dBm		-51.0	-41	dBc
	LPM, Pout = -5 dBm		-49.0	-41	dBc
EVM RMS	HPM, Pout = 26 dBm		1.4	3.0	%
ISM Band Noise Power 2400MHz to 2484MHz	Pout = 25 dBm, 20MHz Full Resource Block (FRB) MPR 1 dB RBW=1Hz		-149	-146	dBm/Hz
Band 34 Noise Power 2010MHz to 2025MHz			-135	-125	dBm/Hz
Band 3 Rx Noise Power 1805MHz to 1880MHz			-130	-125	dBm/Hz
Harmonic Peak, 2fo	HPM, Pout = 26 dBm		-55	-36	dBm
Stability (Spurious), VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V, T_A= -30 to +85°C.			-36	dBm
Ruggedness, VSWR 10:1	VSWR=10:1; all phase angles Pin adjusted for Prated into 50Ω load Vcc=3.1V to 4.8V; T_A= -30 to +85°C.	No damage or permanent degradation to device.			

Note: Refer to Mode Table for futher operating conditions.

Electrical Specifications: Switch

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.5V, Pin = 6.0 dBm, T_A=+25°C, Duty Cycle = 100% (CW)

Parameter		Conditions	Min.	Typ.	Max.	Units
Insertion Loss, Includes Coupler Loss		Frequency MHz				
Low Band	ANT_L to L_TRX 1 – 7	699 – 960		0.75		dB
Mid Band	ANT_M to M_TRX 1 – 5	1400 – 1700		0.70		dB
Mid Band	ANT_M to M_TRX 1 – 5	1700 – 2200		0.95		dB
High Band	ANT_H to H_TRX 1 – 4	1400 – 1700		0.80		dB
High Band	ANT_H to H_TRX 1 – 4	1700 – 2200		1.1		dB
High Band	ANT_H to H_TRX 1 – 4	2300 – 2700		1.1		dB
High Band	ANT_H to H_TRX 1 – 4	2496 – 2690		1.1		dB
Band 41	ANT_H to H_TRX 2	2496 – 2690 5GHz Filter Off		0.8		dB
Band 41	ANT_H to H_TRX 1 – 4	2496 – 2690 5GHz Filter On *Note 1		1.1		dB
High Band	ANT_H to H_TRX 1 – 4	3400 – 3800		1.4		dB
High Band	ANT_H to H_TRX 1 – 4	5150 – 5850		1.4		dB

Note 1: The 5 GHz Filter provides additional TRx attenuation for LTE and WiFi co-existence.
Refer to MIPI Programing Section for Register 6 Settings.

Coupling Ratio: Measurement from TRx to the coupled antenna port

Parameter	Conditions	Min.	Typ.	Max.	Units
Low Band	Freq = 699 – 960 MHz	20	23.5		dB
Mid Band	Freq = 1400 – 2200 MHz	19	21		dB
High band	Freq = 1400 – 3800 MHz	18	22		dB

Isolation: Measurement from Antenna to Coupler Port

Parameter	Conditions	Min.	Typ.	Max.	Units
Low Band	Freq = 699 – 960 MHz	40	44		dB
Mid Band	Freq = 1400 – 2200 MHz	40	45		dB
High band	Freq = 1400 – 3800 MHz	40	47		dB

Return Loss

Parameter	Conditions	Min.	Typ.	Max.	Units
Low Band	Freq = 699 – 960 MHz	10	20		dB
Mid Band	Freq = 1400 – 2200 MHz	7	15		dB
High band	Freq = 1400 – 3800 MHz	5	10		dB

Isolation TRx to TRx

Band	Parameter	Conditions	Min.	Typ.	Max.	Units
Low Band	L_TRx 1 to L_TRx 2	Freq = 699 – 960 MHz	27.5	31.1		dB
	L_TRx 2 to L_TRx 3		28.5	31.2		dB
	L_TRx 3 to L_TRx 4		27.5	30.3		dB
	L_TRx 4 to L_TRx 5		28.0	30.9		dB
	L_TRx 5 to L_TRx 6		29.5	32.9		dB
	L_TRx 6 to L_TRx 7		28.5	31.3		dB
	L_TRx 7 to L_TRx 6		29.0	31.6		dB
Mid Band	M_TRx 1 to M_TRx 2	Freq = 1400 – 2300 MHz	24.0	29.0		dB
	M_TRx 2 to M_TRx 3		27.0	30.8		dB
	M_TRx 3 to M_TRx 4		24.0	28.0		dB
	M_TRx 4 to M_TRx 5		18.5	22.2		dB
	M_TRx 5 to M_TRx 4		19.0	23.0		dB
High Band	H_TRx 1 to H_TRx 2	Freq = 2300 - 2690	20.0	22.4		dB
	H_TRx 2 to H_TRx 3		19.0	21.0		dB
	H_TRx 3 to H_TRx 4		20.0	22.7		dB
	H_TRx 4 to H_TRx 3		21.0	22.9		dB

Electrical Specifications: Switch

Nominal test conditions unless otherwise stated, all unused ports terminated in 50 Ω.
Vcc = Vbatt = +3.5V, T_A=+25°C, Duty Cycle = 100% (CW)

Parameter	Conditions	Min.	Typ.	Max.	Units
B13 2nd harmonics in L_TRX	Pin=25dBm, GPS		-90	-74	dBm
B8 2nd harmonics in L_TRX	Pin=25dBm, B3/B8 CA		-92	-84	dBm
B8 3rd harmonics in L_TRX	Pin=25dBm, B7/B8 CA		-106	-95	dBm
B26 3rd harmonics in L_TRX	Pin=25dBm, B41/B26 CA		-102	-95	dBm
B12/B17 3rd harmonics in L_TRX	Pin=25dBm, B4/B17(12) CA		-95	-90	dBm
B3 2nd harmonics in M_TRX	Pin=25dBm, B3/B42 CA		-96	-90	dBm
B2 3rd harmonics in M_TRX	Pin=25dBm, B2/B255 CA		-118	-95	dBm
B4 3rd harmonics in M_TRX	Pin=25dBm, B4/B252 CA		-111	-95	dBm
LB TRX 2nd harmonics	Pin=26dBm, Frequency = 699-915MHz, except for non-harmonics band		-92	-60	dBm
LB TRX 3rd harmonics	Pin=26dBm, Frequency = 699-915MHz, except for non-harmonics band		-101	-60	dBm
MB/HB TRX 2nd harmonics	Pin=26dBm, Frequency = 1427-3800MHz		-97	-60	dBm
MB/HB TRX 3rd harmonics	Pin=26dBm, Frequency = 1427-3800MHz		-93	-60	dBm
Linearity: IMD2	Tx Freq = 897.5MHz, (+23dBm) Blocker Frequency = 1840 MHz (-15dBm)		-128	-105	dBm
Linearity IMD3	Tx Freq = 897.5MHz, (+23dBm) Blocker Frequency = 852 MHz (-15dBm)		-130	-105	dBm
Triple Beat Ratio	TX1=TX2= +21.5dBm, Blocker = -30dBm, Freq = 699 to 915 MHz, 1710 to 2155 MHz	81	103		dBc
Linearity: MB + MB FDD UL CA IMD3 (B2 + B4)	B2 TX=22.5dBm (1860MHz, 20MHz) B4 TX= 10dBm (1752.5MHz, 5MHz) Measure 1940MHz, 20MHz		-109	-95	dBm
Linearity: MB + MB FDD UL CA IMD5 (B2 + B4)	B2 TX=10dBm (1868.3MHz, 5MHz) B4 TX= 22.5dBm (1735MHz, 5MHz) Measure 2135MHz, 5MHz		-140	-105	dBm

MIPI Programming Guide:

The CMOS controller supports both the traditional GMSK Vramp Power Control and the Pin Power Control. For the Pin Power Control the Vramp is set as a bias point along with the DAC control of Register 1. Register 1 is not used in the traditional Vramp Control.

The MIPI register settings for both are listed separately below.

Vramp Power Control Register Summary:

QM57508 RFFE Register Map Summary								
Reg Dec (Hex)	7	6	5	4	3	2	1	0
Reg 00 (0x00)	RESERVED [7] (1)	BAND_SEL [6:3] (0000)				PA_EN [2] (0)	PA_MODE [1:0] (00)	
Reg 03 (0x03)	RESERVED [7:6] (00)		HIGH_ISO [5] (0)	RESERVED [4] (0)	HB_SEL [3:0] (0000)			
Reg 04 (0x04)	RESERVED [7:5] (000)			MB_SEL [4:0] (00000)				
Reg 05 (0x05)	RESERVED [7] (0)	LB_SEL [6:0] (0000000)						
Reg 06 (0x06)	RESERVED [7] (0)	CPL2 [6:4] (000)			RESERVED [3] (0)	CPL1 [2:0] (000)		
Reg 29 (0x1D)	PRODUCT_ID [7:0] (0010 0101)							
Reg 30 (0x1E)	MANUFACTURER_ID [7:0] (0011 0100)							
Reg 31 (0x1F)	RESERVED [7] (0)	RESERVED [6] (0)	MAN_ID MSB [5:4] (01)		USID [3:0] (1111)			

Note: Reg 30 is a 10 bit register which ultilizes Reg 31 B5:4 for the Most Significant Bits (MSB)

Register 00

Register Address	Data Bits	Register Name	Bit Field	Defaults	RFMD Description	R/W F/SEF	Broadcast ID support
0x00	Reg00 [7]	PA_CTRL0	VRAMP_EN	1b 0	Reserved. = 1 (Vramp Enabled)	R/W	No
0x00	Reg00 [6:3]	PA_CTRL0	BAND_SEL	4b 0000	Band Select. Selects the band and modulation of operation. 0000: TX_OFF 0001: TX_LB_GSM 0010: TX_MB_GSM 0101: TX_LB_EDGE 0110: TX_MB_EDGE 0111: TX_MB_TDSCDMA_TDDLTE	R/W	No
0x00	Reg00 [2]	PA_CTRL0	PA_EN	1b 0	Enables GSM PA Bias 0 = DISABLED 1 = ENABLED	R/W	No
0x00	Reg00 [1:0]	PA_CTRL0	MODE	2b 00	PA Mode. 01 = LPM 11 = HPM	R/W	No

Register 03

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x03	Reg03[7:6]	SW_Ctrl1	RESERVED	4b0000	Reserved. = 0	R/W	No
0x03	Reg03[5]	SW_Ctrl1	HIGH_ISO	1b0	HB high-isolation mode 1: High-isolation mode 0: Normal mode	R/W	No
0x03	Reg03[4]	SW_Ctrl1	RESERVED	1b0	Reserved. = 0	R/W	No
0x03	Reg03[3:0]	SW_Ctrl1	HB_SEL [3:0]	4b0000	Each bit controls one of four RF paths to be connected to the HB antenna. Multiple bits can be enabled at the same time. 1000: HB_TRX4 0100: HB_TRX3 0010: HB_TRX2 0001: HB_TRX1 0000: No HB connection	R/W	No

Register 04

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x04	Reg04[7:5]	SW_Ctrl2	RESERVED	3b000	Reserved. = 0	R/W	No
0x04	Reg04[4:0]	SW_Ctrl2	MB_SEL	5b00000	Each bit controls one of five RF paths to be connected to the MB antenna. Multiple bits can be enabled at the same time. 10000: MB_TRX5 01000: MB_TRX4 00100: MB_TRX3 00010: MB_TRX2 00001: MB_TRX1 00000: No MB connection	R/W	No

Register 05

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x05	Reg05[7]	SW_Ctrl3	RESERVED3	1b0	Reserved. = 0	R/W	No
0x05	Reg05[6:0]	SW_Ctrl3	LB_SEL	7b0000000	Each bit controls one of seven RF paths to be connected to the LB antenna. Multiple bits can be enabled at the same time. 1000000: LB_TRX7 0100000: LB_TRX6 0010000: LB_TRX5 0001000: LB_TRX4 0000100: LB_TRX3 0000010: LB_TRX2 0000001: LB_TRX1 0000000: No LB connection	R/W	No

Register 06

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	CPL Mode	Freq	HB Filter	R/W F/SEF	Broadcast ID
0x06	Reg06 [7]	SW_Ctrl4	RESERVED	1b 0	Reserved. = 0	NA	NA	NA	R/W	No
0x06	Reg06 [6:4]	SW_Ctrl4	CPL2	3b 000	111: VHB 110: HB 101: MHB 100: JHB 011: MB 010: JB 001: LB 000: OFF	HB on HB CPL HB on HB CPL MB on HB CPL MB on HB CPL MB on MB CPL MB on MB CPL LB on LB CPL Coupler OFF	3.5 - 3.8GHz 2.3 - 2.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 0.7 - 0.96GHz 0.7 - 5.8 GHz	Off On On On NA NA NA Off	R/W	No
0x06	Reg06 [3]	SW_Ctrl4	RESERVED	1b 0	Reserved. = 0	NA	NA	NA	R/W	No
0x06	Reg06 [2:0]	SW_Ctrl4	CPL1	3b 000	111: VHB 110: HB 101: MHB 100: JHB 011: MB 010: JB 001: LB 000: OFF	HB on HB CPL HB on HB CPL MB on HB CPL MB on HB CPL MB on MB CPL MB on MB CPL LB on LB CPL Coupler OFF	3.5 - 3.8GHz 2.3 - 2.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 0.7 - 0.96GHz 0.7 - 5.8 GHz	Off On On On NA NA NA Off	R/W	No

Pin Power Control Register Summary:

QM57508 RFFE Register Map Summary								
Reg Dec (Hex)	7	6	5	4	3	2	1	0
Reg 00 (0x00)	RESERVED [7] (0)	BAND_SEL [6:3] (0000)				PA_EN [2] (0)	PA_MODE [1:0] (00)	
Reg 01 (0x01)	PA Bias [7:0] (0000)							
Reg 03 (0x03)	RESERVED [7:6] (00)		HIGH_ISO [5] (0)	RESERVED [4] (0)	HB_SEL [3:0] (0000)			
Reg 04 (0x04)	RESERVED [7:5] (000)			MB_SEL [4:0] (00000)				
Reg 05 (0x05)	RESERVED [7] (0)	LB_SEL [6:0] (0000000)						
Reg 06 (0x06)	RESERVED [7] (0)	CPL2 [6:4] (000)			RESERVED [3] (0)	CPL1 [2:0] (000)		
Reg 29 (0x1D)	PRODUCT_ID [7:0] (0010 0101)							
Reg 30 (0x1E)	MANUFACTURER_ID [7:0] (0011 0100)							
Reg 31 (0x1F)	RESERVED [7] (0)	RESERVED [6] (0)	MAN_ID MSB [5:4] (01)		USID [3:0] (1111)			

Note: Reg 30 is a 10 bit register which ultilizes Reg 31 B5:4 for the Most Significant Bits (MSB)

Register 00

Register Address	Data Bits	Register Name	Bit Field	Defaults	RFMD Description	R/W F/SEF	Broadcast ID support
0x00	Reg00[7]	PA_CTRL0	VRAMP_EN	1b0	Reserved = 0 (Vramp Disabled)	R/W	No
0x00	Reg00[6:3]	PA_CTRL0	BAND_SEL[3:0]	4b0000	Band Select Note: The TX_BYPASS (1000) works in conjunction with PA MODE (Bits1:0) when selected and PA_EN needs to be in the ENABLED State (1). 0000: TX_OFF 0011: TX_LB_GSM_LIN (High Gain) 0100: TX_MB_GSM_LIN 0101: TX_LB_EDGE / GSM_Lin (Low Gain)* 0110: TX_MB_EDGE 0111: TX_MB_TDSCDMA_TDDLTE 1000: TX_BYPASS 1001: TX_LB_GSM + MB_BYPASS 1010: TX_MB_GSM + LB_BYPASS 1011: TX_LB_GSM_LIN + MB_BYPASS 1100: TX_MB_GSM_LIN + LB_BYPASS 1101: TX_LB_EDGE (HPM and LPM) + MB_BYPASS 1110: TX_MB_EDGE (HPM and LPM) + LB_BYPASS 1111: TX_MB_TDSCDMA + LB BYPASS	R/W	No
0x00	Reg00[2]	PA_CTRL0	PA_EN	1b0	Enables GSM PA Bias 0 = DISABLED 1 = ENABLED	R/W	No
0x00	Reg00[1:0]	PA_CTRL0	MODE[1:0]	2b00	PA Mode. If BAND_SEL[3:0] <> 1000 10 = HPM 00 = LPM if BAND_SEL[3:0] = 1000 (direct Input Switch Control) 00 = Input Switches Off 01 = MB off (open), LB = BYPASS 10 = MB = BYPASS, LB = off (open) 11 = MB = BYPASS, LB = BYPASS	R/W	No

* LB EDGE / GSM Lin (0101) optimized for 2G performance. LB GSM Lin (0011) can be used if higher gain is required. Refer to mode table for further details.

Register 01

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x01	Reg01[7:0]	PA_BIAS1	PA_BIAS1	8b00000000	PA Biasing. ICNTL of final Stage (Vramp is disabled)	R/W	No

Register 03

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x03	Reg03[7:6]	SW_Ctrl1	RESERVED	4b0000	Reserved. = 0	R/W	No
0x03	Reg03[5]	SW_Ctrl1	HIGH_ISO	1b0	HB high-isolation mode 1: High-isolation mode 0: Normal mode	R/W	No
0x03	Reg03[4]	SW_Ctrl1	RESERVED	1b0	Reserved. = 0	R/W	No
0x03	Reg03[3:0]	SW_Ctrl1	HB_SEL	4b0000	Each bit controls one of four RF paths to be connected to the HB antenna. Multiple bits can be enabled at the same time. 1000: HB_TRX4 0100: HB_TRX3 0010: HB_TRX2 0001: HB_TRX1 0000: No HB connection	R/W	No

Register 04

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x04	Reg04[7:5]	SW_Ctrl2	RESERVED2	3b000	Reserved. = 0	R/W	No
0x04	Reg04[4:0]	SW_Ctrl2	MB_SEL	5b00000	Each bit controls one of five RF paths to be connected to the MB antenna. Multiple bits can be enabled at the same time. 10000: MB_TRX5 01000: MB_TRX4 00100: MB_TRX3 00010: MB_TRX2 00001: MB_TRX1 00000: No MB connection	R/W	No

Register 05

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	R/W F/SEF	Broadcast ID support
0x05	Reg05[7]	SW_Ctrl3	RESERVED	1b0	Reserved. = 0	R/W	No
0x05	Reg05[6:0]	SW_Ctrl3	LB_SEL	7b0000000	Each bit controls one of seven RF paths to be connected to the LB antenna. Multiple bits can be enabled at the same time. 1000000: LB_TRX7 0100000: LB_TRX6 0010000: LB_TRX5 0001000: LB_TRX4 0000100: LB_TRX3 0000010: LB_TRX2 0000001: LB_TRX1 0000000: No LB connection	R/W	No

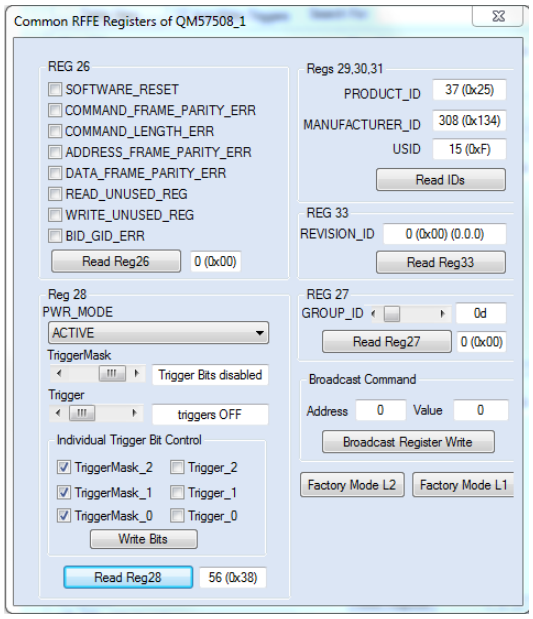
Register 06

Register Address	Data Bits	Register Name	Bit Field	Defaults	Description	CPL Mode	Freq	HB Filter	R/W F/SEF	Broadcast ID
0x06	Reg06 [7]	SW_Ctrl4	RESERVED	1b 0	Reserved. = 0	NA	NA	NA	R/W	No
0x06	Reg06 [6:4]	SW_Ctrl4	CPL2	3b 000	111: VHB 110: HB 101: MHB 100: JHB 011: MB 010: JB 001: LB 000: OFF	HB on HB CPL HB on HB CPL MB on HB CPL MB on HB CPL MB on MB CPL MB on MB CPL LB on LB CPL Coupler OFF	3.5 - 3.8GHz 2.3 - 2.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 0.7 - 0.96GHz 0.7 - 5.8 GHz	Off On On On NA NA NA Off	R/W	No
0x06	Reg06 [3]	SW_Ctrl4	RESERVED	1b 0	Reserved. = 0	NA	NA	NA	R/W	No
0x06	Reg06 [2:0]	SW_Ctrl4	CPL1	3b 000	111: VHB 110: HB 101: MHB 100: JHB 011: MB 010: JB 001: LB 000: OFF	HB on HB CPL HB on HB CPL MB on HB CPL MB on HB CPL MB on MB CPL MB on MB CPL LB on LB CPL Coupler OFF	3.5 - 3.8GHz 2.3 - 2.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 1.7 - 2.2GHz 1.4 - 1.7GHz 0.7 - 0.96GHz 0.7 - 5.8 GHz	Off On On On NA NA NA Off	R/W	No

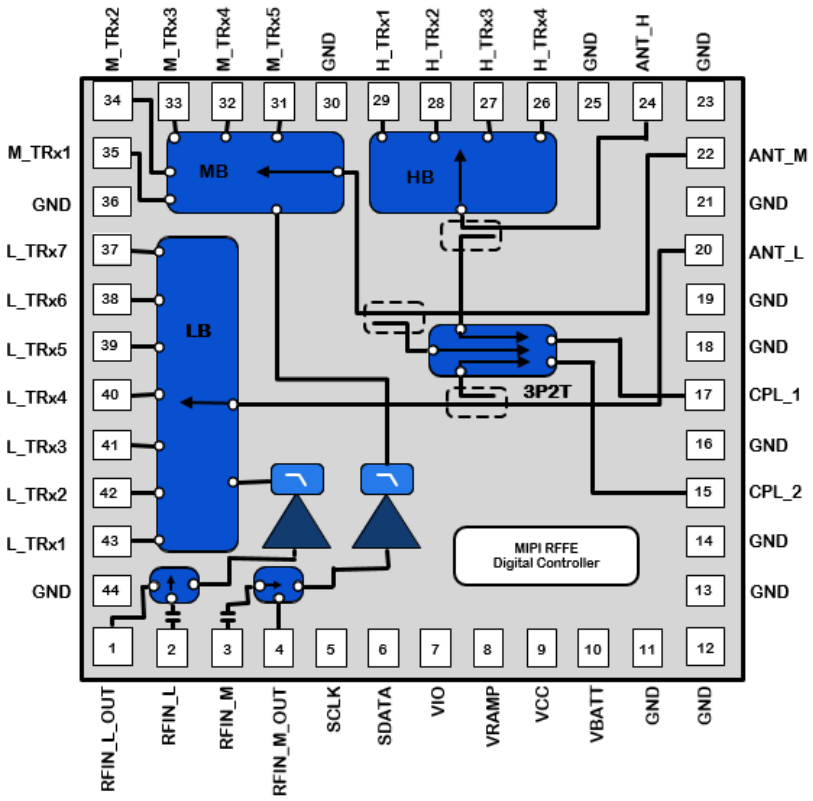
Common to both Vramp and Pin Power Control:
Product Information: Registers 29, 30, 31

Register Address	Data Bits	Register Name	Bit Field	Defaults	RFMD Description	R/W F/SEF	Broadcast ID support
0x1D	Reg29 [7:0]	PRODUCT_ID	PRODUCT_ID	8b 0010_0101	Identifies type of device. (PA, Sw, etc.) Product ID: Dec = 37 Hex = 25 Bin = 0010 0101 This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value. Refer to MIPI Alliance Specification for RFFE Sequence	R	No
0x1E	Reg30 [7:0]	MANUFACTURER_ID	MANUFACTURER_ID	8b 0011_0100	Identifies vendor. Man ID: This value is a 10 bit register consisting of 8 bits in Reg 30 and bits [5:4] in Reg 31. Refer to note below.	R	No
0x1F	Reg31 [7:6]	SPARE MANUFACTURER_ID	RESERVED	2b 00	This is a read-only bit that is reserved and yields a value of 0 at readback.	R	No
0x1F	Reg31[5:4]	SPARE MANUFACTURER_ID	MANUFACTURER_ID (MSB)	2b 01	Reg 31 bits [5:4] contain the Most Significant Bits (MSB) for the manufacturer ID. Refer to note below.	R	No
0x1F	Reg31[3:0]	SPARE MANUFACTURER_ID	USID	4b 1111	Address to program part. USID: Dec = 15 Hex = 0F Bin = 1111	RW	No

Note: In Qorvo's Optimizer Tool the registers will show the combined value for the 10 bit manufacturing ID. (Dec = 308, Bin = 01 0011 0100)



Pin Configuration and Description



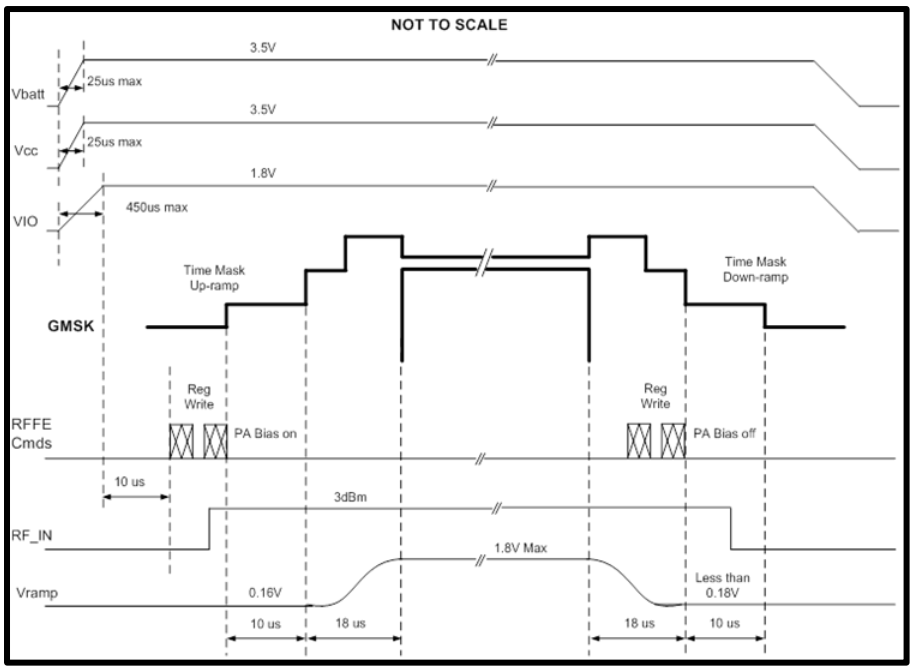
Top View

Pin Number	Label	Description
1	RFIN_L_OUT	RFIN_L Bypass
2	RFIN_L	RF input to the GSM850/EGSM900 bands. This is a 50 Ω, DC Blocked input.
3	RFIN_M	RF input to the DCS1800/PCS1900 bands. This is a 50Ω, DC Blocked input, but will measure as a short to ground.
4	RFIN_M_OUT	RFIN_M Bypass
5	SCLK	Serial interface clock input signal.
6	SDATA	Serial interface data I/O signal.
7	VIO	Supply voltage for the MIPI RFFE serial interface.
8	VRAMP	Power control signal from DAC. A simple RC filter is integrated and may not require additional filtering depending on the baseband selected.
9	VCC	Main DC power supply for the power amplifier circuitry in the module. Traces running to this pin will have high current pulses during transmit operation. Proper decoupling and routing to handle this condition should be observed.
10	VBATT	Supply voltage for bias circuitry.
11,12,13,14	GND	Pin connected to module ground.
15	CPL_2	Coupler output port.
16	GND	Pin connected to module ground.
17	CPL_1	Coupler output port.

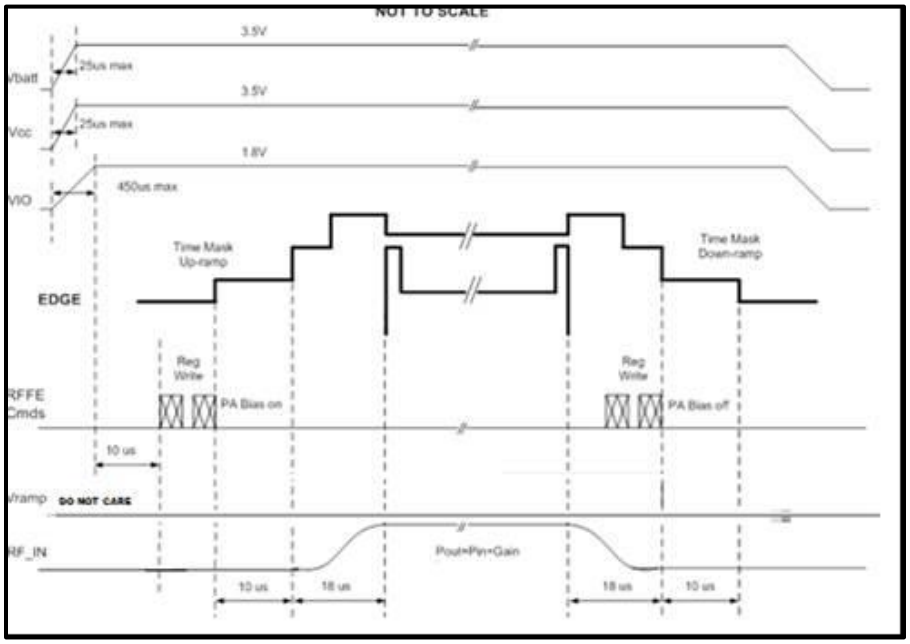
Pin Number	Label	Description
18,19	GND	Pin connected to module ground.
20	ANT_L	Bidirectional RF port. This is the common port of the antenna switch. An inductor makes this port appear as a DC short to ground. Optimized for low band frequencies.
21	GND	Pin connected to module ground.
22	ANT_M	Bidirectional RF port. This is the common port of the antenna switch. An inductor makes this port appear as a DC short to ground. Optimized for mid band frequencies.
23	GND	Pin connected to module ground.
24	ANT_H	Bidirectional RF port. This is the common port of the antenna switch. An inductor makes this port appear as a DC short to ground. Optimized for high band frequencies.
25	GND	Pin connected to module ground.
26	H_TRX4	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB and HB.
27	H_TRX3	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB and HB.
28	H_TRX2	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB and HB.
29	H_TRX1	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB and HB.
30	GND	Pin connected to module ground.
31	M_TRX5	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB.
32	M_TRX4	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB.
33	M_TRX3	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB.
34	M_TRX2	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB.
35	M_TRX1	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for MB.
36	GND	Pin connected to module ground.
37	L_TRX7	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
38	L_TRX6	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
39	L_TRX5	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
40	L_TRX4	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
41	L_TRX3	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
42	L_TRX2	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
43	L_TRX1	Interchangeable GSM/EDGE/UMTS/LTE port. External circuitry must maintain zero volts on this port. Optimized for LB.
44	GND	Pin connected to module ground.

Timing Diagram

GSM Transmit



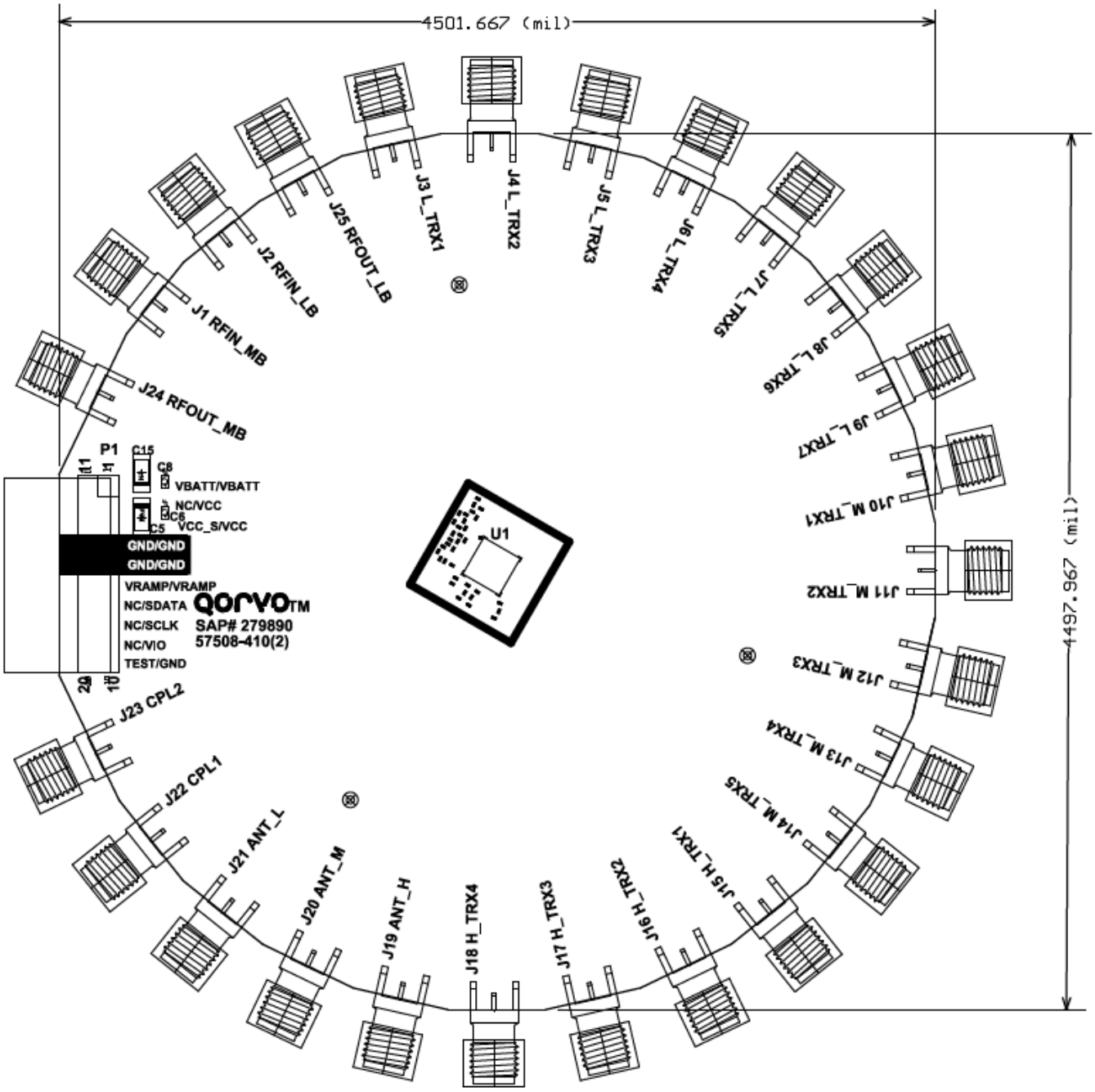
EDGE Transmit



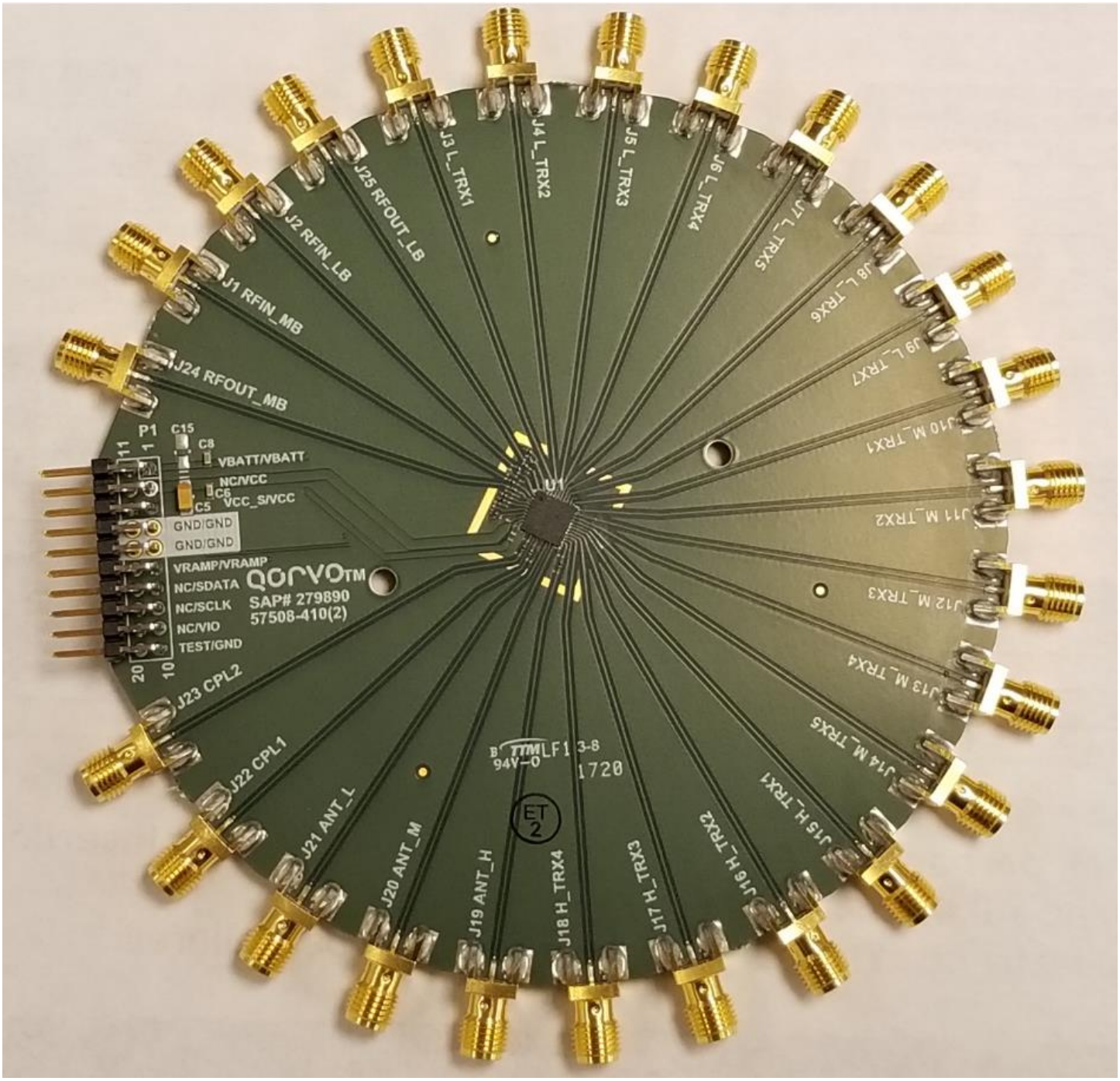
Note: Vramp (Do Not Care) for Linear Operation Only, Refer to Mode table for Vramp operation.

For Switch Turn On allow 10 uS after MIPI command execution.

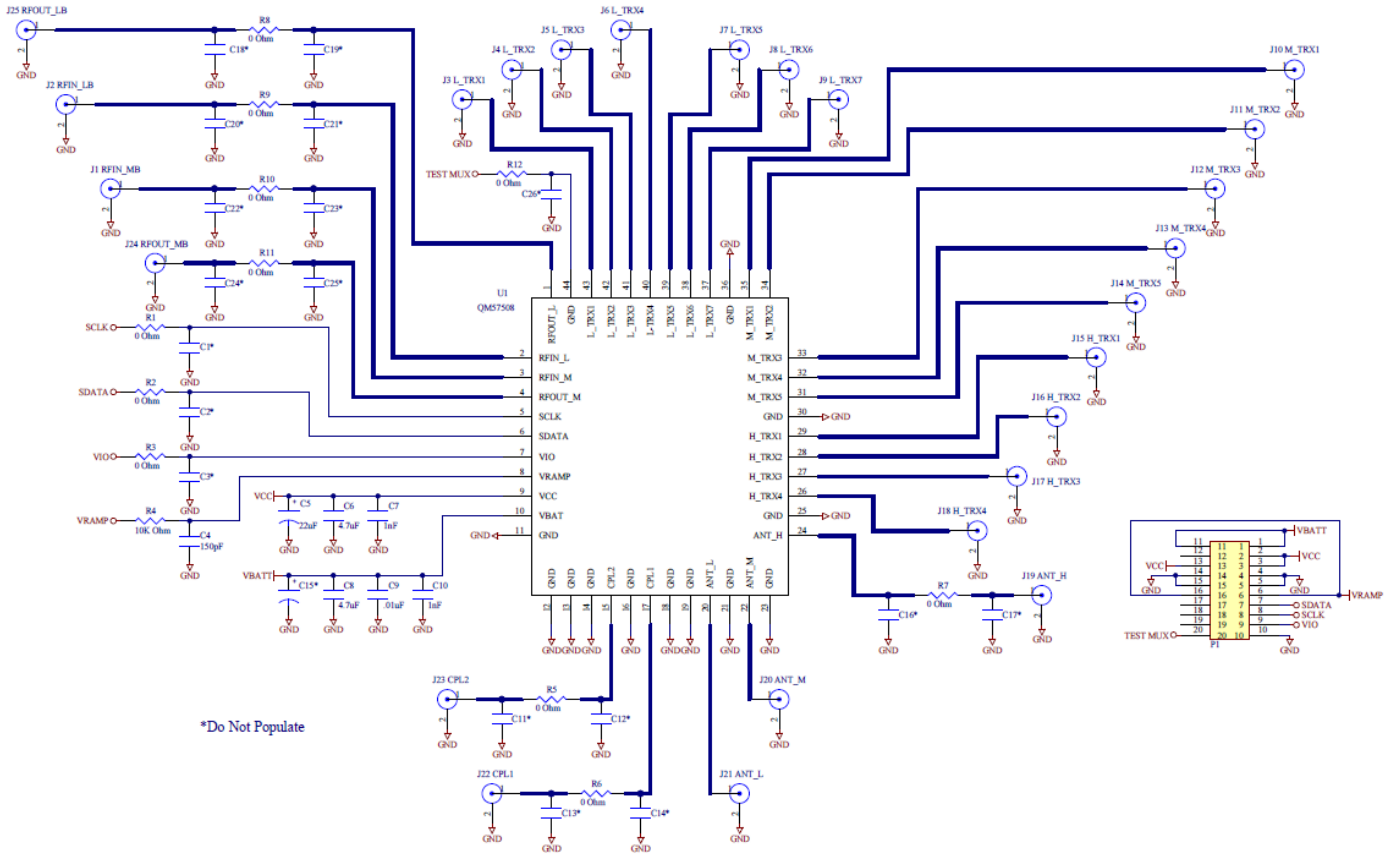
Evaluation Board Drawing



Evaluation Board Picture



Evaluation Board Schematic

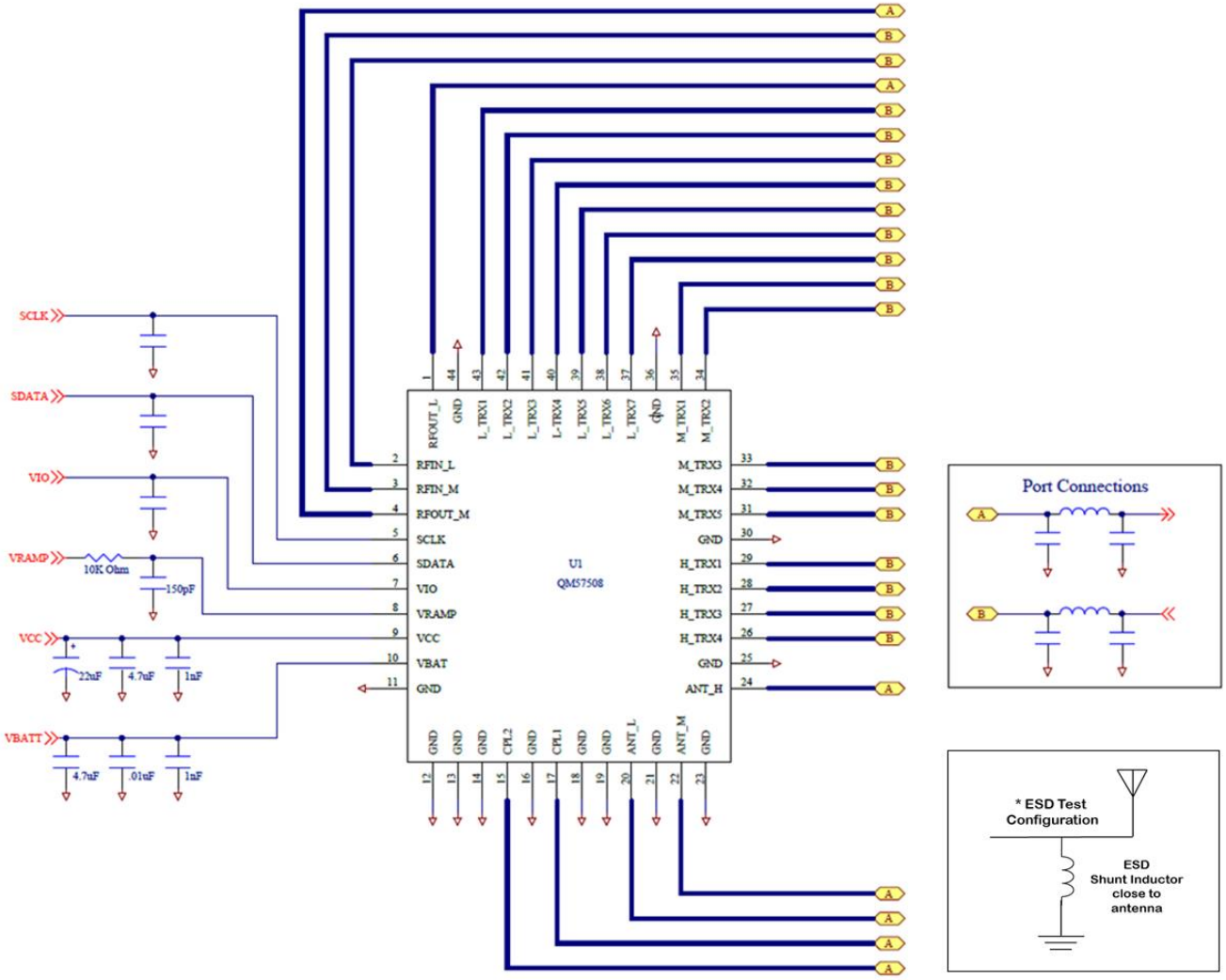


Note: Pin 1 and 4 on block diagram are shown as ground. On EVB, pin1 = J25 RFout_LB and pin 4 = J24 RFout_MB. These pins should be grounded and the EVB was designed for others possible options.

Evaluation Board Bill of Materials (BOM)

Description	Reference Designator	Manufacturer	Manufacturer's P/N
RES, 0 OHM, 1%, 1/20W, 0201	R1, R2, R3	Kamaya, Inc	RMC1/16SJPTH
RES, 10K, 5%, 1/20W, 0201	R4		PFR03S-103-JNH
RES, 0 OHM, 1/20W, 0201	R5, R6, R7, R8, R9, R10, R11, R12	Yageo USA	RC0201FR-070RL
Do Not Populate	C11*, C12*, C13*, C14*, C15*, C16*, C17*, C18*, C19*, C20*, C21*, C22*, C23*, C24*, C25*, C26*		
Do Not Populate	C1, C2, C3		
CAP, 150pF, 10%, 16V, X7R, 0201	C4	Taiyo Yuden (USA), Inc.	EMK063B7151KP-F
CAP, 22uF, 10%, 10V, TANT-A	C5	AVX/KYOCERA ASIA LTD.	TAJA226K010RNJ
CAP, 4.7uF, 10%, 6.3V, X5R, 0603	C6, C8	Murata Electronics	GRM188R60J475KE19D
CAP, 1000pF, 10%, 16V, X7R, 0201	C7, C10	AVX/KYOCERA ASIA LTD.	0201YC102KAT2A
CAP, 10000pF, 10%, 10V, X5R, 0201	C9	AVX/KYOCERA ASIA LTD.	0201ZD103KAT2A
CONN, HDR, ST, 2x10, 0.100"	P1	SAMTEC INC.	TSW-110-07-G-D
CONN, SMA, EL FLT VIPER, MAT-21-1038	J1 thru J25	Amphenol RF Asia Corp	901-10425
DUT	U1*	Qorvo	QM57508
QM57508 EVB PCB	N/A	Marcel Electronics International	279890

Application Schematic



All outputs labeld as A connections, all inputs are labeled as B connections.

For all connections it is recommended that a pi-network placeholder be in place for initial evaluation.

The MIPI lines (SCLK, SDATA, and VIO) do have internal filtering but recommend place holders for initial evaluation.

The Vbatt_Vcc connection should be made as close to the source as possible with separate traces using a star routing configuration.

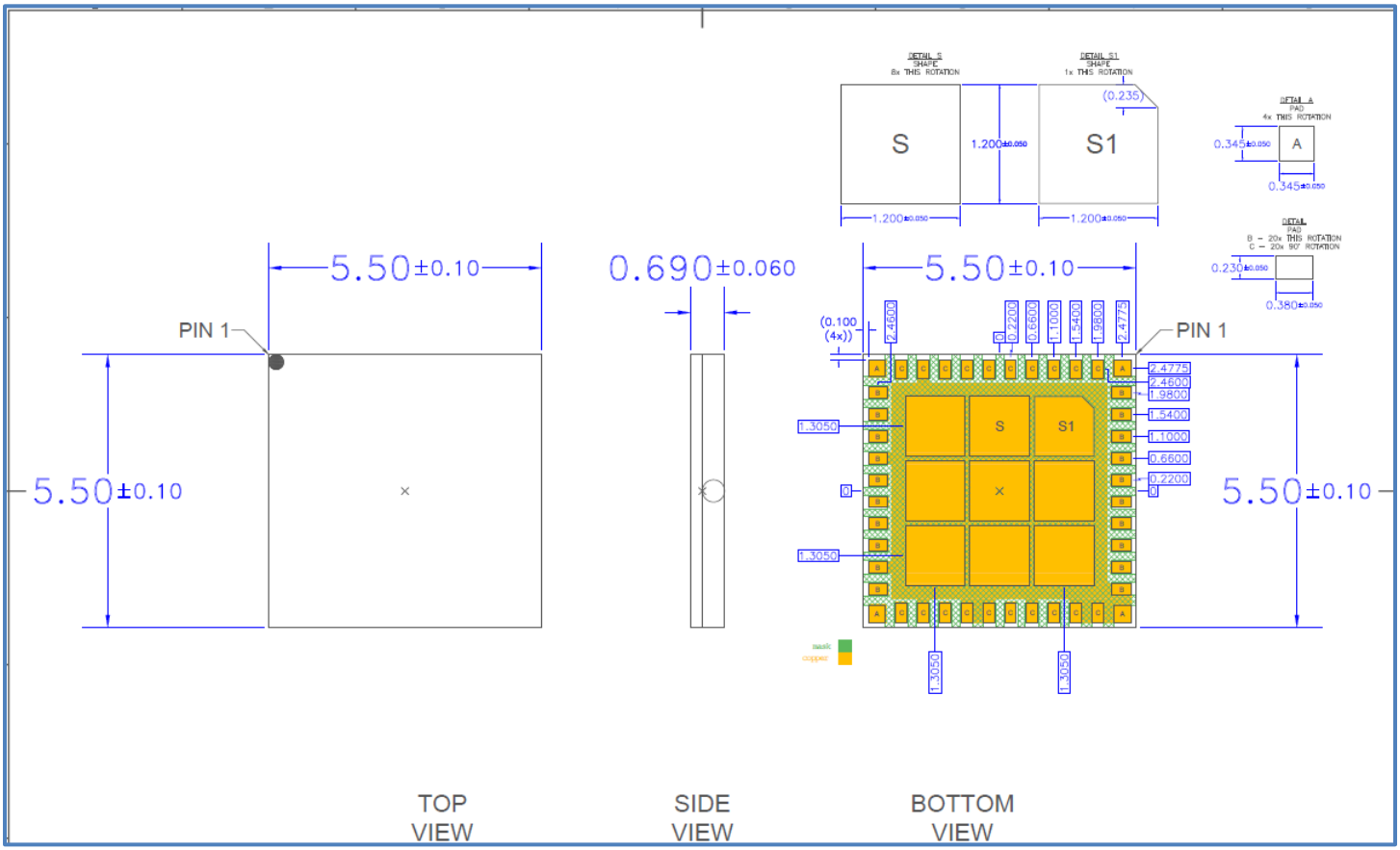
Bypass capacitors should be placed as close to the DUT as possible. The capacitor values for Vcc and Vbatt are suggested based on the EVB layout. They may require additional evaluation depending on specific parasitics of the application circuit board.

System level ESD test passed 8kV on the 57508-evaluation board per IEC 61000-4-2 requirements.

* Shunt inductors values placed on EVB for ESD testing: Low Band_22nH, Mid Band_22nH, High Band_15nH.

Package Outline and Branding Drawing

Dimensions in millimeters



PCB Design Guidelines

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 2 to 5 µinch gold over 180 µinch nickel.

Solderability

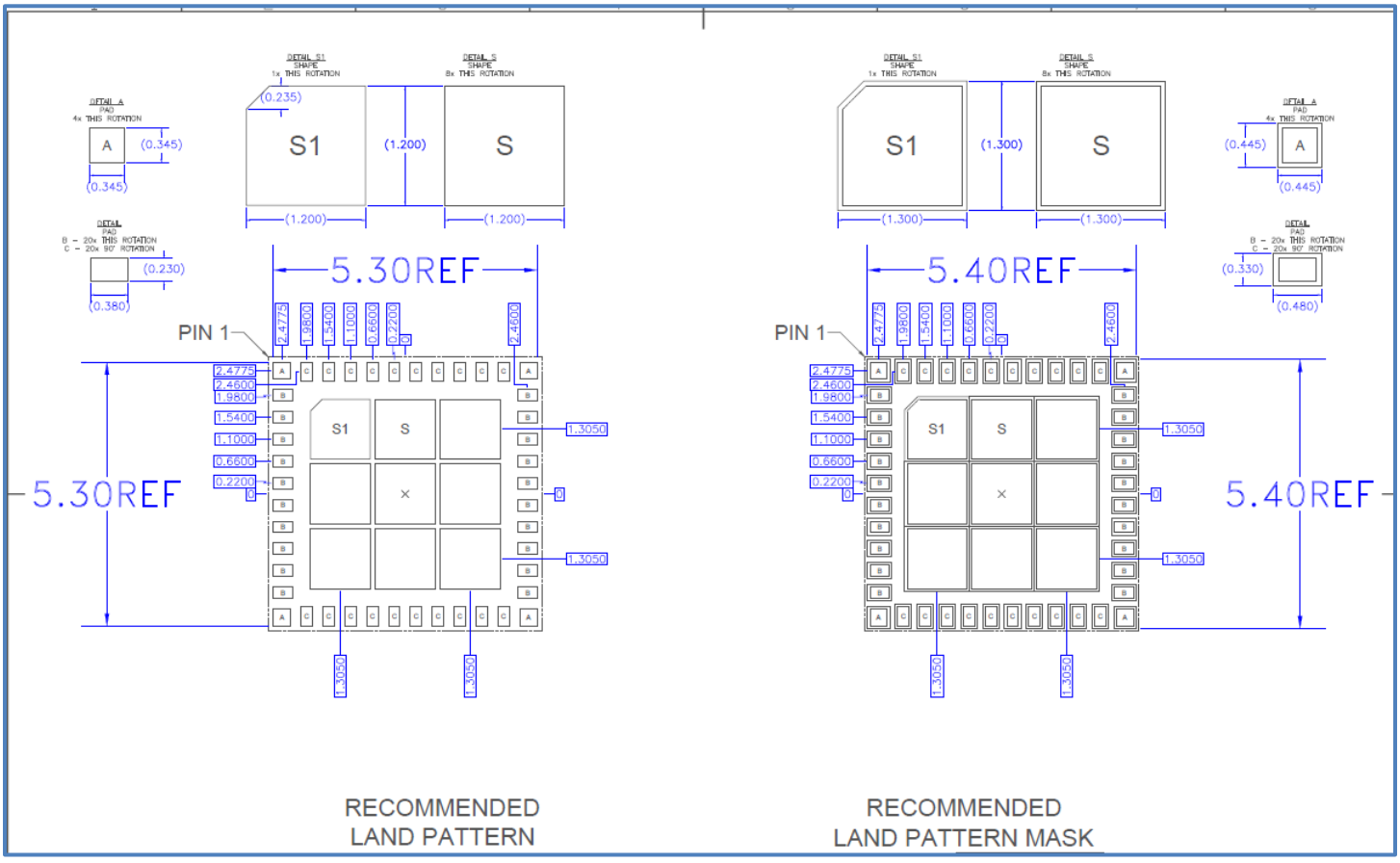
Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

PCB Land Pattern

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ANSI/ESDA/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	ANSI/ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

Revision	Date	Description
MP	7/27/2017	QM57508 Data Sheet Mass Production – J.Mickler
MP	10/02/2017	Correction to GSM Low Band Pin Power Control, Typ value is 35.25 not 34.25 dBm. Added note to EDGE Timing Diagram for Vramp Control in Pin vs Vramp Power Control Mode.
MP	10/26/2017	Correction to Ruggedness Notes Aligning VSWR
MP	11/15/2017	GSM LB Linear Mode optimized with EDGE Mode.
MP	03/04/2019	Correction to Reg 30 MIPI write.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Important Notice