QPD1025L

1800 W, 65 V, 0.96 – 1.215GHz, GaN RF Input-Matched Transistor

Product Overview

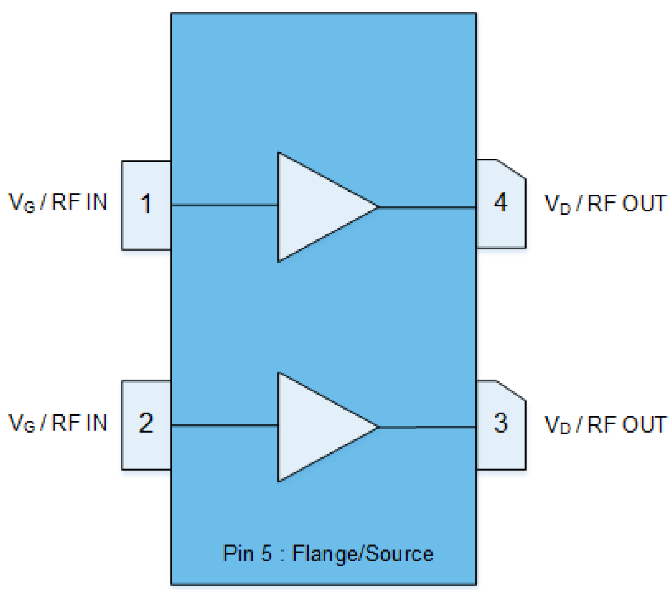
The Qorvo QPD1025L is a 1800 W (P_{3dB}) discrete GaN on SiC HEMT which operates from 0.96 to 1.215 GHz. Input pre-match within the package results in ease of external board match and saves board space. The device is in an industry standard air cavity package and is ideally suited for IFF, avionics and test instrumentation. The device can support both CW and pulsed operations.

RoHS compliant

Evaluation boards are available upon request.

4-lead NI-1230 Package (Eared)

Functional Block Diagram



Key Features

- Frequency: 0.96 to 1.215 GHz
- Output Power (P_{3dB})[1]: 1862 W
- Linear Gain[1]: 22.5 dB
- Typical PAE_{3dB}[1]: 77.2%
- Operating Voltage: 65 V
- CW and Pulse capable

Note 1: @ 1.0 GHz Load Pull

Applications

- IFF Transponders
- DME radar
- Avionics

Ordering info

Part No.	Description
QPD1025L	18 pieces of QPD1025L in 3x3 Waffle Pack
QPD1025LEVB1	1.0 – 1.1 GHz Evaluation Board
QPD1025LEVB2	0.96 – 1.215 GHz Evaluation Board
QPD1025LEVB3	913.5 – 916.5 MHz Evaluation Board

Absolute Maximum Ratings [1, 2, 3]

Parameter	Rating	Units
Breakdown Voltage, BV_{DG}	225	V
Gate Voltage Range, V_G	-7 to +2	V
Drain Current, I_{DMAX}	142	A
Power Dissipation, Pulsed, P_{DISS} [2]	1209	W
RF Input Power, Pulsed, P_{IN} [3]	46.2	dBm
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	−65 to +150	°C

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage
2. Pulsed, 100us PW, 10% DC, Package base at 85 °C
3. Pulsed, 100us PW, 10% DC, T = 25 °C

Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Operating Temp. Range	−40	+25	+85	°C
Drain Voltage Range, V_D	–	+65	+70	V
Drain Bias Current, I_{DQ}		1.5		A
Drain Current, I_D [4]	–	28	–	A
Gate Voltage, V_G [3]	–	−2.8	–	V
Power Dissipation (P_D) [2,4]	–	–	685	W
Power Dissipation (P_D), CW [2]	–	–	496	W

Notes:
1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}
4. Pulsed, 1000us PW, 20% DC

Measured Load Pull Performance – 65 V Power Tuned [1, 2]

Parameter	Typical Values				Units
Frequency, F	0.915	1.0	1.1	1.2	GHz
Output Power at 3dB compression, P_{3dB}	59.9	59.7	59.7	59.8	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	63.2	62.8	65.7	61.9	%
Gain at 3dB compression, G_{3dB}	17.9	17.5	17.3	17.2	dB

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 65 V, I_{DQ} = 750 mA (half device)
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

Measured Load Pull Performance – 65 V Efficiency Tuned [1, 2]

Parameter	Typical Values				Units
Frequency, F	0.915	1.0	1.1	1.2	GHz
Output Power at 3dB compression, P_{3dB}	57.5	57.7	58.5	58.3	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	77.6	77.2	77.0	74.6	%
Gain at 3dB compression, G_{3dB}	19.7	19.5	18.7	19.0	dB

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 65 V, I_{DQ} = 750 mA (half device)
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

Measured Load Pull Performance – 50 V Power Tuned [1, 2]

Parameter	Typical Values				Units
Frequency, F	0.915	1.0	1.1	1.2	GHz
Output Power at 3dB compression, P_{3dB}	58.9	58.6	58.5	58.6	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	66.8	60.1	66.1	62.6	%
Gain at 3dB compression, G_{3dB}	17.6	17	17	16.8	dB

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 750 mA (half device)
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

Measured Load Pull Performance – 50 V Efficiency Tuned [1, 2]

Parameter	Typical Values				Units
Frequency, F	0.915	1.0	1.1	1.2	GHz
Output Power at 3dB compression, P_{3dB}	55.2	55.6	56.5	56.8	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	78.2	74.7	76.6	71.8	%
Gain at 3dB compression, G_{3dB}	19.2	19	18.6	18.2	dB

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 750 mA (half device)
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

RF Characterization – 1.0 – 1.1 GHz EVB1 Performance at 1.05 GHz [1]

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	21.2	–	dB
Output Power at 3dB compression point, P3dB	–	1461	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	73.2	–	%
Gain at 3dB compression point, G3dB	–	18.2	–	dB
Gate Leakage VD = +10 V, VG = −3.3 V	-25 [2]	–	–	mA

Notes:
1. V_D = 65 V, I_{DQ} = 1.5 A (combined), Temp = +25 °C, Pulse Width = 100 us, Duty Cycle = 10%
2. Gate Leakage per path

RF Characterization – 0.96 – 1.215 GHz EVB2 Performance [1]

Parameter	0.96 GHz	1.08 GHz	1.2GHz	Units
Linear Gain, G_{LIN}	20	19.5	19.6	dB
Output Power at 2dB compression point, P2dB	1800	1678	1570	W
Drain Efficiency at 2dB compression point, DEFF2dB	64	68	66	%
Gain at 2dB compression point, G2dB	18	17.5	17.6	dB

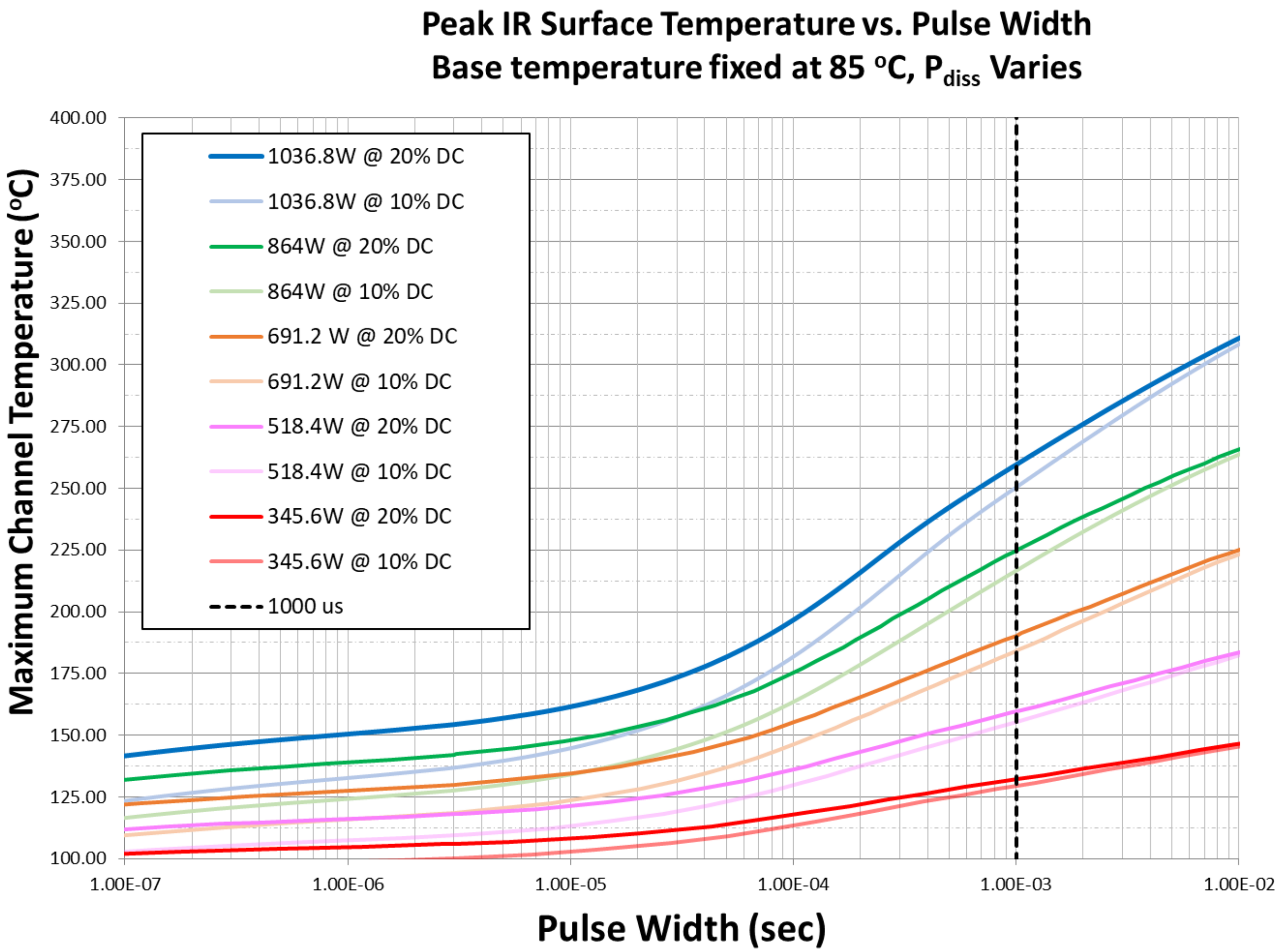
Notes:
1. V_D = 65 V, I_{DQ} = 1.5 A (combined), Temp = +25 °C, Pulse Width = 100 us, Duty Cycle = 10%

RF Characterization – Mismatch Ruggedness at 1.0 GHz [1, 2, 3]

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 65 V, I_{DQ} = 1.5 A (combined)
2. Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector
3. Pulse: 100us, 10% Duty cycle

Thermal and Reliability Information – Pulsed [1]



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case backside Temperature Pdiss = 518 W, Pulse: 100 us PW, 10% DC	0.10	°C/W
Peak IR Surface Temperature[1] (T_{ch})		131	°C

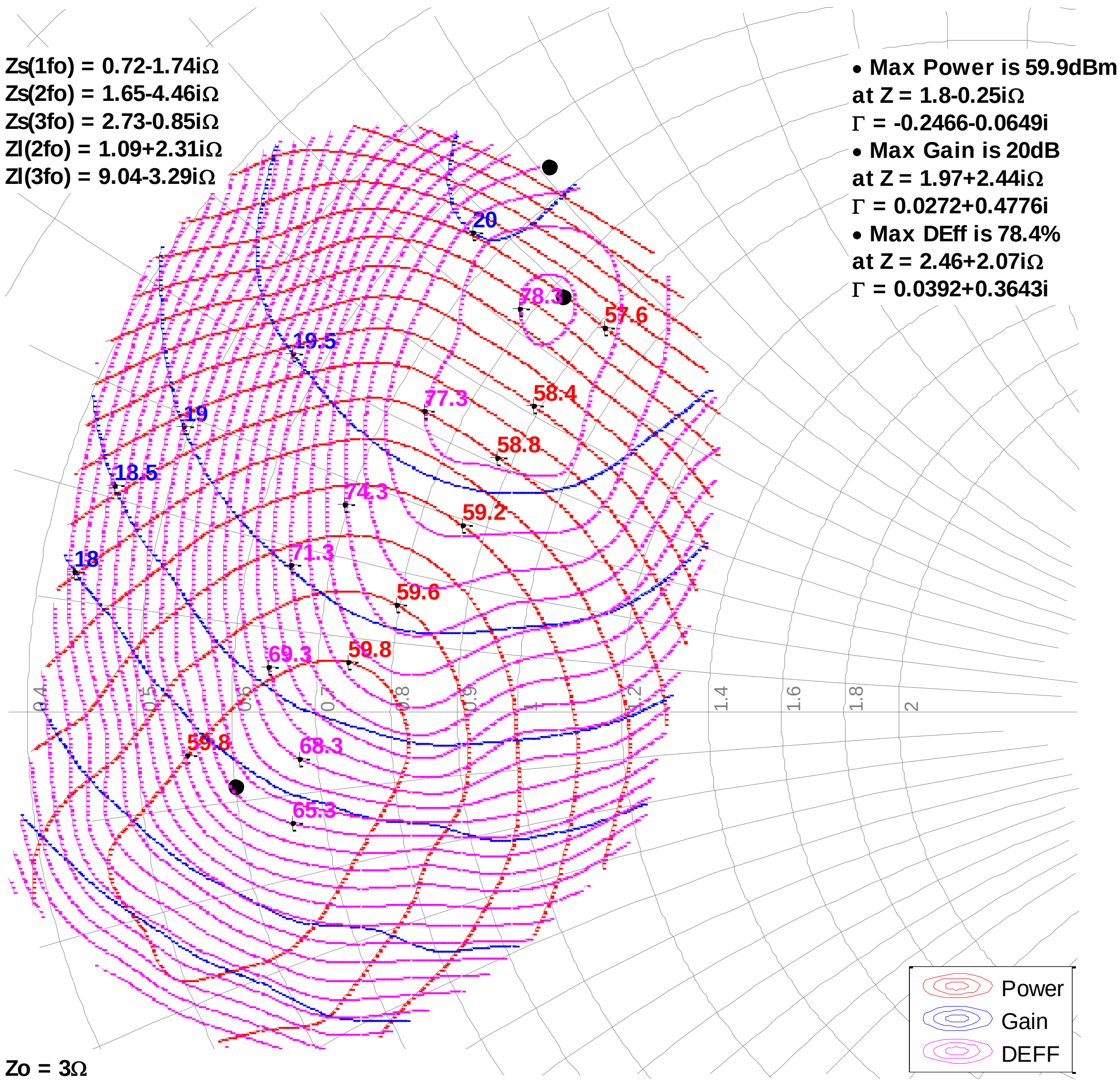
Notes:
1. Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Measured Load-Pull Smith Charts at 65 V [1, 2, 3]

Notes:

1. Test Conditions: V_D = 65 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 16 for load pull reference planes where the performance was measured.

0.915GHz, Load-pull



Zo = 3Ω
3dB Compression Referenced to Peak Gain

Measured Load-Pull Smith Charts at 65 V [1, 2, 3]

Notes:

1. Test Conditions: V_D = 65 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
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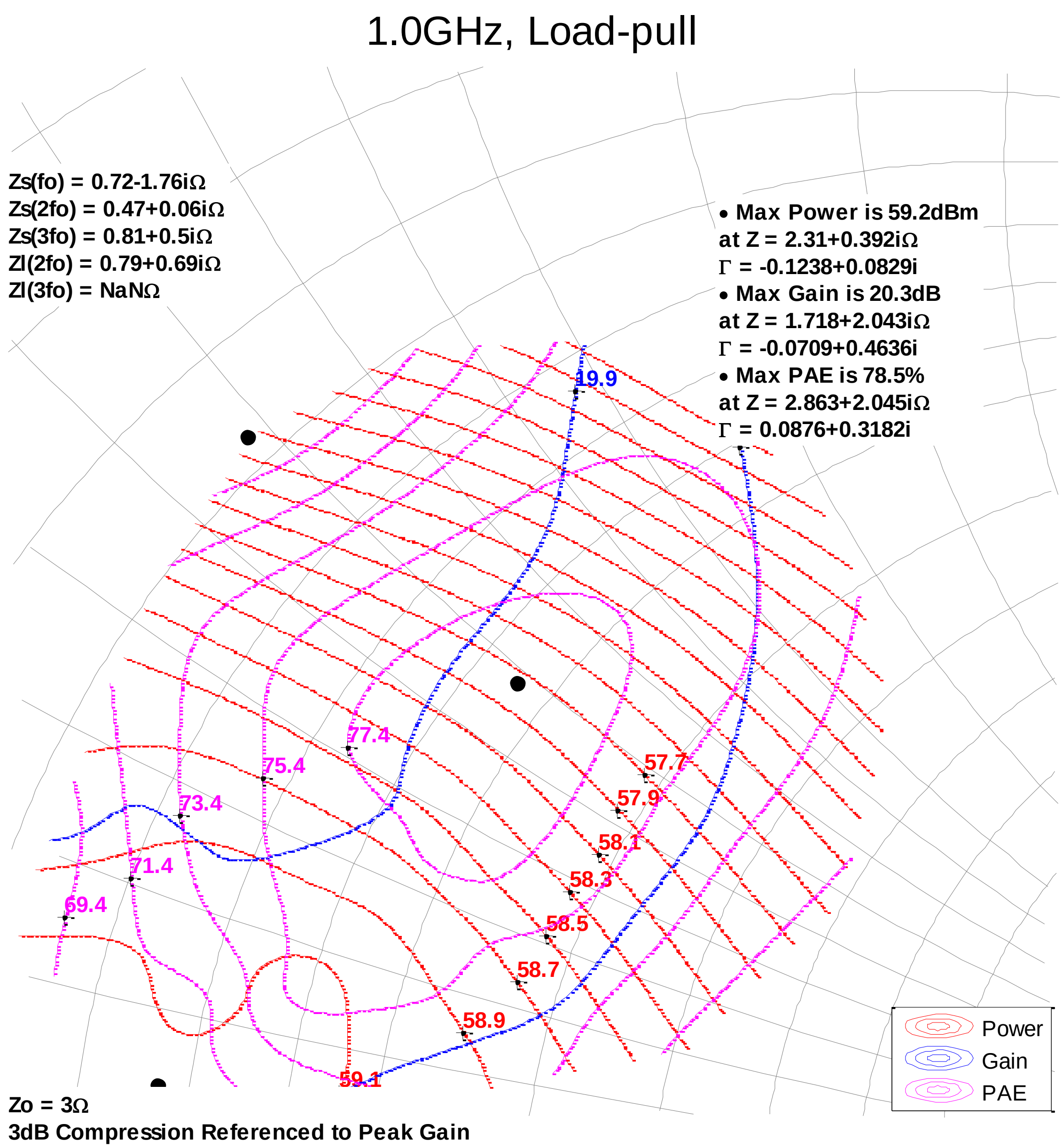

Measured Load-Pull Smith Charts at 65 V [1, 2, 3]

Notes:

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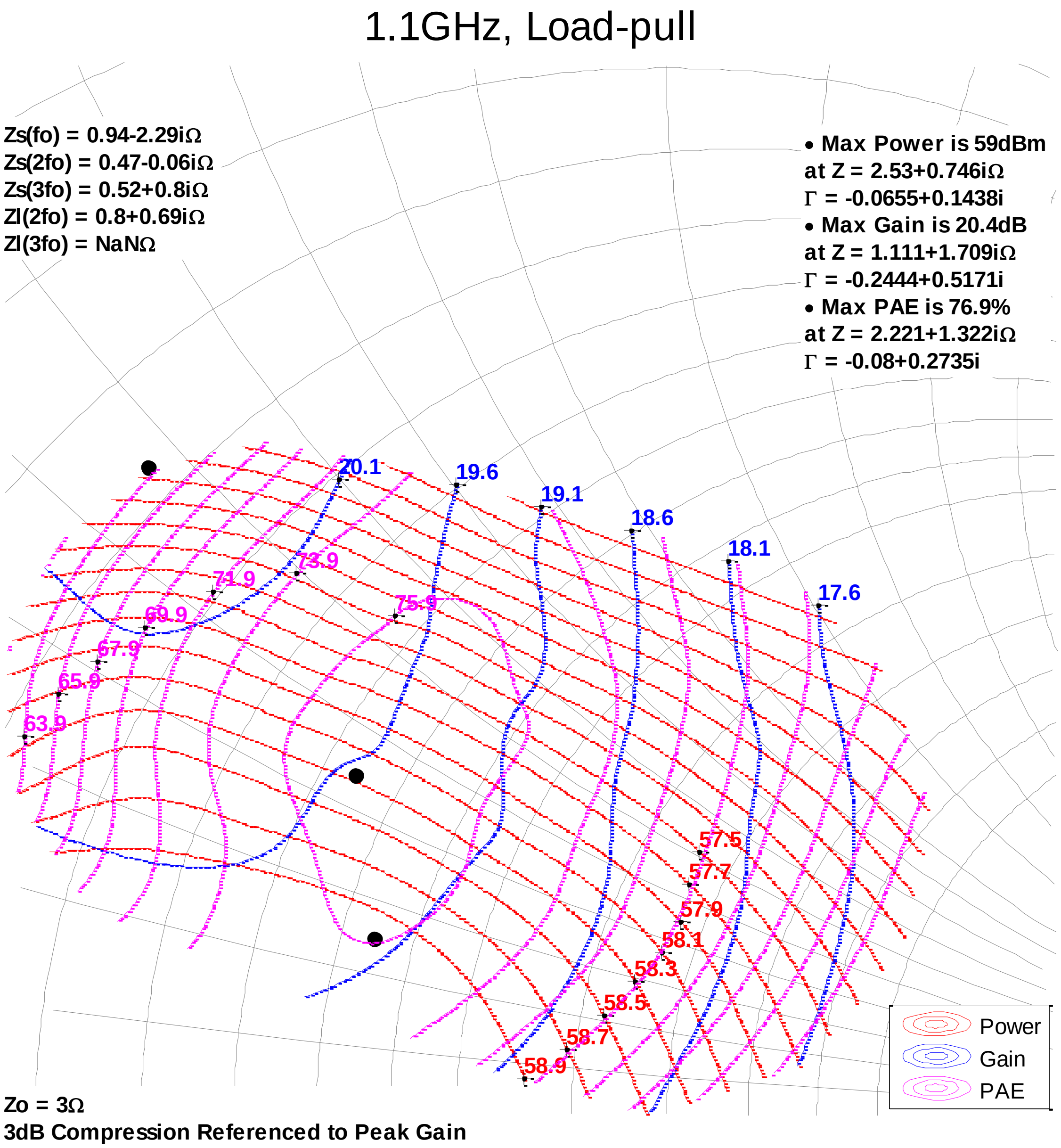

Measured Load-Pull Smith Charts at 65 V [1, 2, 3]

Notes:
1. Test Conditions: V_D = 65 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
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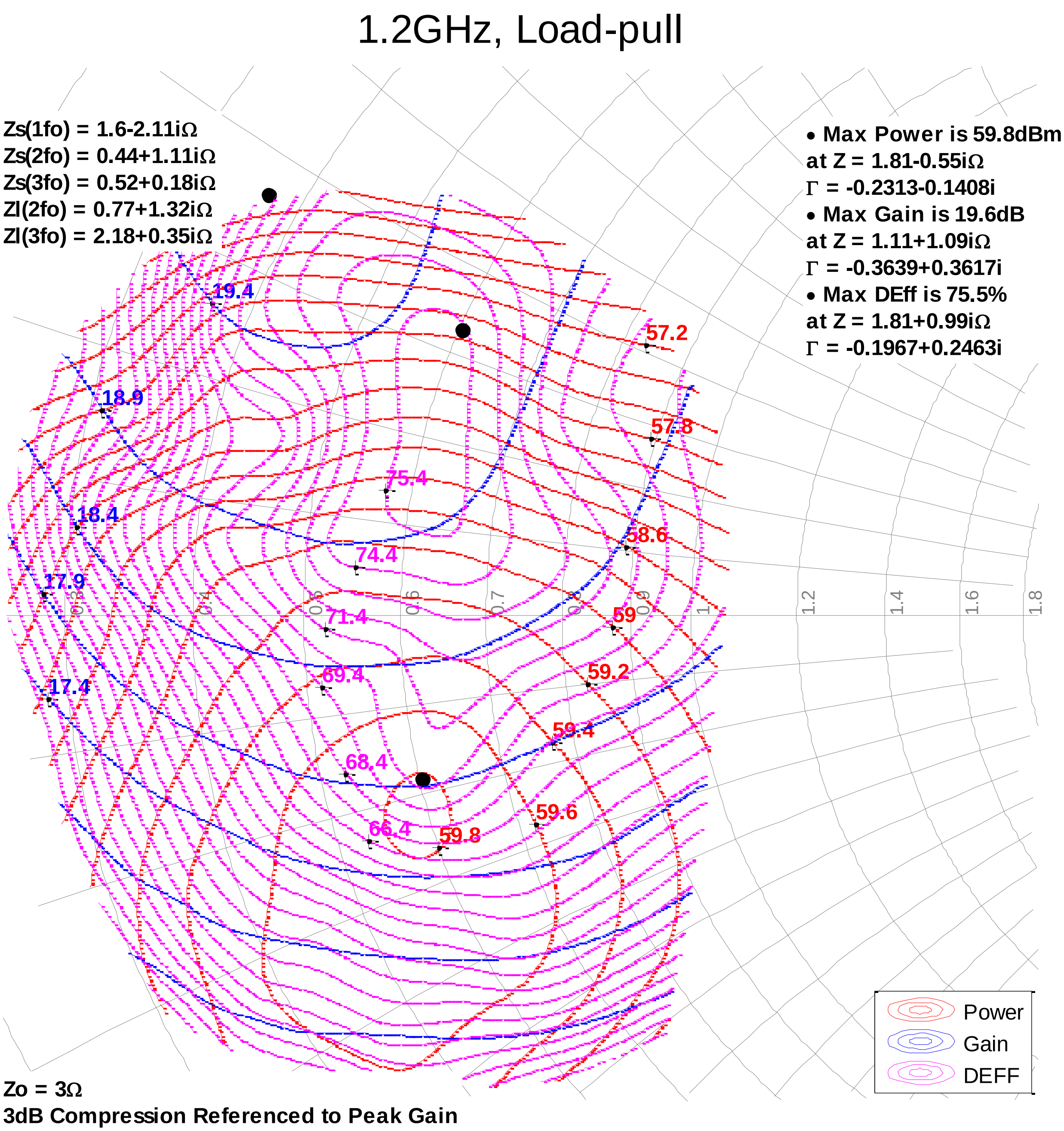
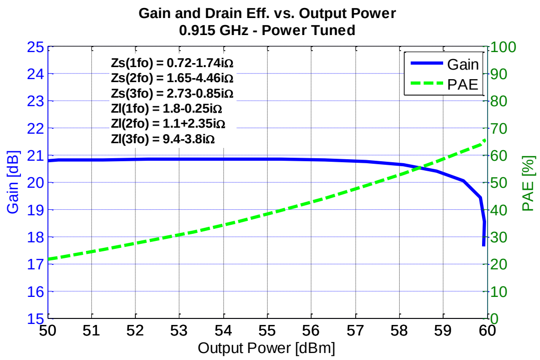
3. See page 16 for load pull reference planes where the performance was measured.

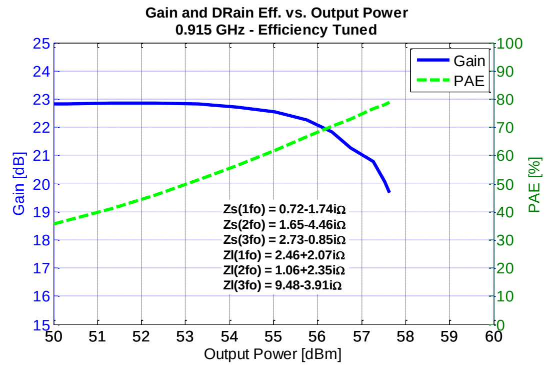


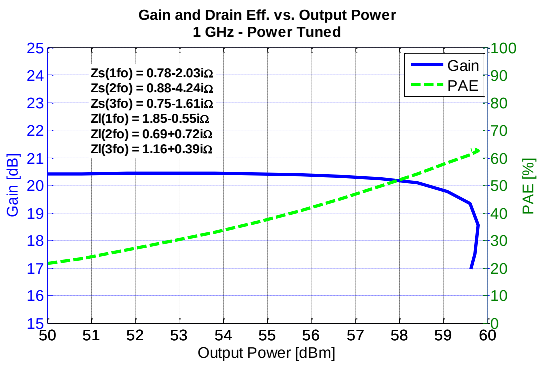
Typical Measured Performance – Load-Pull Drive-up at 65 V [1, 2, 3]

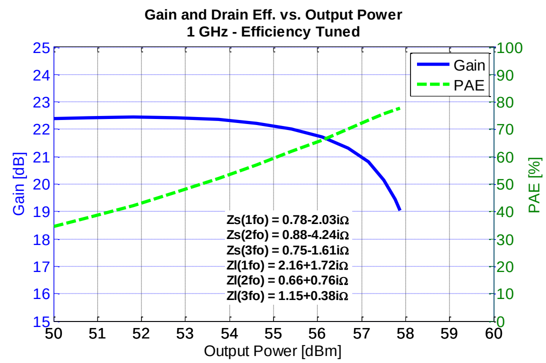
Notes:

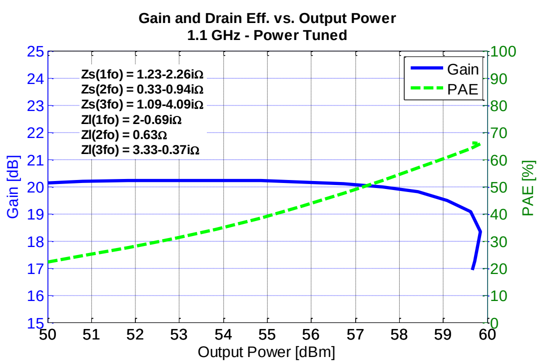
1. Test Conditions: V_D = 65 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 16 for load pull reference planes where the performance was measured.

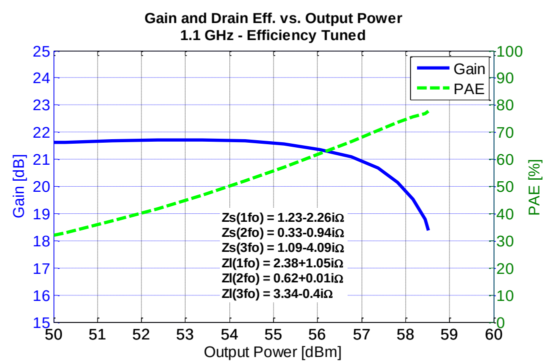


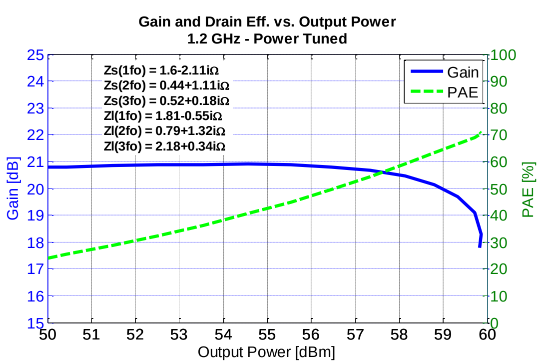


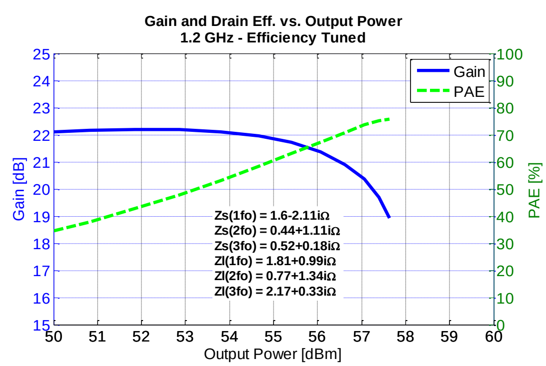








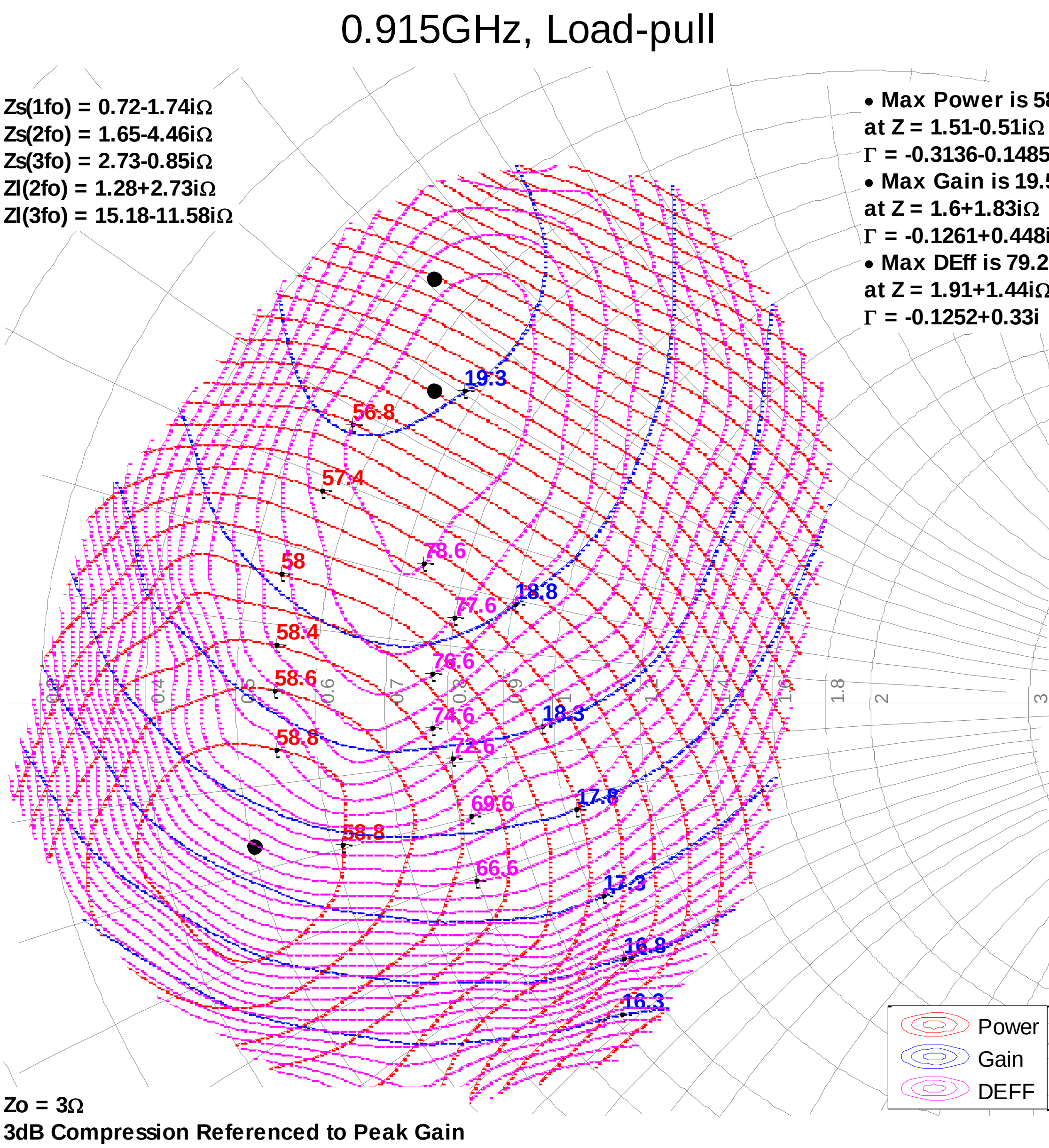




Measured Load-Pull Smith Charts at 50 V [1, 2, 3]

Notes:

1. Test Conditions: V_D = 50 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 16 for load pull reference planes where the performance was measured.



Measured Load-Pull Smith Charts at 50 V [1, 2, 3]

Notes:
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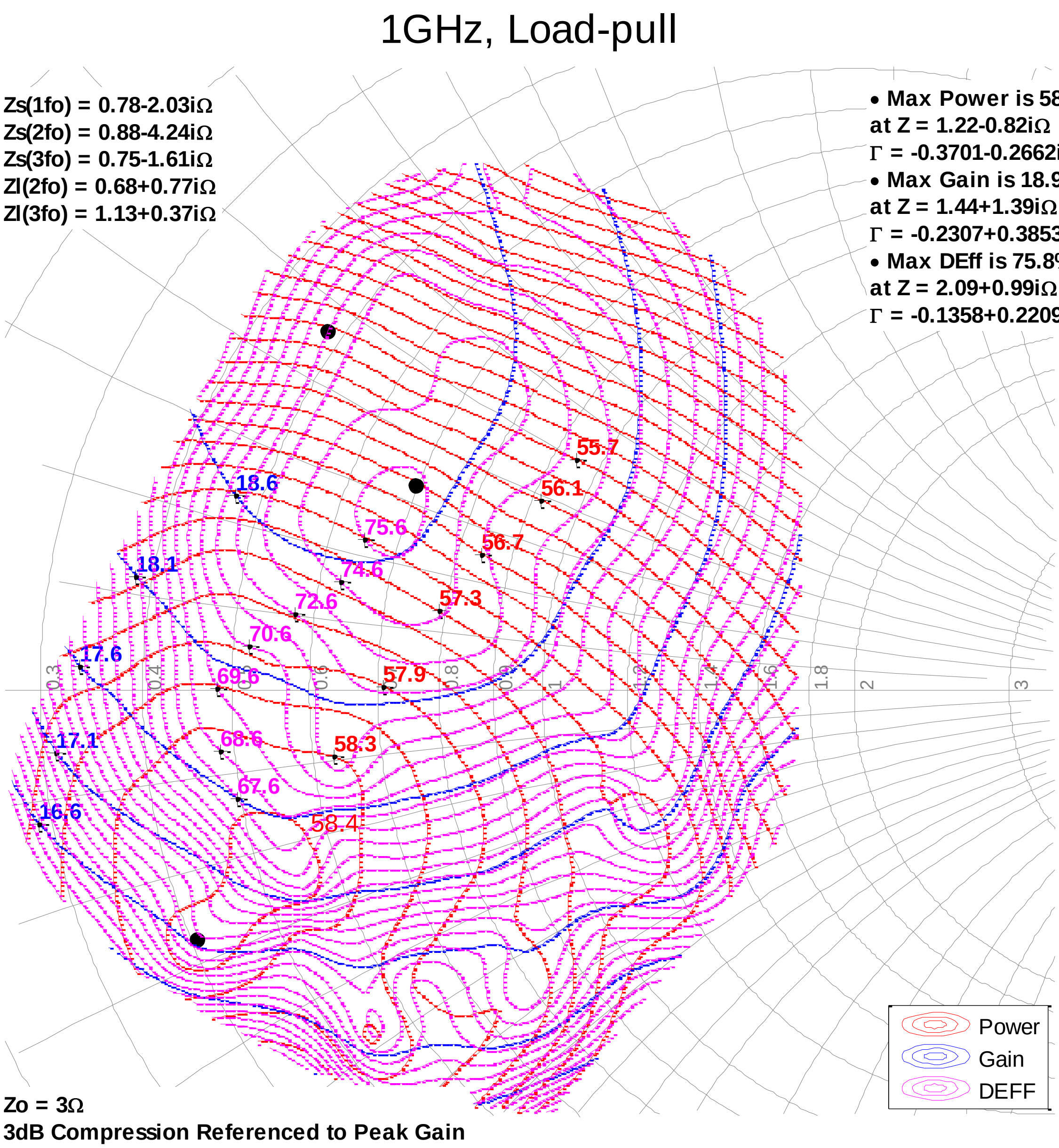

Measured Load-Pull Smith Charts at 50 V [1, 2, 3]

Notes:
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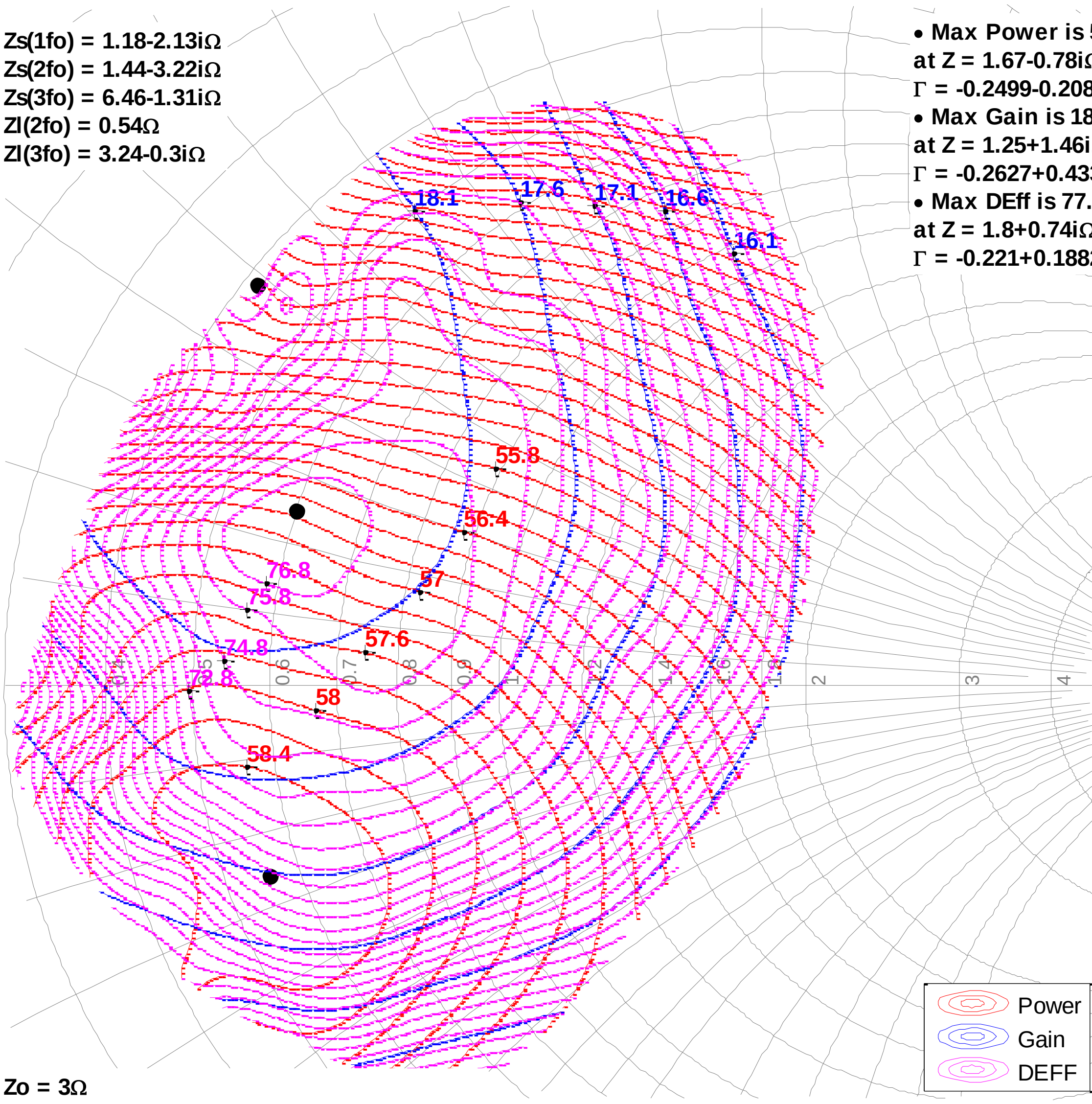
3. See page 16 for load pull reference planes where the performance was measured.

1.1GHz, Load-pull



Zo = 3Ω
3dB Compression Referenced to Peak Gain

Measured Load-Pull Smith Charts at 50 V [1, 2, 3]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
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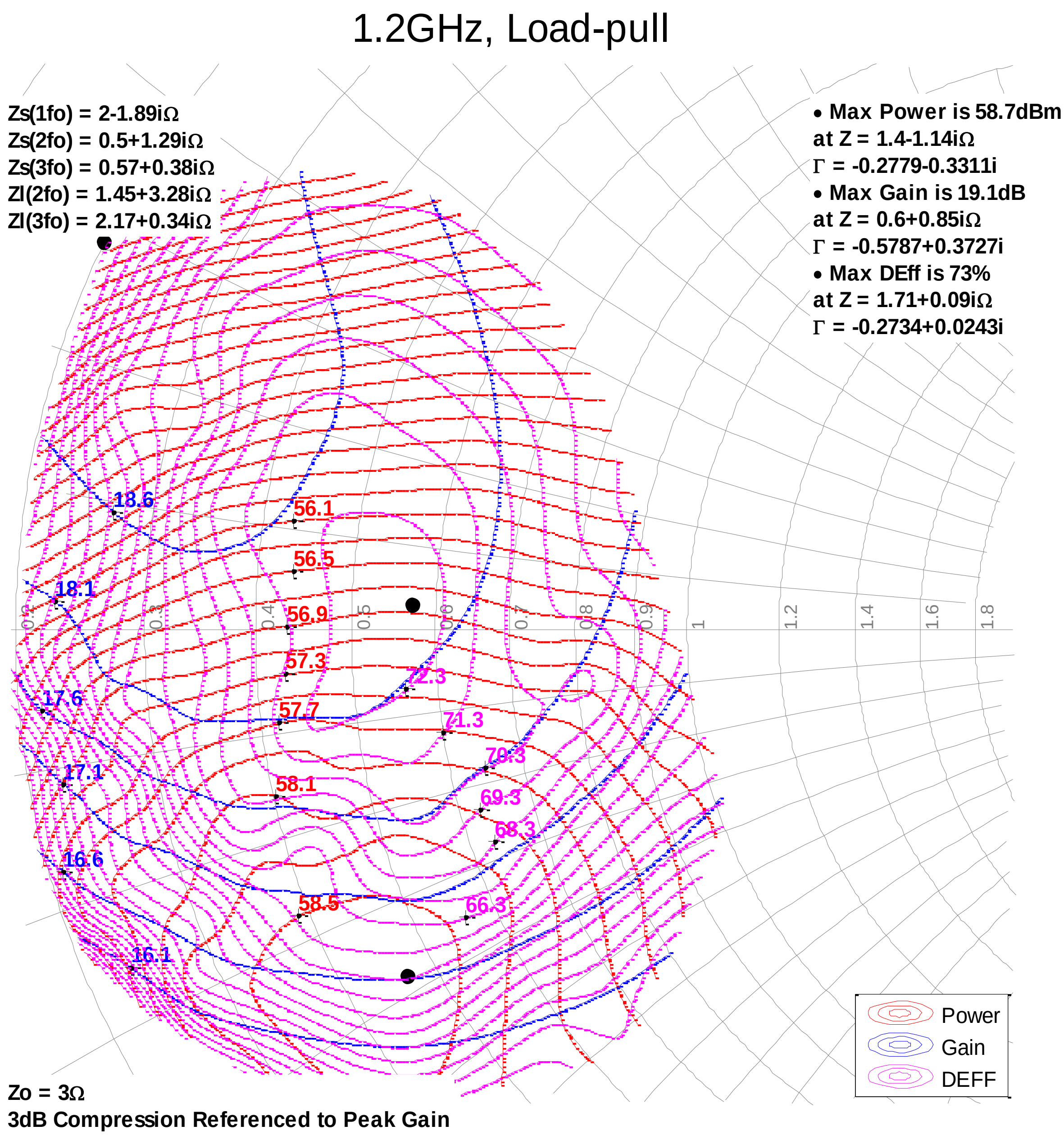
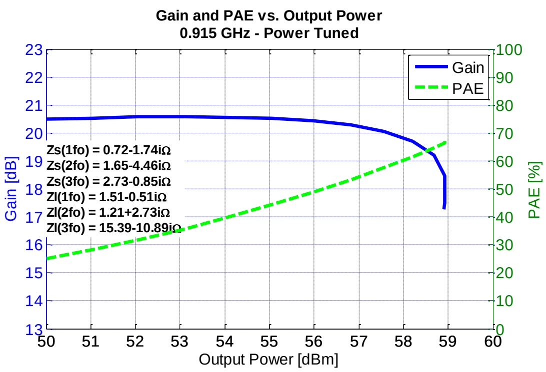
3. See page 16 for load pull reference planes where the performance was measured.

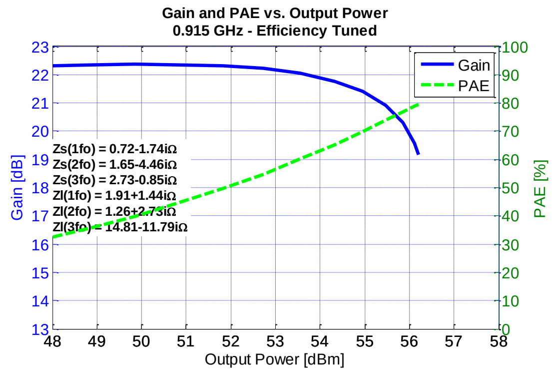


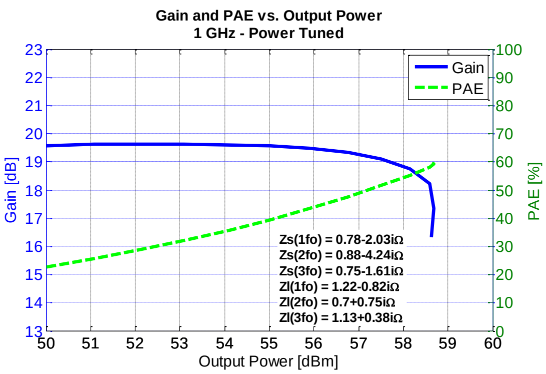
Typical Measured Performance – Load-Pull Drive-up at 50 V [1, 2, 3]

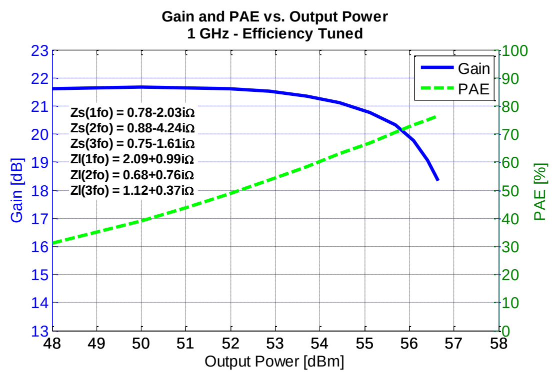
Notes:

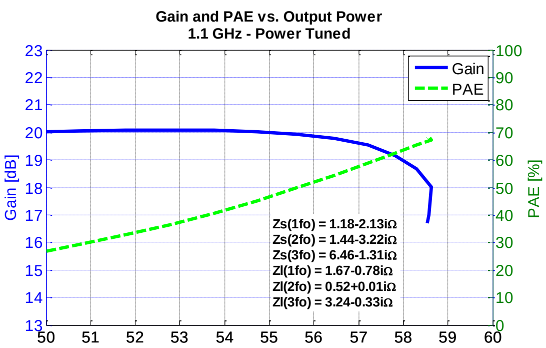
1. Test Conditions: V_D = 50 V, I_{DQ} = 750 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 16 section for load pull reference planes where the performance was measured.

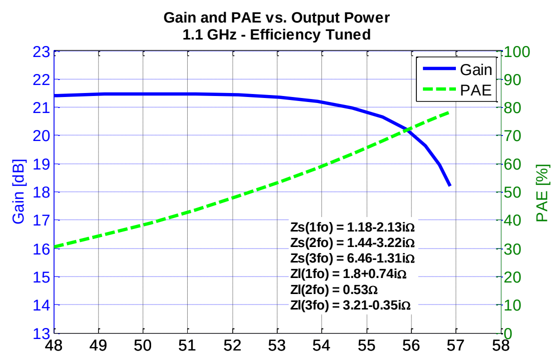


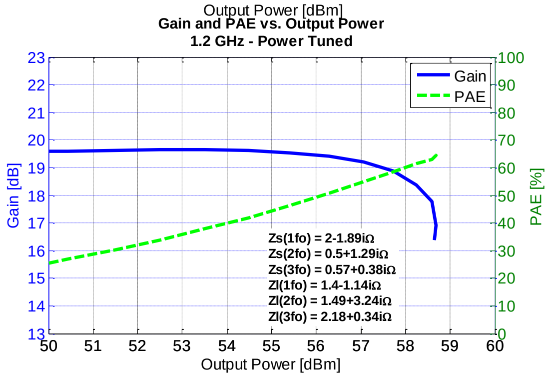


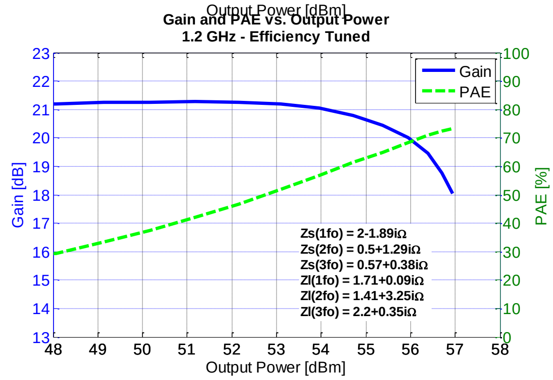




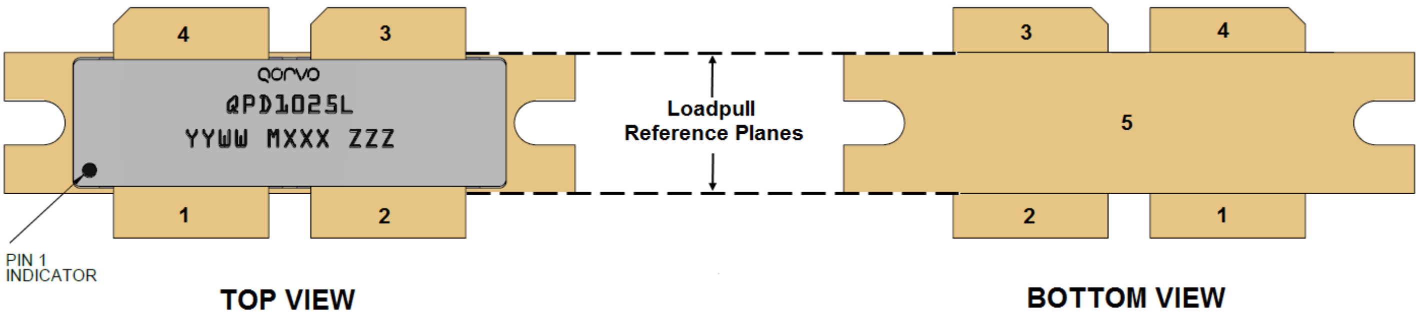








Pin Configuration and Description [1]

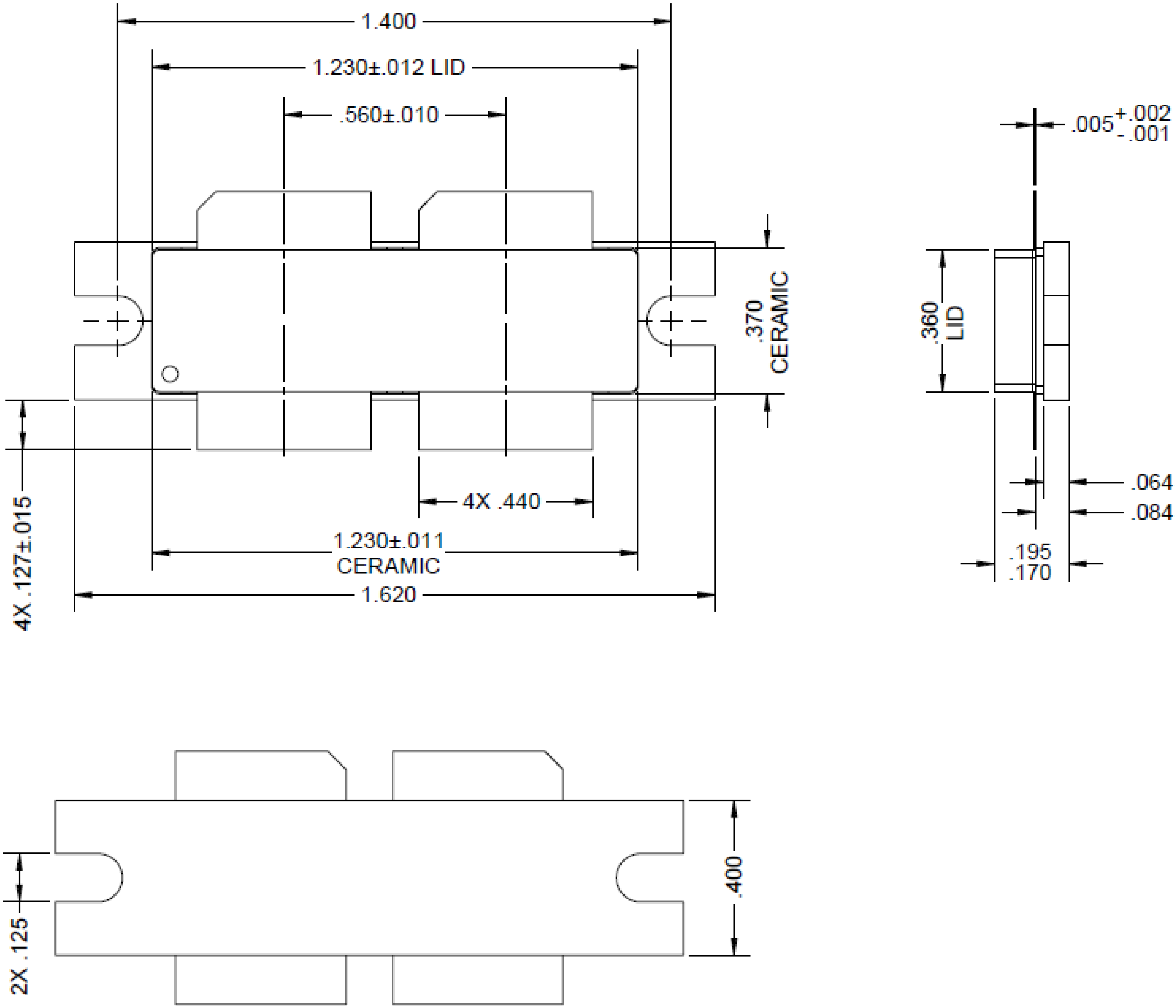


Note:

1. The QPD1025L will be marked with the "QPD1025L" designator and a lot code marked below the part designator. The "YY" represents the last two digits of the calendar year the part was manufactured, the "WW" is the work week of the assembly lot start, the "MXXX" is the production lot number, and the "ZZZ" is an auto-generated serial number.

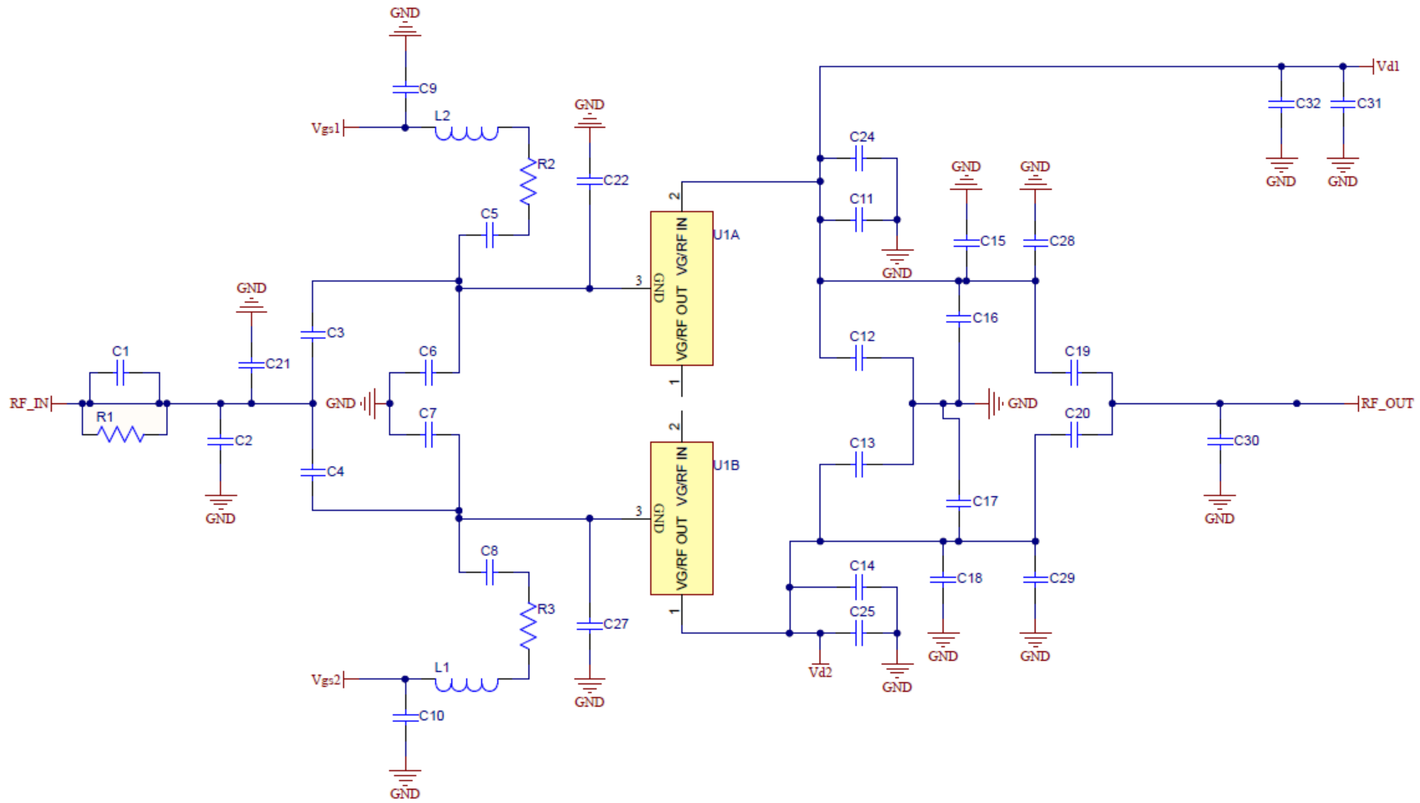
Pin	Symbol	Description
1, 2	RF IN / V_G	Gate
3, 4	RF OUT / V_D	Drain
5	Source	Source / Ground / Backside of part

Mechanical Drawing (NI-1230) [1-7]



Notes:
1. All dimensions are in inches.
2. Dimension tolerance is ± 0.005 inches, unless noted otherwise.
3. Package base: Ceramic/Metal, Package lid: Ceramic
4. Package Metal base and leads are gold plated
5. Parts are epoxy sealed.
6. Parts meet industry NI1230 footprint
7. Body dimensions do not include runout which can be up to 0.020 inches per side.

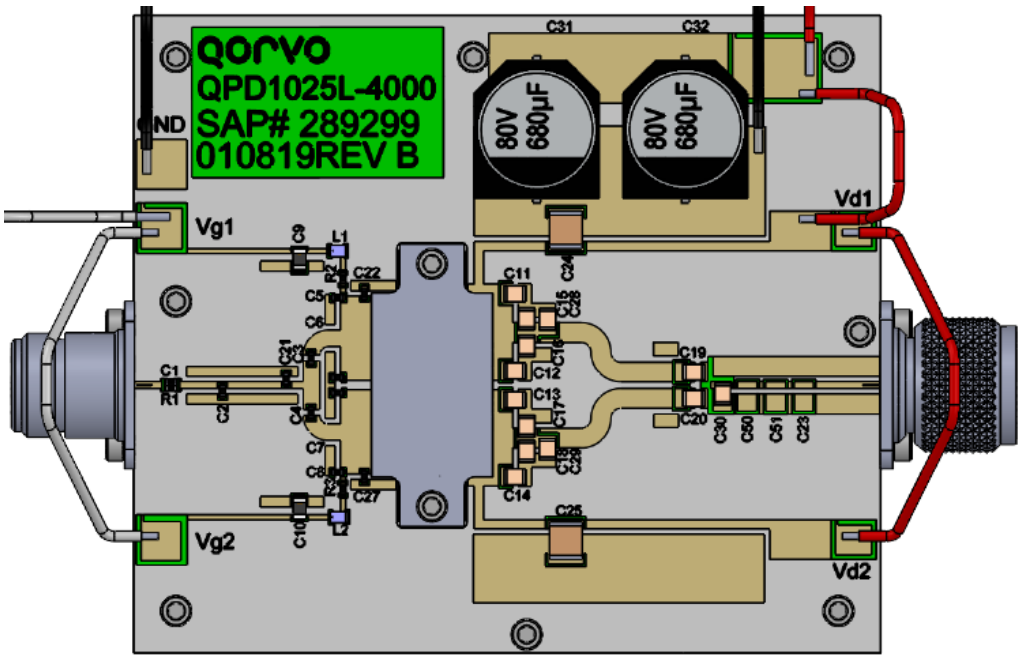
1.0 – 1.1 GHz Application Circuit - Schematic



Bias-up Procedure	Bias-down Procedure
1. Set V_G to -5 V.	1. Turn off RF signal.
2. Set I_D current limit to 4 A.	2. Turn off V_D
3. Apply 65 V V_D.	3. Wait 2 seconds to allow drain capacitor to discharge.
4. Slowly adjust V_G until I_D is set to 1.5 A.	4. Turn off V_G
5. Apply RF.	

1.0 – 1.1 GHz Application Circuit EVB1 – Layout [1, 2]

Notes:
1. PCB material is RO4350B 0.020" thick, 2 oz. copper each side.
2. The two gates could be tied together or (optionally) adjusted independently.



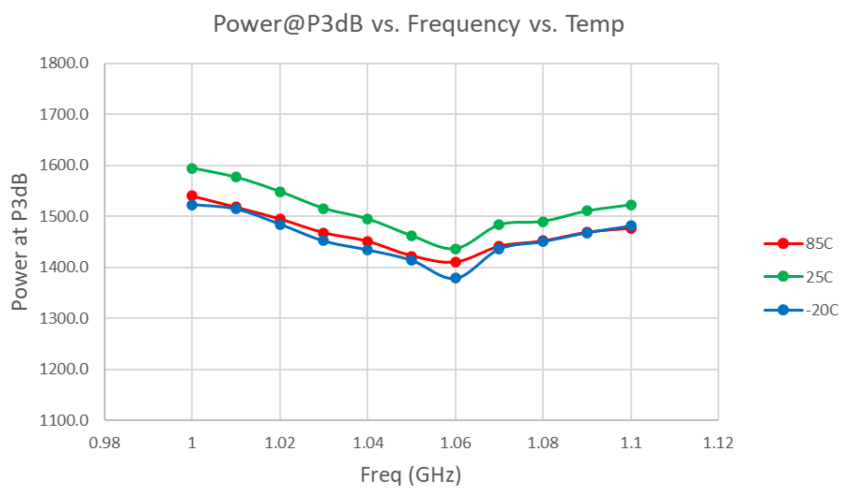
1.0 – 1.1 GHz Application Circuit – Bill of Material EVB1

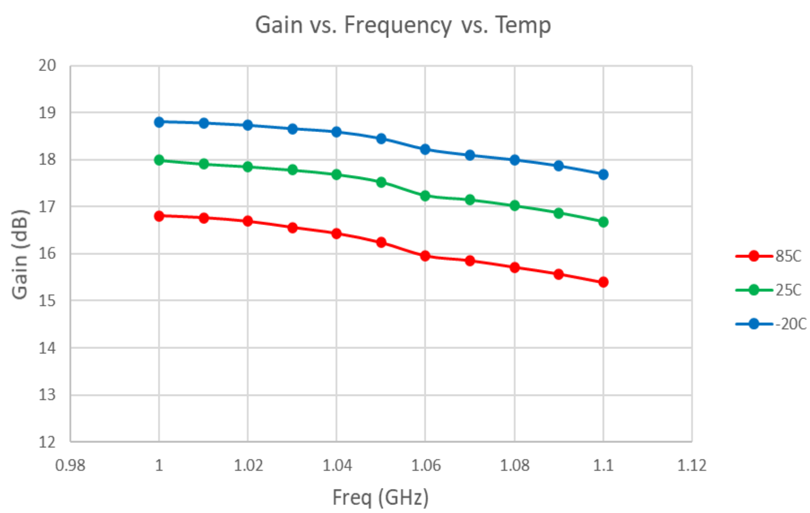
Reference Design	Value	Qty	Manufacturer	Part Number
U1		1	QORVO	QPD1025L
C1,C5,C8	8.2pF	3	American Technical Ceramics	600S8R2BT250XT
C11,C12,C13,C14	10pF	4	American Technical Ceramics	100B100JW500XT
C15,C18	5.6pF	2	American Technical Ceramics	100B5R6CT500XT
C16,C17,C28,C29	6.8pF	4	American Technical Ceramics	800B6R8CT500XT
C19,C20	56pF	2	American Technical Ceramics	800B560JT500XT
C2	0.7pF	1	American Technical Ceramics	800B560JT500XT
C21,C22,C27	6.8pF	3	American Technical Ceramics	100B100JW500XT
C24,C25	10uF	2	TDK Signapore PDE LTD	C5750X7S2A106M230KB
C3,C4	20pF	2	American Technical Ceramics	600S200FT250XT
C30	3pF	1	American Technical Ceramics	800B3R0BT500XT
C31,C32	680uF	2	Vishay Americas Inc	MAL215099708E3
	5.6pF	2	American Technical Ceramics	600S5R6BW250XT
C9,C10	4.7uF	2	Murata Electronics	GRM31CR71H475KA12L
L1,L2	110nH	2	Coilcraft, Inc	0805CS-111XJBC
R1	47	1	Panasonic Industrial Devices	KTR03EZPF47R0
R2,R3	10	2	Vishay Dale Electronics	CRCW060310R0FKEA
Connector	N type F/M	1	Huber+Suhner, Inc	23_N-50-0-33/133_NE

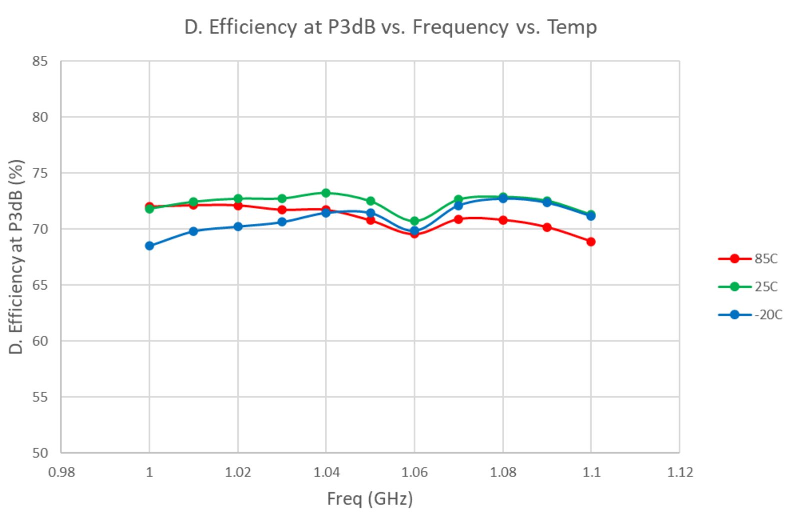
Power Driveup Performance over Temperatures of 1.0 – 1.1 GHz EVB1 [1]

Notes:

1. Test Conditions: V_D = 65 V, I_{DQ} = 1.5 A, 100 us Pulse Width, 10% Duty Cycle.



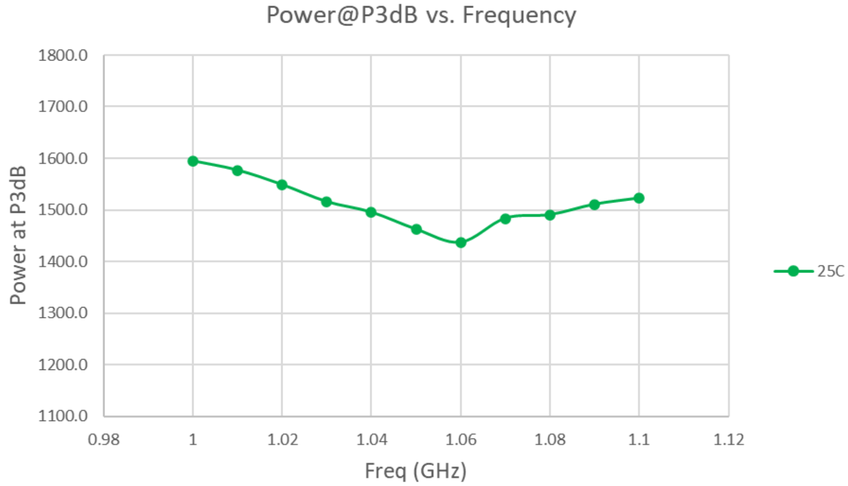


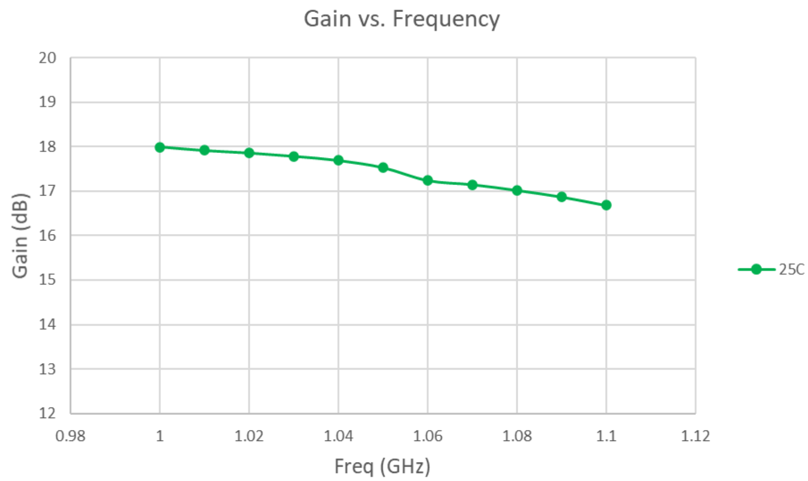


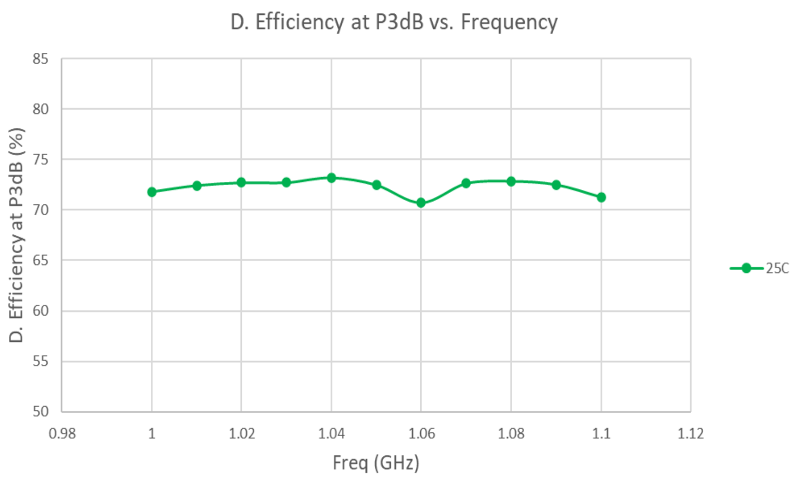
Power Driveup Performance at 25°C of 1.0 – 1.1 GHz EVB1 [1]

Notes:

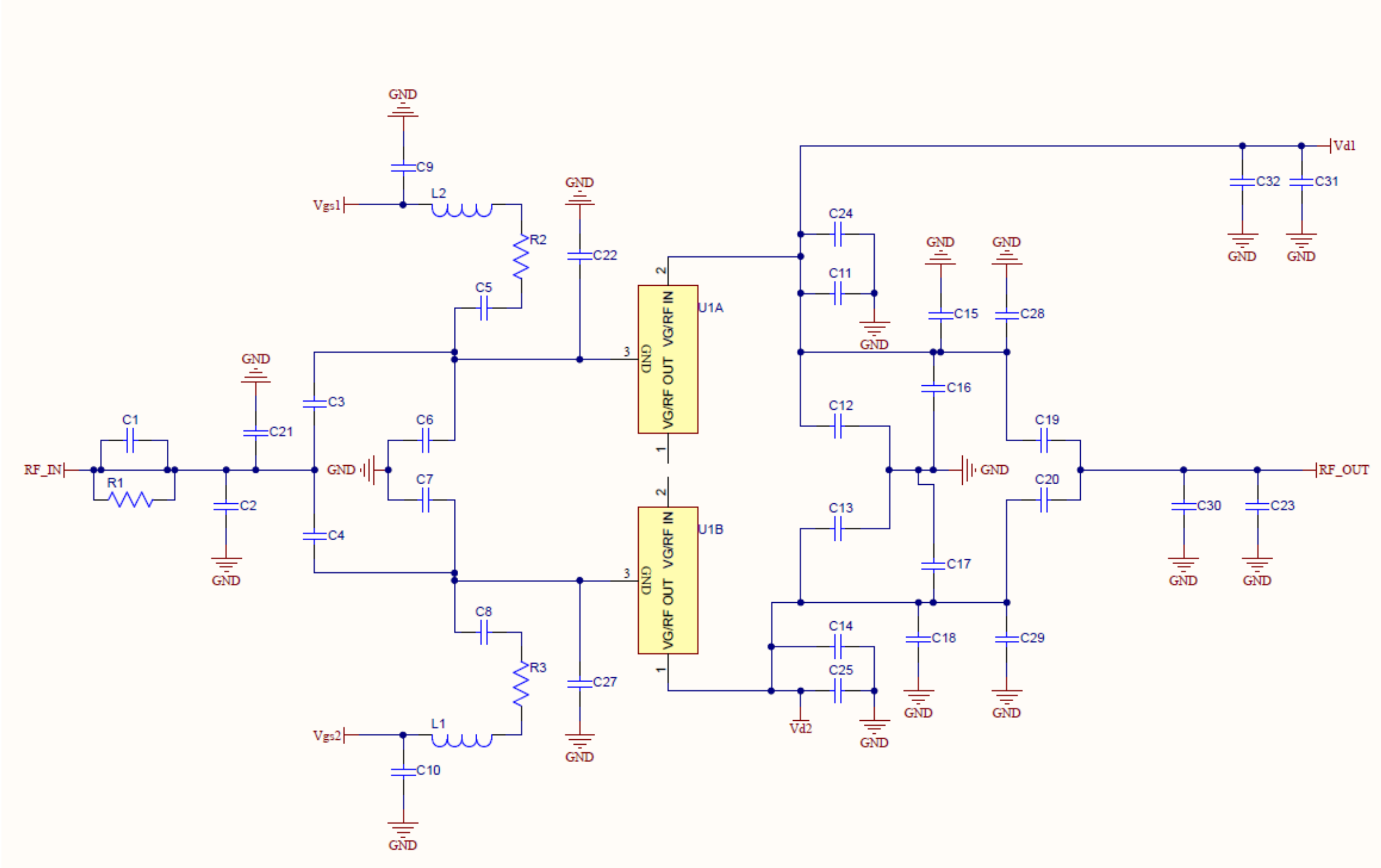
1. Test Conditions: V_D = 65 V, I_{DQ} = 1.5 A, 100 us Pulse Width, 10% Duty Cycle.







0.96 – 1.215 GHz Application Circuit EVB1 - Schematic



Bias-up Procedure

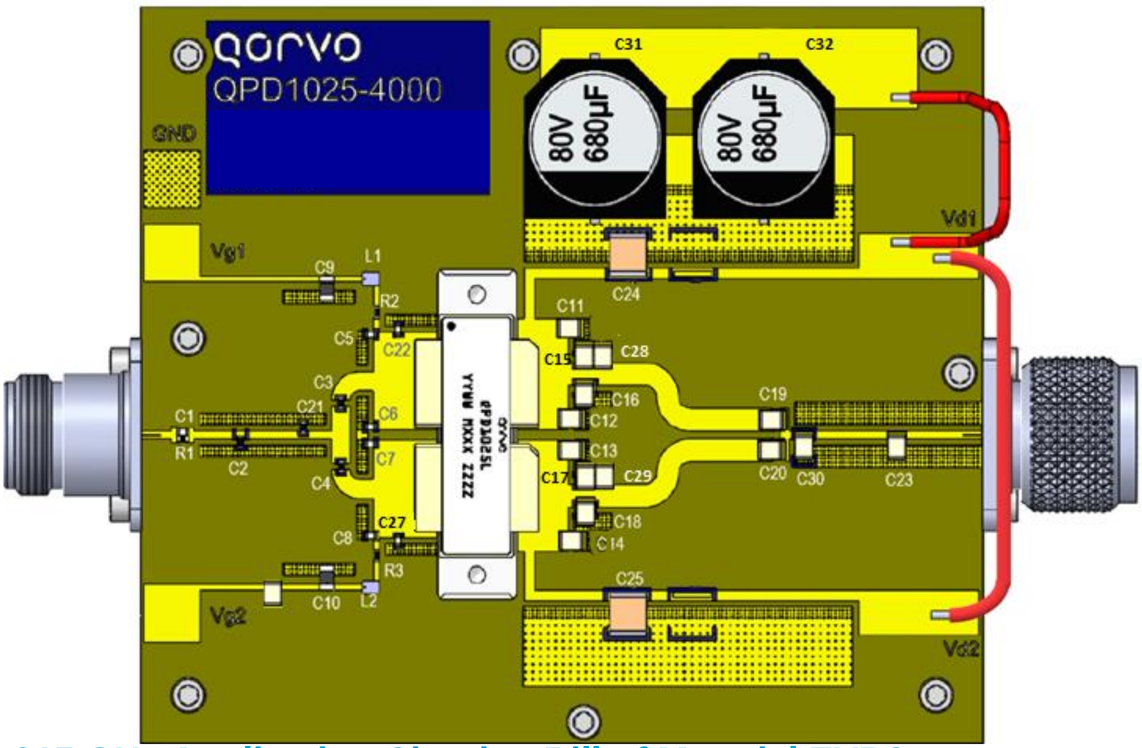
2. Set V_G to -5 V.
4. Set I_D current limit to 4 A.
5. Apply 65 V V_D.
6. Slowly adjust V_G until I_D is set to 1.5 A.
7. Apply RF.

Bias-down Procedure

3. Turn off RF signal.
4. Turn off V_D
5. Wait 2 seconds to allow drain capacitor to discharge.
6. Turn off V_G

0.96 – 1.215 GHz Application Circuit EVB2– Layout [1, 2]

Notes:
1. PCB material is RO4350B 0.020” thick, 2 oz. copper each side.
2. The two gates could be tied together or (optionally) adjusted independently.

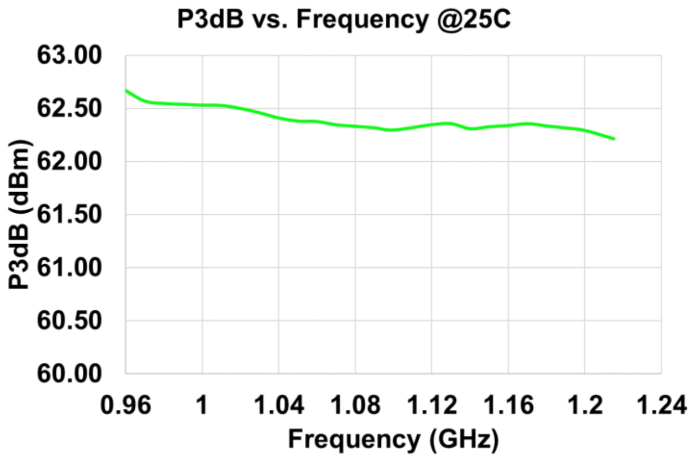


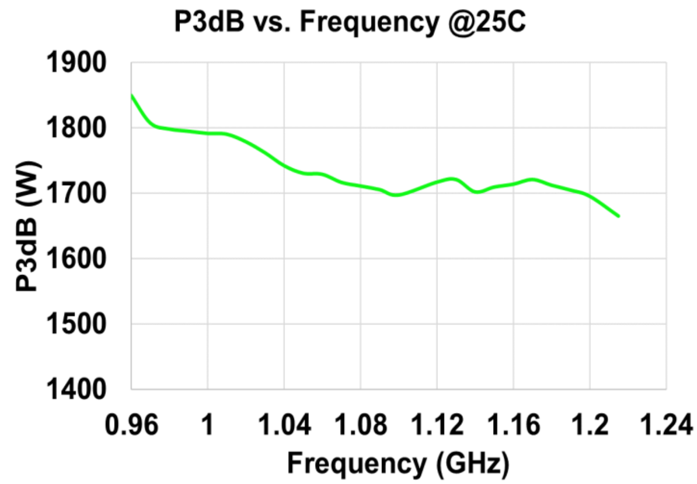
0.96 – 1.215 GHz Application Circuit – Bill of Material EVB2

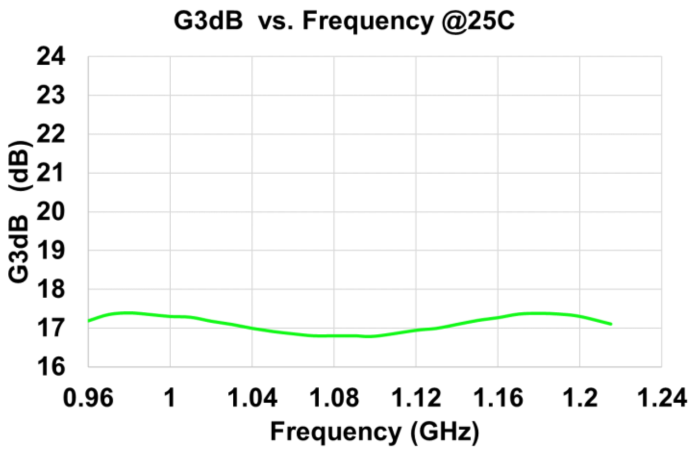
Reference Designator	Value	Qty	Manufacturer	Part Number
L1,L2	110nH	2	Coilcraft, Inc	0805CS-111XJBC
C2	0.7pF	1	American Technical Ceramics	600S0R7AT250XT
C3,C4	20pF	2	American Technical Ceramics	600S200FT250XT
C6,C7	5.6pF	2	American Technical Ceramics	600S5R6BW250XT
C21, C22, C27	6.8pF	3	American Technical Ceramics	600S6R8BT250XT
C1, C5,C8	8.2pF	3	American Technical Ceramics	600S8R2BT250XT
C19,C20	12pF	2	American Technical Ceramics	800B120GT500XT
C23	1.5pF	1	American Technical Ceramics	800B1R5BT500XT
C30	1.8pF	1	American Technical Ceramics	100B1R8BT500XT
C28,C29	2.4pF	2	American Technical Ceramics	100B2R4BT500XT
C12,C13,C15,C16,C17,C18	5.6pF	6	American Technical Ceramics	100B5R6CT500XT
C11,C14	8.2pF	2	American Technical Ceramics	800B8R2CT500XT
C24,C25	10uF	2	TDK Singapore (Pte) Ltd	C5750X7S2A106M230KB
R2,R3	10 Ohms	2	Vishay Dale Electronics	CRCW060310R0FKEA
Connector	N type F	1	Huber+Suhner, Inc	23_N-50-0-33/133_NE
Connector	N type M	1	Huber+Suhner, Inc	13_N-50-0-33/133_NE
R1	47 Ohms	1	Panasonic Industrial Devices	KTR03EZPF47R0
C9,C10	4.7uF	2	Murata Electronics	GRM31CR71H475KA12L
C31, C32	680uF	2	Vishay Americas Inc	MAL215099708E3

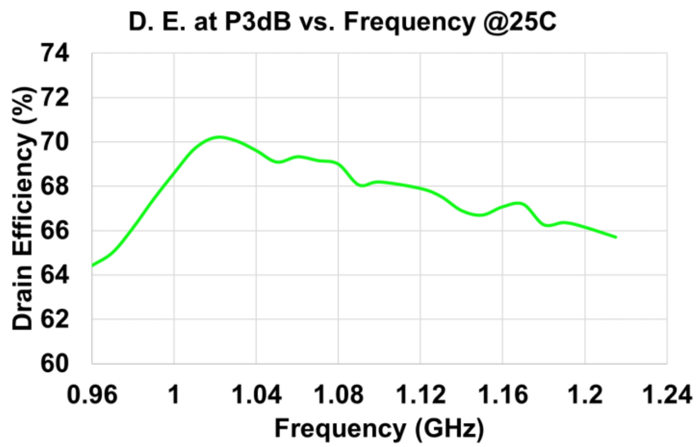
Performance at 25°C of 0.96 – 1.215 GHz EVB2 [1]

Notes:
1. Test Conditions: VD = 65 V, IDQ = 1.5 A, 100 us Pulse Width, 10% Duty Cycle.

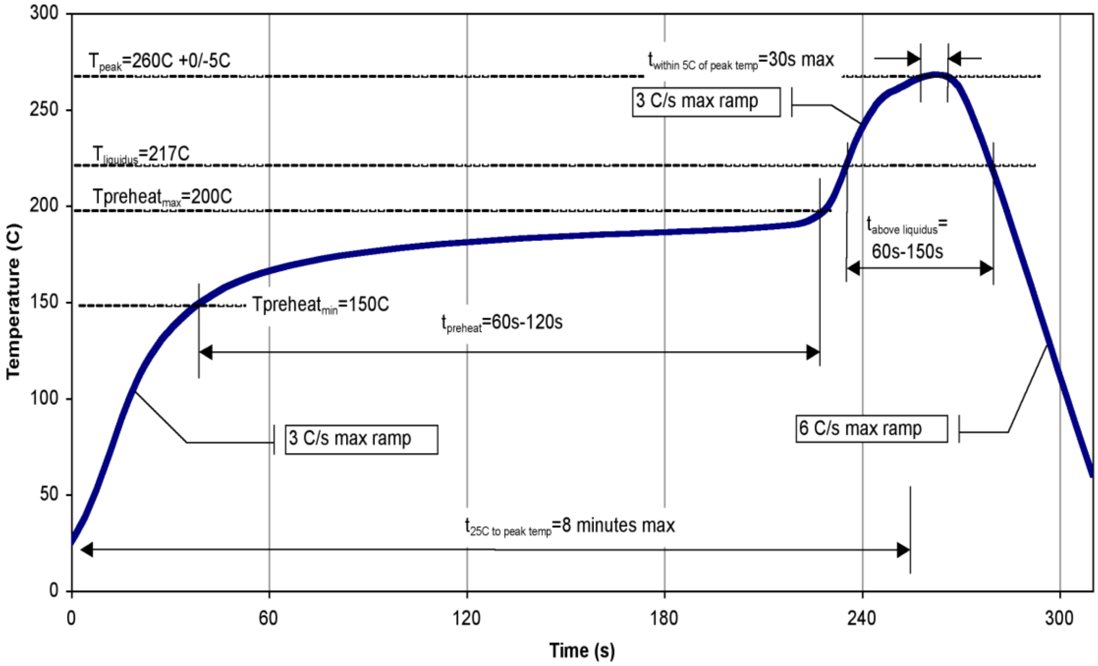








Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL3	JESD J-STD-020 (260°C Convection reflow)

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: **1-844-890-8163**

Email: customer.support@qorvo.com

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